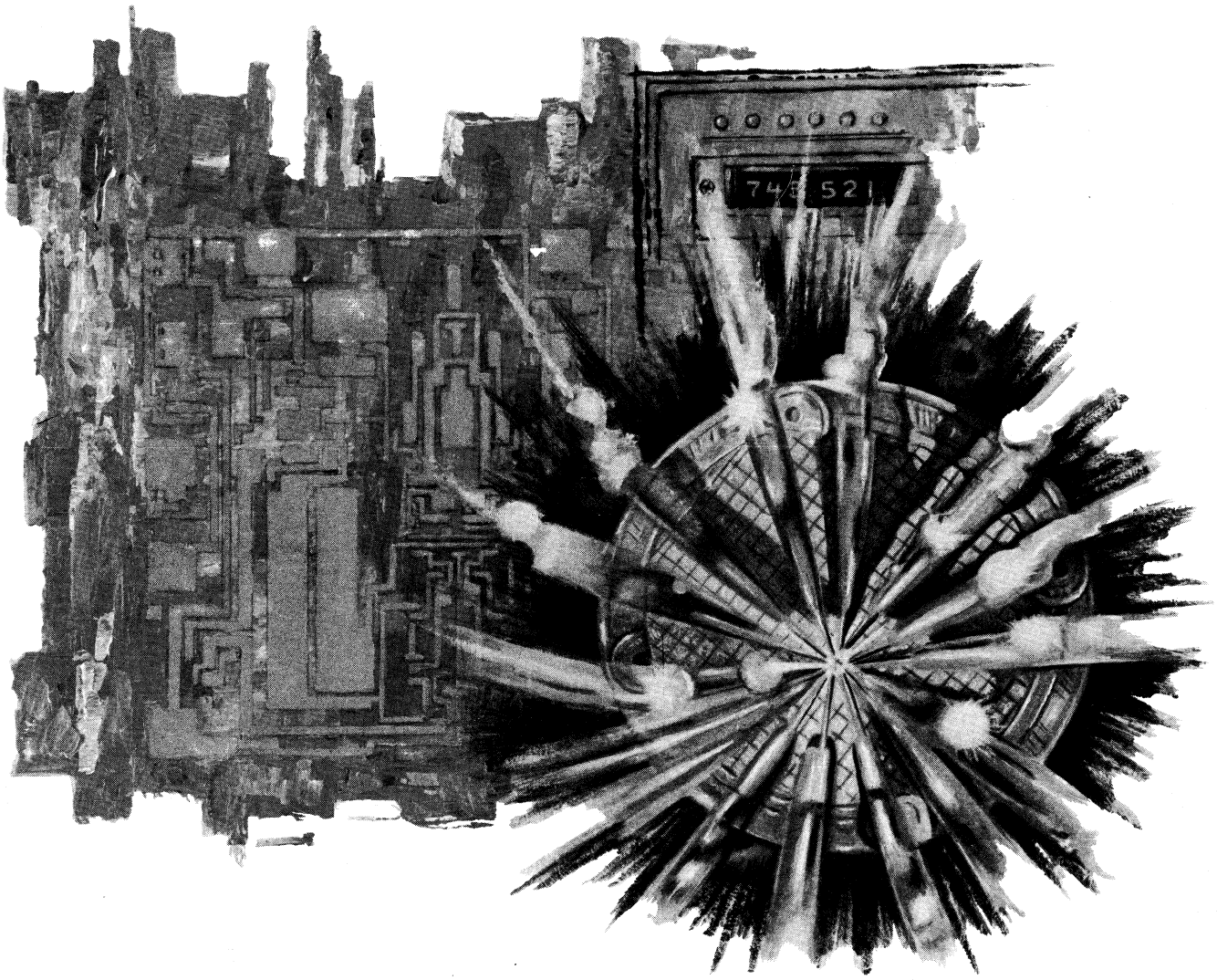
November 1972

INTEGRATED CIRCUITS CATALOG



HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HISTORY

The present Harris Semiconductor operation began in 1962 as a small integrated circuit laboratory operation of the Systems Division of Radiation Incorporated.

November 1966, the department became the Microelectronics Division of Radiation Incorporated. By that time, the operation had demonstrated a strong production capability in dielectrically isolated circuits.

By 1967, when Harris-Intertype Corporation acquired Radiation, the Microelectronics Division had developed a diverse line of both standard and custom integrated circuit products.

September 1970, the division name was changed to Harris Semiconductor; a new three-story Engineering and Manufacturing building with adjacent service building were dedicated.

Harris Semiconductor, a Division of Harris-Intertype Corporation, now occupies four buildings with a total floor space of approximately 176,000 square feet in Melbourne, Florida. These facilities are completely devoted to design, development, manufacture, and marketing of a wide variety of semiconductor devices.

PRODUCT LINE

With the broad range of technologies available at Harris Semiconductor, a standard product line consisting of linear, digital, and memory products has been established. Device families have been characterized to permit satisfaction of the cost/performance goals of both the military and industrial designer through proper product selection. Products currently in development will continue to expand the standard product line to include additional proprietary products and pin-compatible versions of popular alternate source types.

Harris has established itself as a leading supplier of high performance op amps as well as a reliable second source of popular types. Analog switches, multiplexers, D/A converters, signal comparators, and a new line of monolithic Phase Locked Loops round out Harris' growing line of LIC's serving all the end use sections of analog applications.

Memory products are comprised of PROM's™, RAM'S and programmable diode matrices. A wide range of new products will introduce advanced technologies such as CMOS and POLIPLANAR to the memory product line. With these new technologies, the memory product line will fit applications ranging from low cost mass storage to high performance buffers and scratch pads in both commercial and military systems.

Digital products include transmitter/receiver interface circuits, display drivers, keyboard encoders, special purpose circuits, and a new line of Dielectrically Isolated DI/CMOS logic functions rapidly expanding to include MSI/LSI functions offering improved performance and reliability.

The Harris Application Department has published articles which detail those design techniques best suited for maximizing the high performance available in all elements of the product line. Additional applications information is available upon request at your local Harris Field Sales Office or By calling area code: 305 - 727-5430.

CUSTOM PROGRAMS

Harris has complete custom capability in digital, analog, random logic, memory and special purpose interface circuits. Assistance in all phases of a development program can be provided from concept to volume production.

The technologies available are:

- MULTILEVEL METALIZATION
- DIELECTRIC ISOLATION (DI)
- JUNCTION ISOLATION (JI)
- THIN FILM RESISTORS
- DI-CMOS
- P-CHANNEL MOS
- CHIP PASSIVATION
- ION IMPLANTATION
- CAD MASK LAYOUT
- SCHOTTKY DEVICES
- NPN/PNP COMPLEMENTARY TRANSISTORS
- J-FETS

Contact Product Marketing, (305) 727-5430, for further information.

HARRIS DASH 8 PROGRAM

Off-the-shelf delivery. Process in accordance with MIL-STD-883 Class B screening. Harris' reliability add-on program provides generic Group B and Group C data. Contact (305) 727-5430 for product pricing. Minimum order $250.00 per line item. Group B and Group C prices quoted on request.

EXPLANATION OF HARRIS PRODUCT CODE

HARRIS PRODUCTS ARE DESIGNATED BY "PRODUCT CODE." WHEN ORDERING, PLEASE REFER TO PRODUCTS BY THE FULL CODE. HARRIS PRODUCTS WILL ALWAYS BEGIN WITH H. SPECIFIC DEVICE NUMBERS WILL ALWAYS BE ISOLATED BY HYPHENS.

EXAMPLE:

HARRIS LOGO (LETTER – H)
FAMILY DESIGNATION (LETTERS)
PACKAGE TYPE (NUMBERS)
SPECIFIC DEVICE TYPE (NUMBERS & LETTERS)
TEMPERATURE RANGE (NUMBERS)

H PROM 1 – 1024 – 5

PACKAGE (NUMBERS)

1 – DUAL IN-LINE
2 – TO-5 TYPE
9 – FLAT PACKAGE
7 – MINIDIP
0 – CHIP FORM

SPECIFIC DEVICE (NUMBERS)

HPROM-1024 (EXAMPLE ONLY)

TEMPERATURE RANGE (NUMBERS)

2 – -55°C to +125°C
3 – -55°C to +125°C (Reduced Parameter Values)
4 – -25°C to +85°C
5 – 0°C to +75°C
6 – 100% +25°C PROBE (DICE ONLY)
8 – DASH 8 PROGRAM MIL-STD-883 CLASS B HA2-2700-8 (EXAMPLE ONLY)
9 – -40°C to +85°C

FAMILY (LETTERS)

A – AMPLIFIER
D – DIGITAL
M – DIODE MATRIX
PROM* – FIELD PROGRAMMABLE READ-ONLY MEMORY
RAM – RANDOM ACCESS MEMORY
ROM – READ-ONLY MEMORY, MASK PROGRAMMABLE
S – MSI/LSI
T – TRANSISTOR ARRAY

*PROM™ is the trademark of Harris Semiconductor for its family of memory products which can be programmed in the field.

HARRIS/ INTEGRATED CIRCUITS

Linear

- Data Sheets
- Application Notes
- Chip Data Sheets

Digital

- Data Sheets
- Application Notes

Memory

- Data Sheets
- Application Notes

Dash 8

- MIL-STD-883 Off-the-Shelf

Linear

Data Sheets

Application Notes

Chip Data Sheets

LINEAR DATA SHEETS

HA-909/911	Operational Amplifiers
HA-2000/2005/2000A/2005A	F.E.T. Input Preamplifier
HA-2050/2055/2050A/2055A	High Slew Rate F.E.T. Input Operational Amplifiers
HA-2060/2065/2060A/2065A	Wide Band F.E.T. Input Operational Amplifiers
HA-2101	Operational Amplifiers
HA-2101A/2201A	Operational Amplifiers
HA-2107/2207	Operational Amplifiers
HA-2107-3	Operational Amplifier
HA-2111/2211	Voltage Comparators
HA-2311	Voltage Comparator
HA-2400/2404/2405	PRAM Four Channel Programmable Amplifier
HA-2500/2502/2505	High Slew Rate Operational Amplifiers
HA-2510/2512/2515	High Slew Rate Operational Amplifiers
HA-2520/2522/2525	High Slew Rate Operational Amplifiers
HA-2600/2602/2605	High Impedance Operational Amplifiers
HA-2620/2622/2625	Wide Band, High Impedance Operational Amplifiers
HA-2700/2704/2705	High Performance Operational Amplifiers
HA-2800/2805	Locked Loop
HA-2825	Phase Locked Loop
HI-0180/0185	8-Bit, A to D Encoder
HI-0910/1010	10-Bit, D/A Ladder Network
HI-1080/1085	8-Bit, D to A Converter High Speed Monolithic
HI-1800/1800A	Analog Switch Four-Channel
HI-1818/1828/1818A/1828A	8 Channel Analog Multiplexers
HS-1000	16 Channel Analog Multiplexer
2N4044/2N4045/2N4100 2N4878/2N4879/2N4800	DI NPN Matched Pairs
2N5117/2N5118/2N5119	DI PNP Matched Pairs

LINEAR APPLICATION NOTES

NOTE 501	HA-909 Operational Amplifier
NOTE 502	HA-909 Operational Amplifiers Performance Tailoring
NOTE 504	Automatic Phase Margin Testing
NOTE 505	A High Impedance Hystersis Circuit
NOTE 506	Equivalent Input Noise Measurements on High Gain Monolithic Operational Amplifiers
NOTE 507	A Simple Function Generator Using Operational Amplifiers
NOTE 508	Test Procedures for Operational Amplifiers
NOTE 509	A Simple Comparator Using the HA-2620
NOTE 510	A Simple Square-Triangle Waveform Generator
NOTE 511	Digital to Analog Converter Applications
NOTE 512	Counter Type A to D Converter
NOTE 514	The HA-2400 PRAM Four Channel Operational Amplifier
NOTE 515	Operational Amplifier Stability: Input Capacitance Considerations

LINEAR CHIP DATA SHEETS

CF-0185	8-Bit A to D Encoder
CF-0910/1010	10-Bit D/A Ladder Network
CF-911	High Performance, Low Noise Op Amp
CF-2101	Gen. Purpose Op Amp
CF-2101A	Gen. Purpose, Low Offset Op Amp
CF-2107	Gen. Purpose, Low Offset Current, Internally Compensated Op Amp
CF-2107-3	Gen. Purpose, Internally Compensated Op Amp
CF-2301A	Gen. Purpose Op Amp
CF-2307	Gen. Purpose, Internally Compensated Op Amp
CF-2505	High Slew Rate Op Amp
CF-2515	High Slew Rate Op Amp
CF-2525	High Slew Rate Op Amp
CF-2605	High Input Impedance Op Amp
CF-2625	Wide Band Op Amp
CF-2705	High Performance Op Amp

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-909/911

Operational Amplifiers

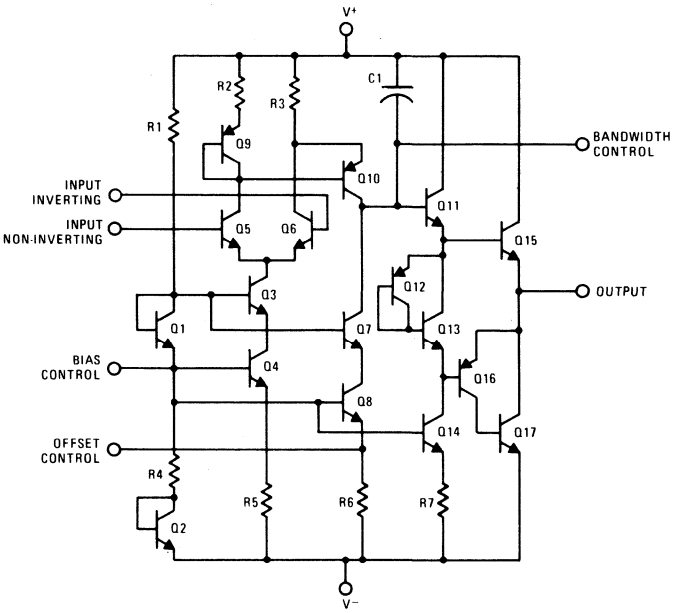
GENERAL DESCRIPTION

The integrated circuit covered by this data sheet forms a part of Harris' family of linear circuits intended for use as universal building blocks for analog circuitry. This Low Noise Operational Amplifier provides the 6dB per octave high frequency roll-off required for unconditional stability in operational feedback connections without the use of external compensation networks.

Simple resistive trim adjustment for zeroing input offset voltage is provided on the TO-86 package. The circuit is comprised of vertical NPN and PNP transistors in separate dielectrically isolated islands using advanced isolation techniques. These advanced production processes give the designer access to high performance integrated circuits without the technical compromises necessary with conventional junction isolation and lateral PNP fabrication methods.

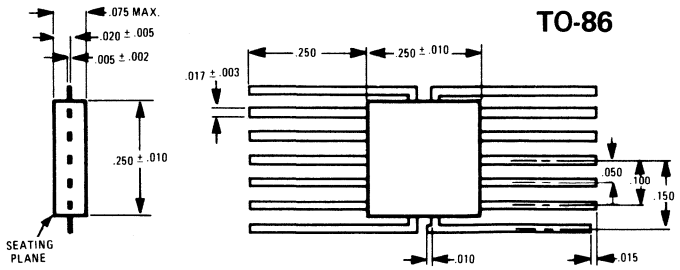
The circuit is designed to meet or exceed the mechanical and environmental requirements of MIL-STD-883.

SCHEMATIC

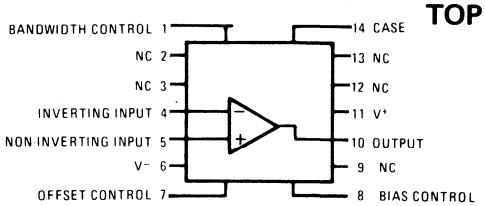


PACKAGES

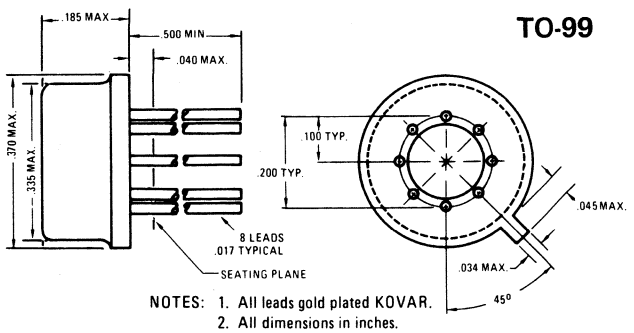
TO-86



TO-86 TOP VIEW

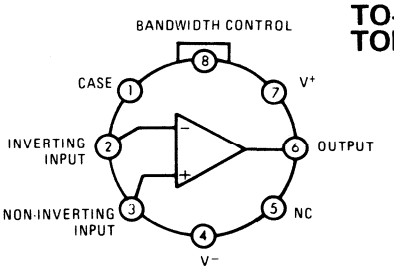


TO-99



NOTES: 1. All leads gold plated KOVAR.
2. All dimensions in inches.

TO-99 TOP VIEW



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals		50.0V
Differential Input Voltage		±7.0V
Peak Output Current		±50mA
Internal Power Dissipation		300mW
Operating Temperature Range –	HA-909	$-55^oC \leq T_A \leq +125^oC$
	HA-911	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

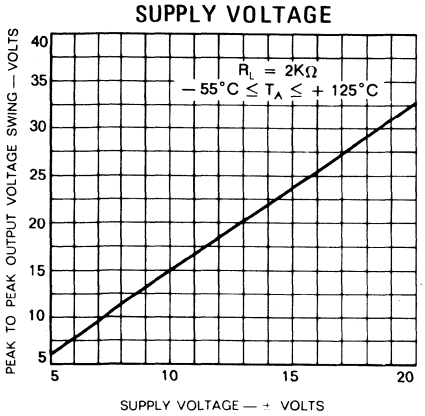
ELECTRICAL CHARACTERISTICS

PARAMETER	TEMPERATURE	HA-909 −55°C to +125°C MIN.	HA-909 TYP.	HA-909 MAX.	HA-911 0°C to +75°C MIN.	HA-911 TYP.	HA-911 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2.0	5.0		2.0	6.0	mV
	Full			6.0			7.5	mV
Equivalent Input Noise (Note 9)			1.0	5.0		1.0		μV
Bias Current	+25°C		87	300		200	500	nA
	Full			750		300	750	nA
Offset Current	+25°C		25	150		100	300	nA
	Full		50	300		150	450	nA
Offset Current Average Drift	Full		1.0			1.0		nA/°C
Input Resistance	+25°C	200	600		100	250		KΩ
	Full	100	300					KΩ
Common Mode Range	Full		±12.0		±12.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	25K	45K		20K	45K		V/V
	Full	25K	45K		15K	45K		V/V
Common Mode Rejection Ratio (Note 2)	Full	80	96		74	90		dB
Unity Gain Bandwidth (Note 3)	+25°C		7			7		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±12.0			±11.0			V
Output Current (Note 4)	+25°C	±20			±15			mA
Output Resistance	+25°C		150			500		Ohms
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		40	75		40	75	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		15	40		15	40	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	+3.5	+5.0			+5.0		V/μs
	Full	−1.2	−2.0			−2.0		
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		1.8	2.5		1.8	2.5	mA
Power Supply Rejection Ratio (Note 7)	Full	80	92		74	90		dB

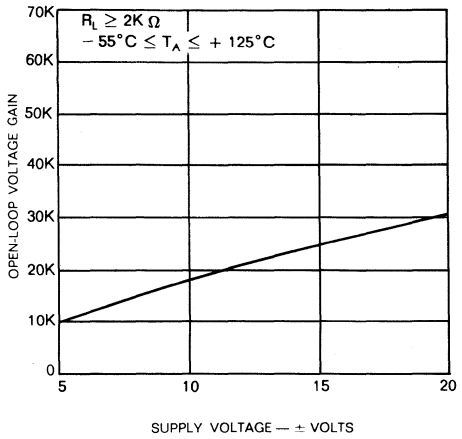
NOTES:
1. R_L = 2KΩ
2. V_{CM} = ±5.0V
3. V_O < 90mV
4. V_O = ±10.0V
5. C_L = 100pF
6. V_O = ±200mV
7. V_{Sup} = ±9.0V to ±15.0V
8. See Transient Response test circuits and waveforms – page 3.
9. 10 – 1000Hz, R_S = 10KΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

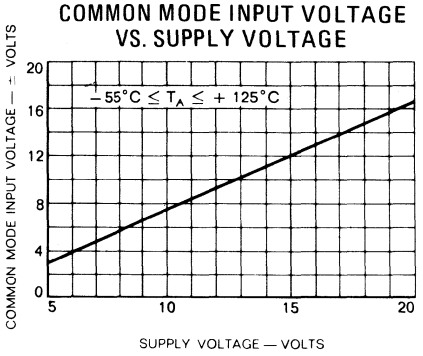
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



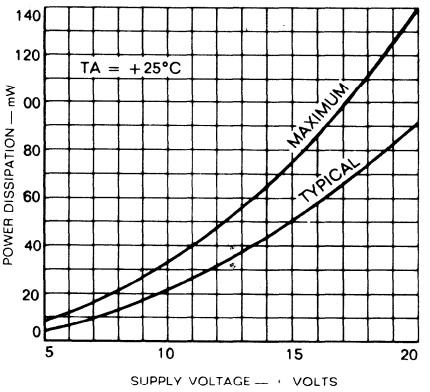
OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



COMMON MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE

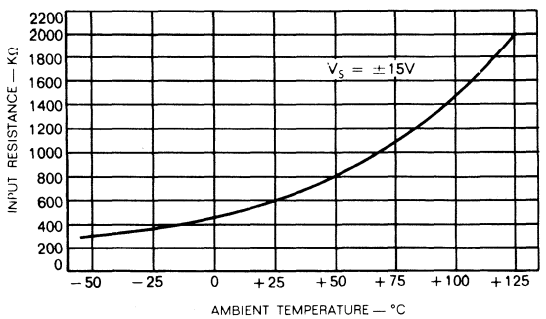


POWER DISSIPATION VS. SUPPLY VOLTAGE

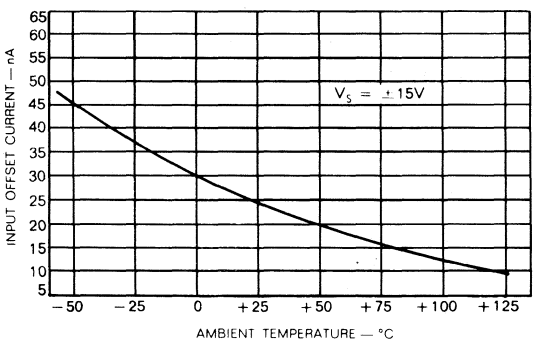


TYPICAL PERFORMANCE CURVES

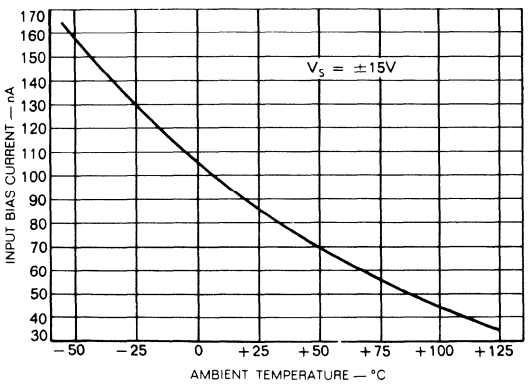
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



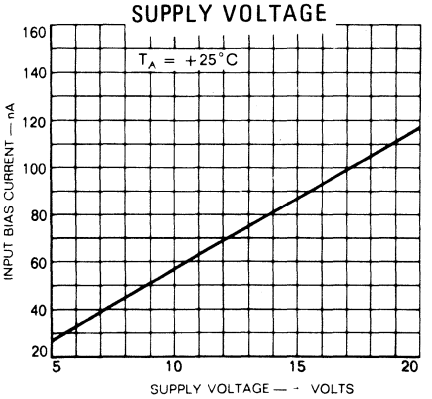
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE

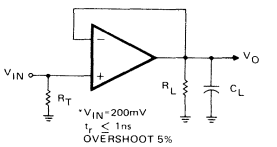


INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE

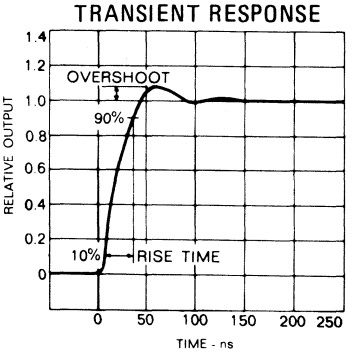


INPUT BIAS CURRENT VS. SUPPLY VOLTAGE



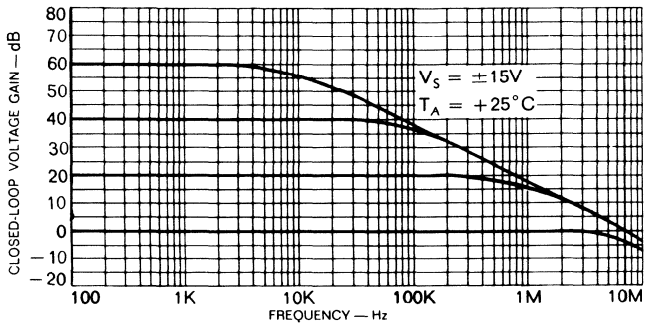


TRANSIENT RESPONSE

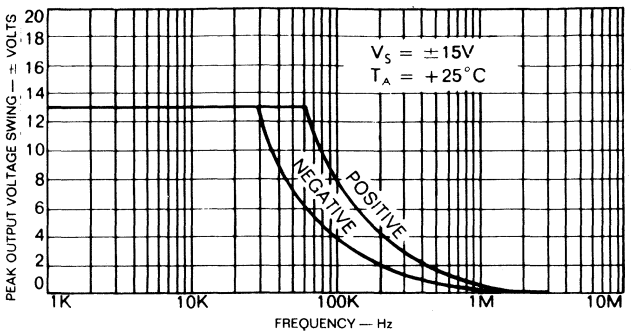


TYPICAL PERFORMANCE CURVES(continued)

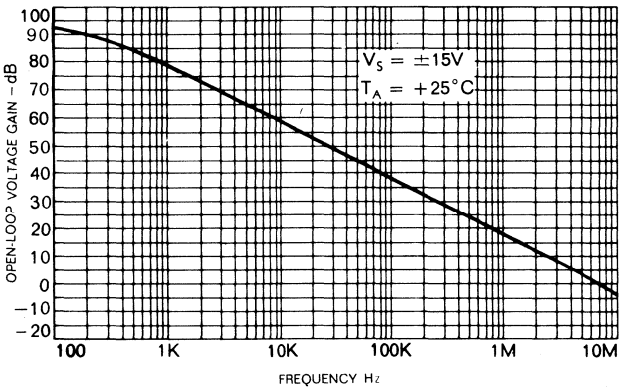
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING VS. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE



DEFINITIONS

Input Offset Voltage — That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

Input Offset Current — The difference in the currents into the two input terminals when the output is at zero voltage.

Input Bias Current — The average of the currents flowing into the input terminals when the output is at zero voltage.

Input Common Mode Voltage — The average referred to ground of the voltages at the two input terminals.

Common Mode Range — The range of voltages which if exceeded at either input terminal will cause the amplifier to cease operating.

Common Mode Rejection Ratio — The ratio of a specified range of input common mode voltage to the peak to peak change in input offset voltage over this range.

Output Voltage Swing — The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

Input Resistance — The ratio of the change in input voltage to the change in input current.

Output Resistance — The ratio of the change in output voltage to the change in output current.

Positive Output Voltage Swing — The peak positive output voltage swing, referred to ground, that can be obtained without clipping.

Negative Output Voltage Swing — The peak negative output voltage swing, referred to ground, that can be obtained without clipping.

Voltage Gain — The ratio of the change in output voltage to the change in input voltage producing it.

Bandwidth — The frequency at which the voltage gain is 3 dB below its low frequency value.

Unity Gain Bandwidth — The frequency at which the voltage gain of the amplifier is unity.

Power Supply Rejection Ratio — The ratio of the change in input offset voltage to the change in power supply voltage producing it.

Transient Response — The closed loop step function response of the amplifier under small signal conditions.

Phase Margin — $[180° - (\phi_1 - \phi_2)]$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unityo_2 is the phase shift at a frequency much lower than the open loop bandwidth.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2000/2005/2000A/2005A

F.E.T. Input Preamplifier

FEATURES

- CONVERTS ANY OP AMP OR COMPARATOR TO F.E.T. INPUT
- INPUT BIAS CURRENT: 1pA
- INPUT RESISTANCE: 10^{12} OHMS
- SLEW RATE: 100 V/μS
- BANDWIDTH: 10 MHz
- MEETS MIL-STD-883 REQUIREMENTS

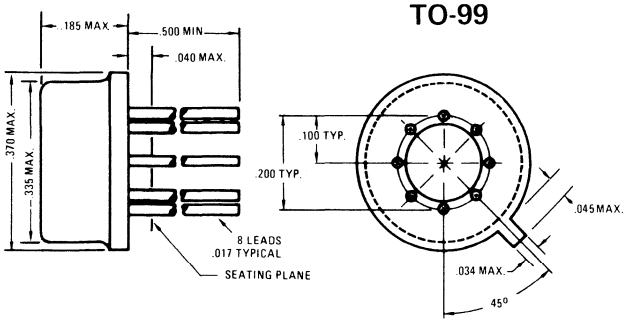
DESCRIPTION

The HA-2000/2005 is a monolithic unity gain differential amplifier stage with J.F.E.T. inputs and bipolar transistor outputs. It is intended for use as a preamplifier for operational amplifiers and comparators to produce high input resistance and low bias currents without sacrificing high speed performance. The circuit has a much wider common mode range than simple F.E.T. pairs, allowing op amps to be connected as voltage followers with full output swing. The circuit can also be used as a high impedance unity gain buffer for differential or two single-ended signals for frequencies from D.C. to R.F.

The HA-2000 is guaranteed for operation from -55°C to +125°C while the HA-2005 is guaranteed from 0°C to +75°C.

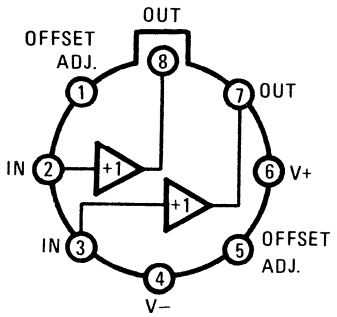
PACKAGES

TO-99



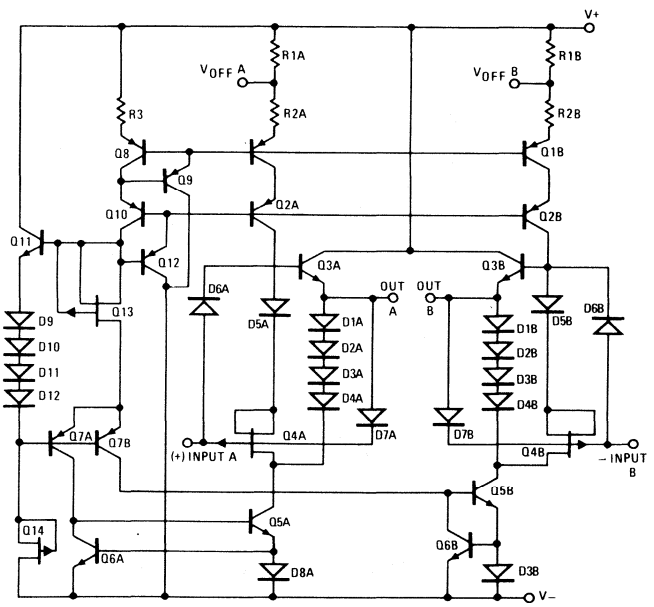
NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

PIN-OUT



(TOP VIEW)

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	35V	Internal Power Dissipation	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temp. Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2000)
Output Current	30mA		$0^oC \leq T_A \leq +75^oC$ (HA-2005)
		Storage Temp. Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

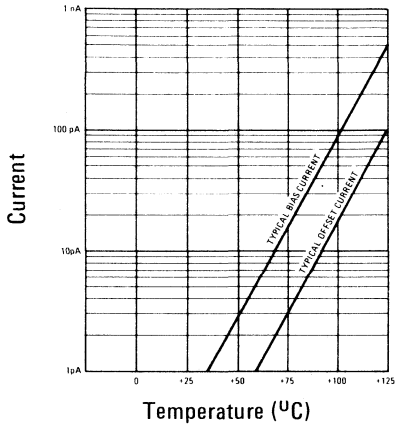
		HA-2000/HA-2000A			HA-2005/HA-2005A			
		−55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP.	MIN.	LIMITS TYP.	MAX.	MIN.	LIMITS TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 1)								
HA-2000 / HA-2005	+25°C		12	20		25	50	mV
	Full			25			55	mV
HA-2000A / HA-2005A	+25°C		5	10		5	10	mV
	Full			12			12	mV
Bias Current	+25°C		1	20		1	20	ρA
	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
	Full		0.1	5		.005	.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	.99	.999		.99	.999		V/V
	Full	.99			.99			V/V
Common Mode Rejection Ratio (Note 3)	Full	80	90		70	90		dB
-3dB Bandwidth	+25°C		10			10		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10			±10			V
Output Current Source	+25°C	+5			+5			mA
Sink	+25°C	-0.1			-0.1			mA
Output Common Mode Offset Voltage	Full			0.5			0.5	V
Full Power Bandwidth (Notes 4,5)	+25°C		1,000			1,000		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		50			50		ns
Overshoot (Notes 4,6)	+25°C		5			5		%
Slew Rate (Notes 4,5)	+25°C		100			100		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		0.7	1.7		0.7	1.7	mA
Power supply Rejection Ratio (Note 7)	Full	80	90		70	90		dB

NOTES:
1. Adjustable to 0 with 100KΩ pot between pins 1 and 5 wiper to V+
2. R_L = 1M
3. $V_{CM} = \pm 5.0V$
4. R_L = 10K to V−
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. V_S = +9V to +15V

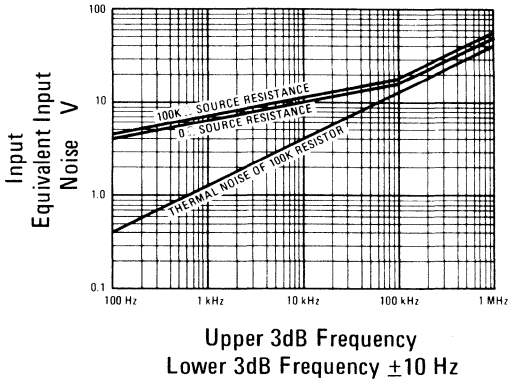
PERFORMANCE CURVES

V+ = 15 VDC, V– = 15 VDC, T_A = 25°C UNLESS OTHERWISE STATED.

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

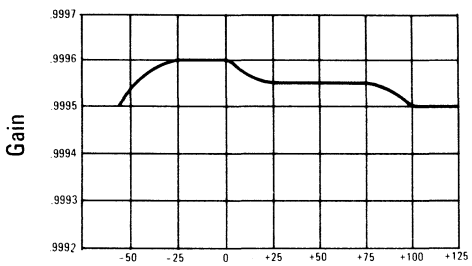


EQUIVALENT INPUT NOISE VS. BANDWIDTH

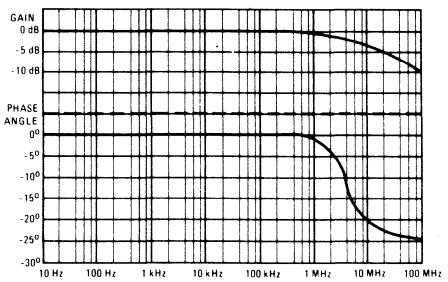


Upper 3dB Frequency
Lower 3dB Frequency ±10 Hz

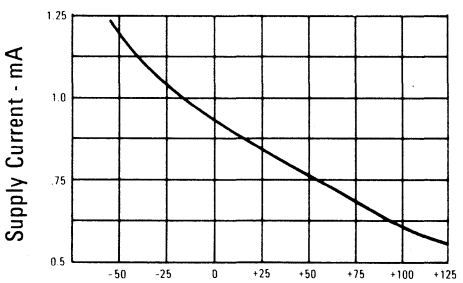
D.C. GAIN VS. TEMPERATURE



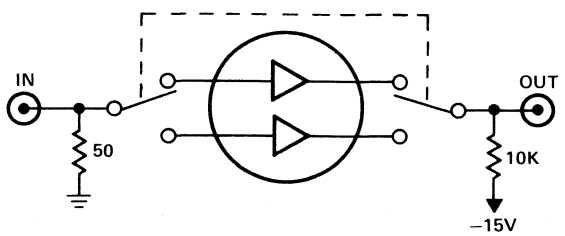
GAIN, PHASE ANGLE VS. FREQUENCY



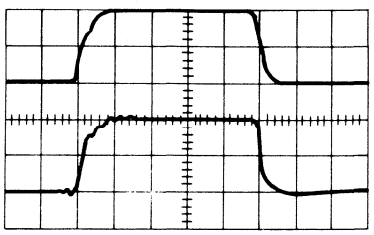
POWER SUPPLY CURRENT VS. TEMPERATURE



TRANSIENT RESPONSE, SLEW RATE TEST HOOK-UP



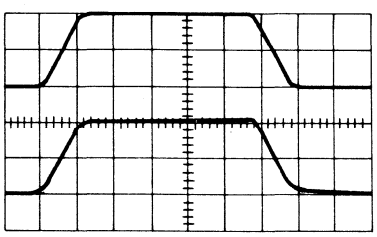
TYP. TRANSIENT RESPONSE WAVEFORM



Typical Transient Response Waveforms

Upper Trace: Input
Lower Trace: Output
Vertical Scale: 100mV/Div.
Horizontal Scale: 100ns/Div.

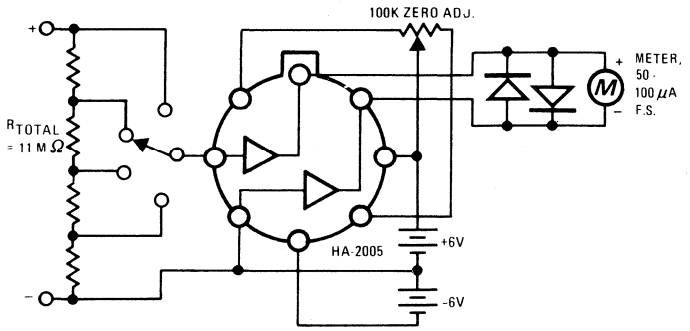
TYP. SLEWING RESPONSE WAVEFORM



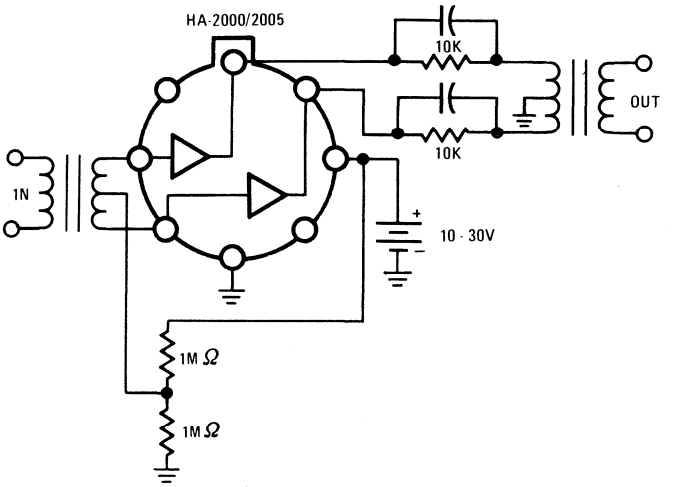
Typical Slewing Response Waveforms

Upper Trace: Input
Lower Trace: Output
Vertical Scale: 5V/Div.
Horizontal Scale: 100ns/Div.

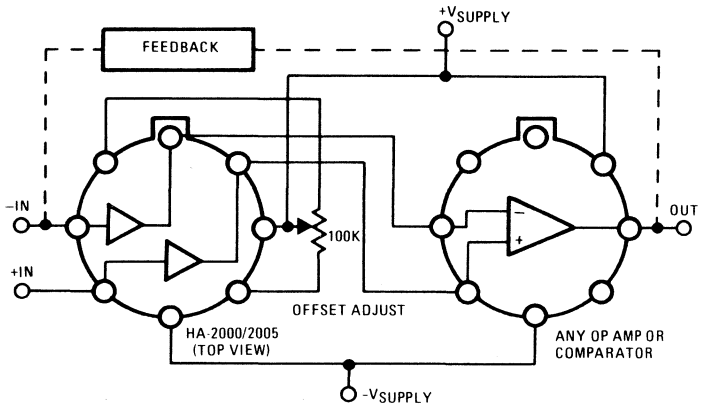
TYPICAL APPLICATIONS



F.E.T. VOLTMETER



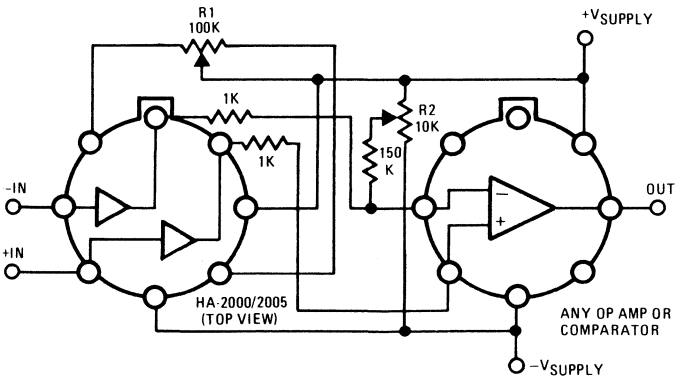
BALANCED LINE AMPLIFIER FOR AUDIO TO 100MHz SIGNALS



HOOKUP TO CREATE F.E.T. INPUT OP AMP OR COMPARATOR

ALTERNATE HOOKUP TO ADJUST FOR MINIMUM OFFSET VOLTAGE TEMPERATURE COEFFICIENT

Adjust R_1 to point of minimum offset voltage change over temperature range. Adjust R_2 to zero offset voltage. Drifts of less than 10 μV/o_C can typically be achieved.



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2050/2055/2050A/2055A

High Slew Rate F.E.T. Input Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 400ns
- WIDE POWER BANDWIDTH — 2 MHz
- HIGH GAIN BANDWIDTH — 20 MHz
- HIGH INPUT IMPEDANCE — 10^{12} OHMS
- LOW BIAS CURRENT — 1 pA
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING
- MEETS MIL-STD-883 REQUIREMENTS

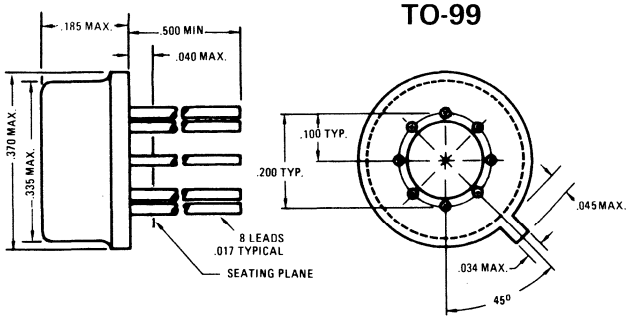
DESCRIPTION

The HA-2050/2055 is an operational amplifier combining the advantages of very high slew rate and wide bandwidth with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The device may be operated inverting or non-inverting; and external compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2050 is guaranteed for operation from -55°C to +125°C and the HA-2055 is guaranteed from 0°C to +75°C.

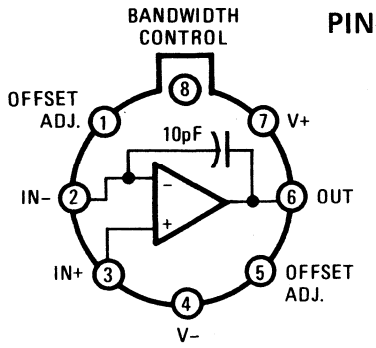
PACKAGE

TO-99



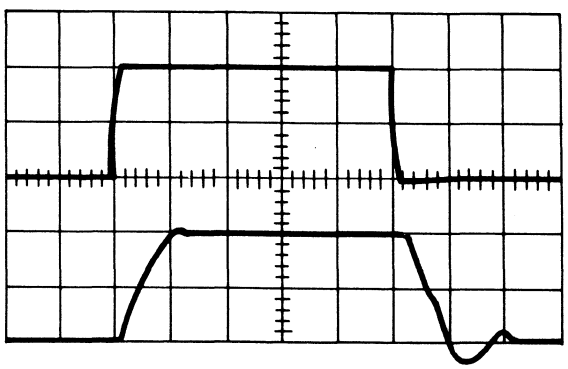
NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

PIN-OUT



(TOP VIEW)

SLEWING WAVEFORM



Horizontal Scale: 100ns/Div.
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5.0V/Div.
Gain = +3, R_L = 2K Ohms, C_L = 50pF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	35.0V	Internal Power Dissipation	300mW	
Differential Input Voltage	±15.0V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2050)
Output Current	50mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2055)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

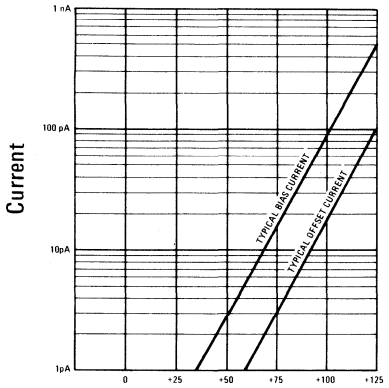
		HA-2050/HA-2050A $-55^{o}C$ to $+125^{o}C$			HA-2055/HA-2055A $0^{o}C$ to $+75^{o}C$			
		LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 1)								
HA-2050 / HA-2055	+25°C		15	25		30	60	mV
	Full			30			65	mV
HA-2050A / HA-2055A	+25°C		7	14		7	14	mV
	Full			17			17	mV
Bias Current	+25°C		1	20		1	20	pA
	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	pA
	Full		0.1	5		.005	0.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		pF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	7.5K	15K		7.5K	15K		V/V
	Full	5K			5K			V/V
Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		20			20		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
Output Current	+25°C	±10	±20		±10	±20		mA
Full Power Bandwidth (Note 5)	+25°C		2,000			2,000		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		25			25		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		120			120		V/μs
Settling Time	+25°C		0.4			0.4		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		6.0	8.0		6.0	8.0	mA
Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. $C_L = 50pF$
9. $A_V = +3$, See transient response test circuit and wave forms, page 4.

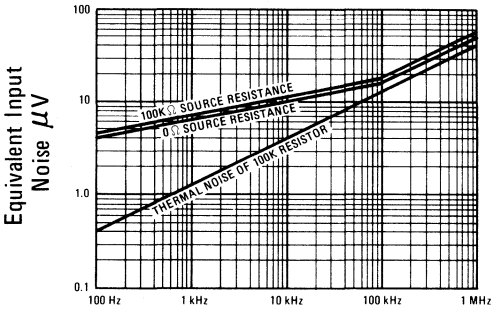
PERFORMANCE CURVES

V+ = 15 VDC, V- = 15 VDC, T_A = 25°C UNLESS OTHERWISE STATED.

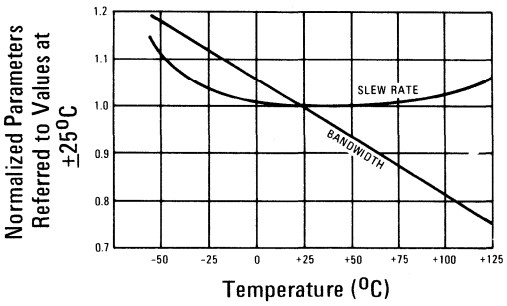
INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



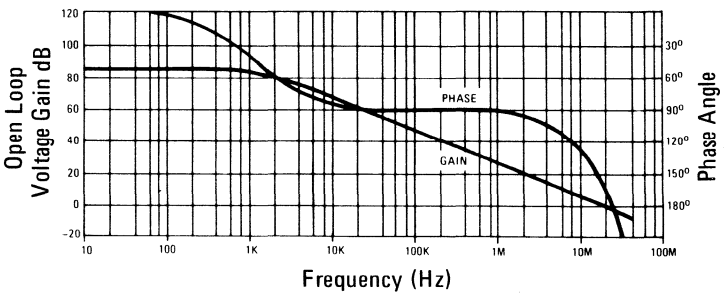
EQUIVALENT INPUT NOISE VS. BANDWIDTH



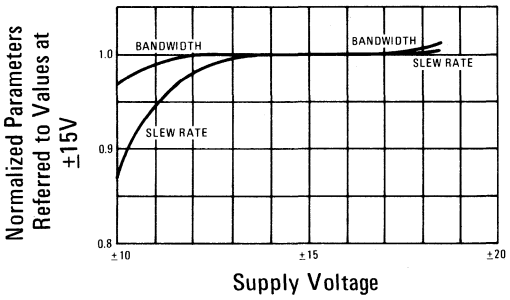
NORMALIZED AC PARAMETERS VS. TEMPERATURE



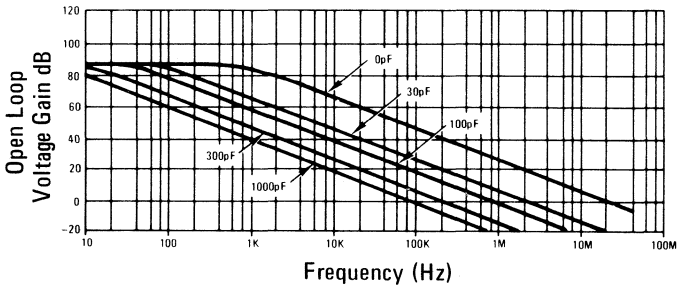
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



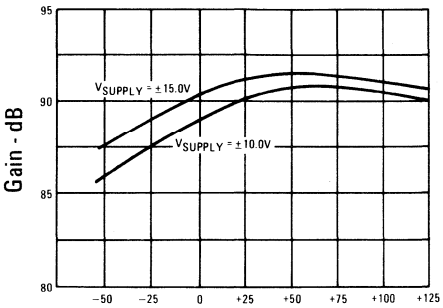
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



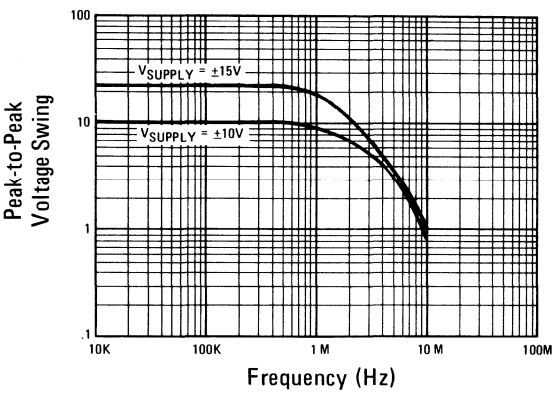
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

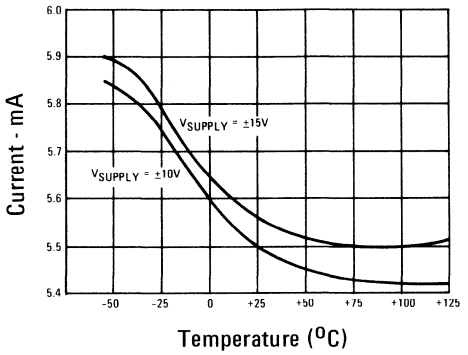


OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C

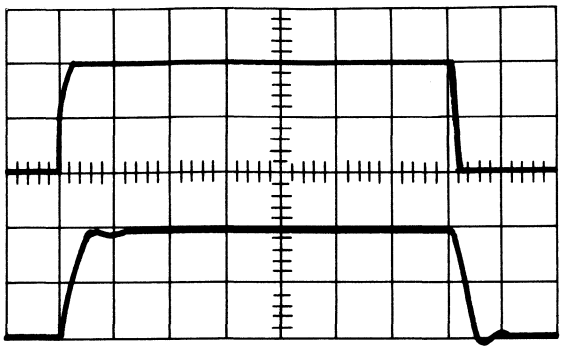


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT VS. TEMPERATURE

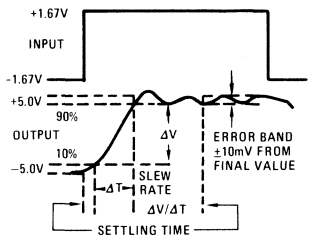


TRANSIENT RESPONSE; A_V = +3

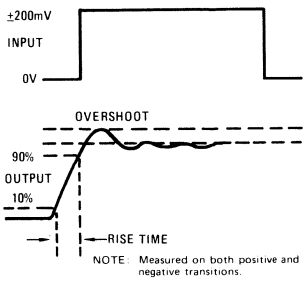


R_L = 2K Ohms, C_L = 50pF
Upper Trace: Input; 33mV/Div.
Lower Trace: Output; 100mV/Div.
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

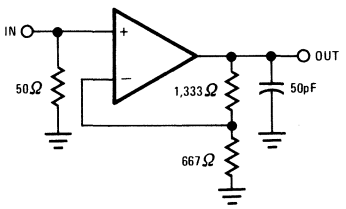
SLEW RATE AND SETTLING TIME



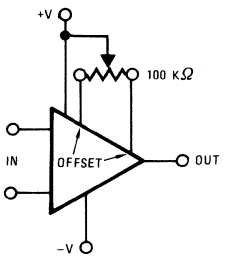
TRANSIENT RESPONSE



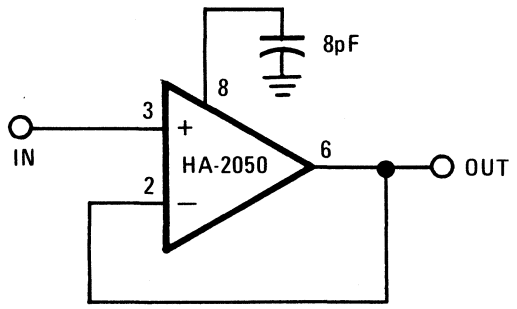
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

Slew Rate ≈ 40V/μs

Bandwidth ≈ 8 MHz

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2060/2065/ 2060A/2065A

Wide Band F.E.T. Input Operational Amplifier

LINEAR DATA

FEATURES

- GAIN BANDWIDTH PRODUCT 100 MHz
- HIGH INPUT IMPEDANCE 10^{12} OHMS
- LOW BIAS CURRENT 1 pA
- HIGH SLEW RATE 35V/μs
- WIDE POWER BANDWIDTH 600 kHz
- TRUE OP AMP - CAN BE OPERATED INVERTING OR NON-INVERTING
- MEETS MIL-STD-883 REQUIREMENTS

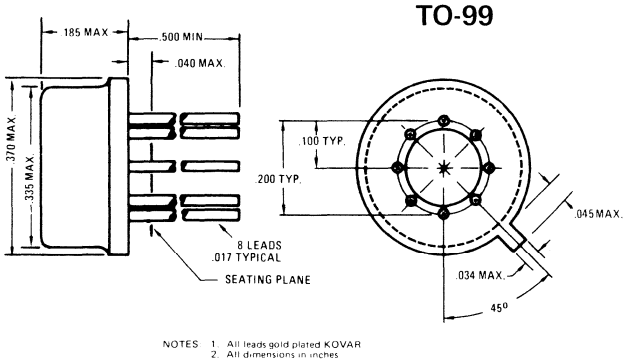
DESCRIPTION

The HA-2060/2065 is an operational amplifier combining the advantages of very wide bandwidth and high slew rate with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, active filters, wide band amplifiers, high gain amplifiers with superior bandwidth, and wherever very low closed loop gain and phase shift errors are required. The device may be operated inverting or non-inverting; and external compensation is required only when operated at closed loop gains less than five. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2060 is guaranteed for operation from -55°C to +125°C and the HA-2065 is guaranteed from 0°C to +75°C.

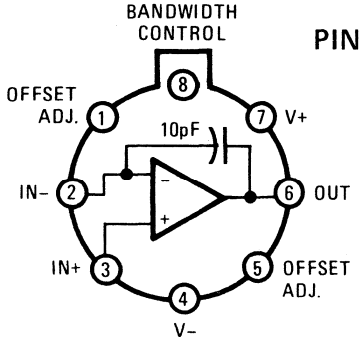
PACKAGE

TO-99



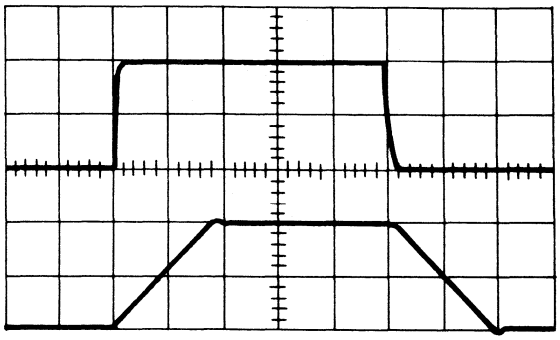
NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

PIN-OUT



(TOP VIEW)

SLEWING WAVEFORM



Horizontal Scale: 200ns/Div.
Upper Trace: Input; 1.0V/Div.
Lower Trace: Output; 5.0V/Div.
Gain = +5, R_L = 2K Ohms, C_L = 50pF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 35.0V
Differential Input Voltage ±12V
Output Current / Full Short Circuit Protection

Internal Power Dissipation 300mW
Operating Temp. Range $-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2060)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2065)
Storage Temp. Range $-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

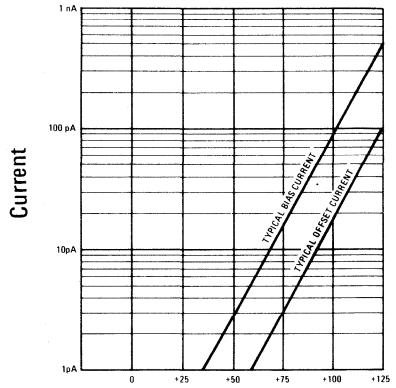
PARAMETER	TEMP.	HA-2060/HA-2060A -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2065/HA-2065A 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 1)								
HA-2060 / HA-2065	+25°C		15	25		15	60	mV
	Full			30			65	mV
HA-2060A / HA-2065A	+25°C		7	12		7	12	mV
	Full			15			15	mV
Bias Current	+25°C		1	20		1	20	ρA
	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
	Full		0.1	5		.005	.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	80K	150K		80K	150K		V/V
	Full	60K			70K			V/V
Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		100			100		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
Output Current	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 5)	+25°C		600			600		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		17			17		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		35			35		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.0	6.0		4.0	6.0	mA
Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. $V = \pm 5.0V$
8. $C_L = 50\rho F$
9. $A_V = +5$, See transient response test circuits and waveforms, page 4.

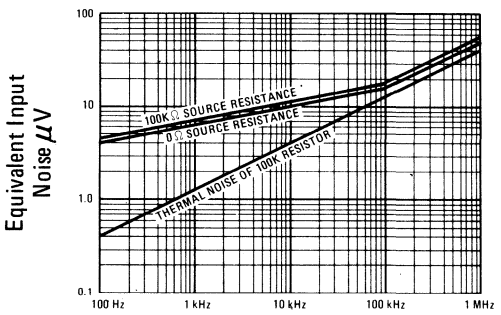
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

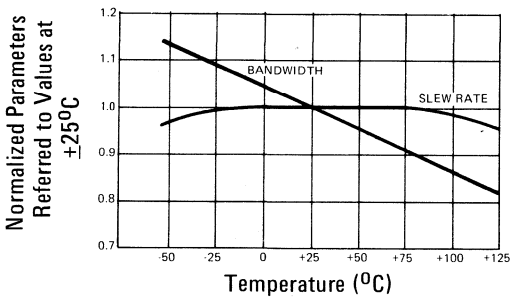


EQUIVALENT INPUT NOISE VS. BANDWIDTH

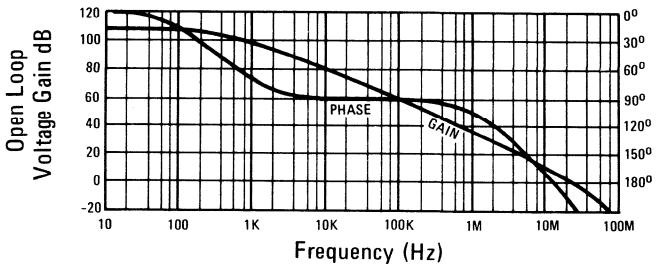


Upper 3dB Frequency
Lower 3dB Frequency - 10 Hz

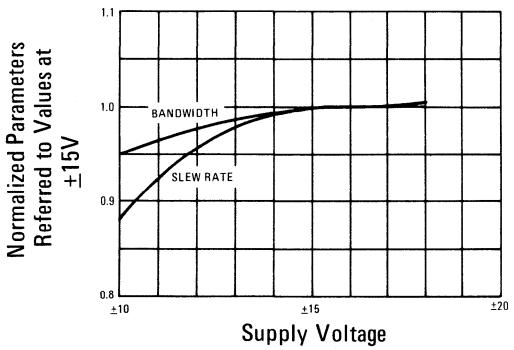
NORMALIZED AC PARAMETERS VS. TEMPERATURE



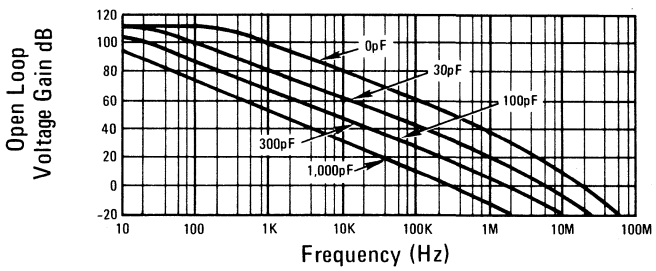
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



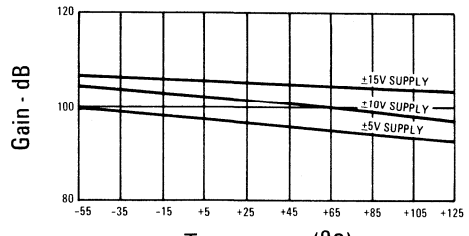
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



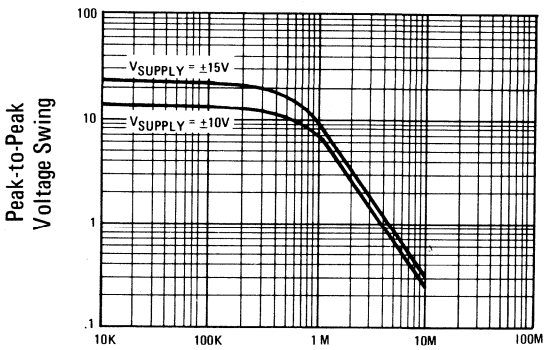
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

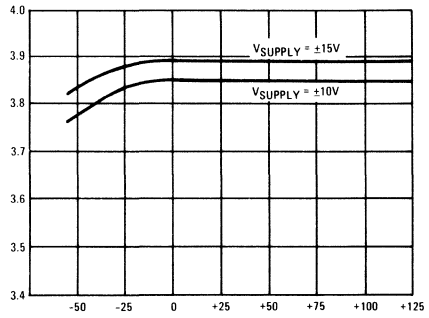


OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C

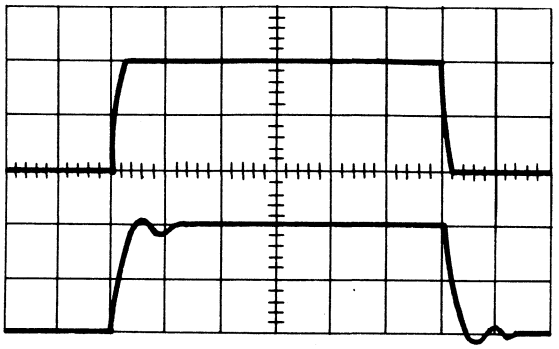


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT VS. TEMPERATURE

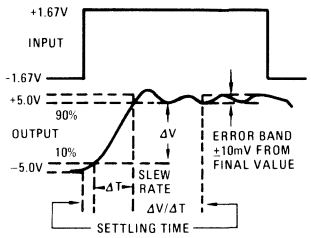


TRANSIENT RESPONSE; A_V= +5

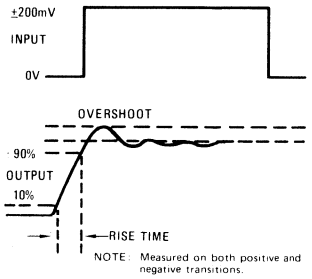


R_L = 2K Ohms, C_L = 50pF
Upper Trace: Input; 20mV/Div.
Lower Trace: Output; 100mV/Div.
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

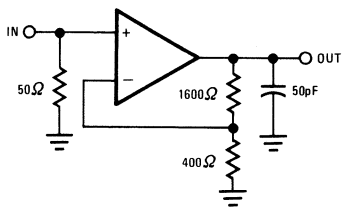
SLEW RATE AND SETTLING TIME



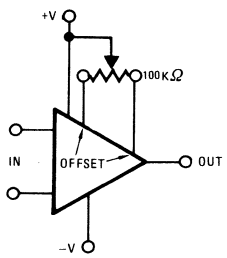
TRANSIENT RESPONSE



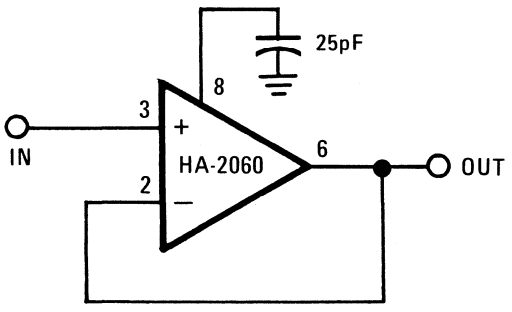
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

SLEW RATE ≈ 5 V/μs

BANDWIDTH ≈ 10 MHz

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2101

Operational Amplifier

LINEAR DATA

FEATURES

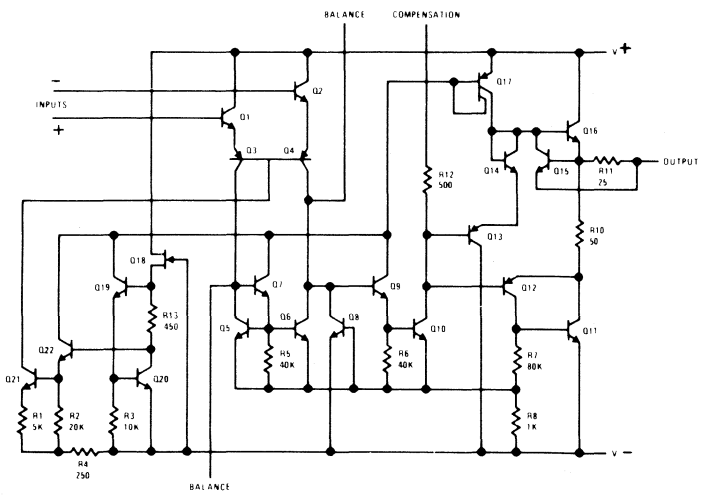
- FREQUENCY COMPENSATION WITH A SINGLE 30pF CAPACITOR
- OPERATION FROM ±5.0V TO ±20.0V SUPPLIES
- CONTINUOUS SHORT CIRCUIT PROTECTION
- LOW CURRENT DRAIN – 1.8mA AT ±20.0V

GENERAL DESCRIPTION

The HA-2101 is a general purpose operational amplifier which can be compensated for unity gian stability with a single 30pF capacitor.

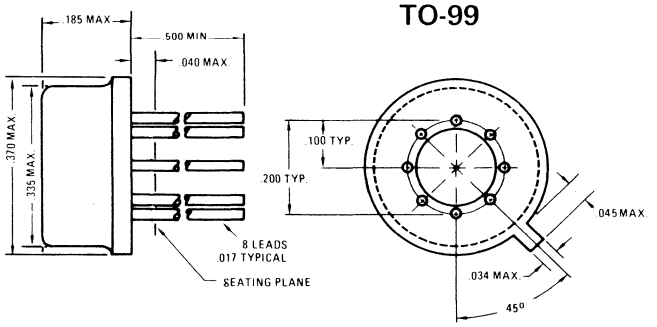
This amplifier has input and output overload protection. Large common mode signals do not cause latch-up. The HA-2101 has a guaranteed operating temperature of −55°C to +125°C.

SCHEMATIC

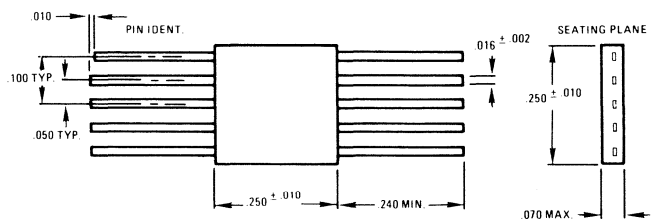


PACKAGES

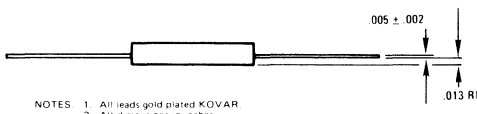
TO-99



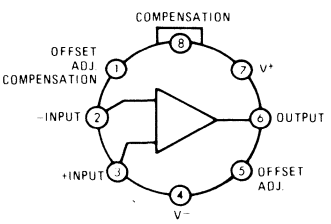
NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



TO-91

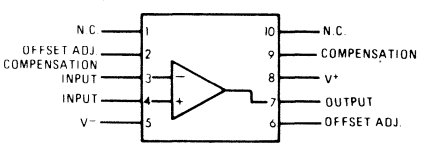


NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



TO-99

TO-91



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.0V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30.0V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 Seconds)	300°C

ELECTRICAL CHARACTERISTICS

PARAMETER	TEMPERATURE	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		1.0	5.0	mV
	−55°C to +125°C			6.0	mV
Average Offset Voltage Temperature Coefficient	−55°C to +125°C		6.0		μV/°C
Bias Current	+25°C		120	500	nA
	−55°C to +125°C		0.28	1.5	μA
Offset Current	+25°C		40	200	nA
	−55°C to +125°C		100	500	nA
Input Resistance	+25°C	300	800		KΩ
Input Voltage Range (Note 6)	−55°C to +125°C	±12.0			V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 5 & 6)	+25°C	50K	160K		V/V
	−55°C to +125°C	25K			V/V
Common Mode Rejection Ratio	−55°C to +125°C	70	90		dB
Output Voltage Swing					
R_L = 10KΩ (Note 6)	−55°C to +125°C	12.0	14.0		V
R_L = 2KΩ (Note 6)	−55°C to +125°C	10.0	13.0		V
POWER SUPPLY CHARACTERISTICS					
Supply Current (Note 4)	+25°C		1.8	3.0	mA
	+125°C		1.2	2.5	mA
Supply Voltage Rejection Ratio	−55°C to +125°C	70	90		dB

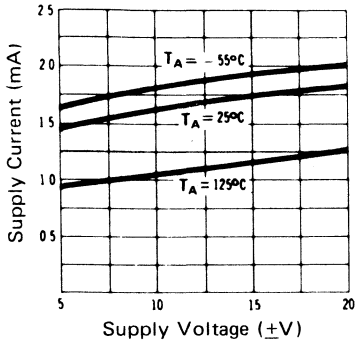
NOTES:

1. Derate TO-99 package at 6.8mW/°C for operation ambient temperature above 75°C and 4.9mW/°C above 50°C for the TO-91 package.
2. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
3. These specifications apply for $\pm 5.0V \leq V_S \leq +20.0V$ and $-55°C \leq T_A \leq +125°C$ unless otherwise specified.
4. $V_S = \pm 20.0V$
5. $R_L = 2K\Omega$, $V_{OUT} = \pm 10.0V$
6. $V_S = \pm 15.0V$

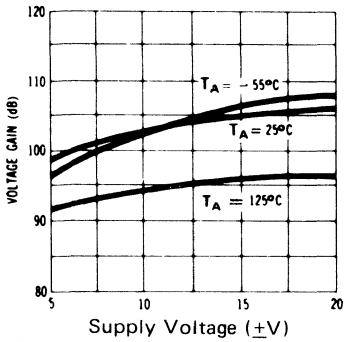
PERFORMANCE CURVES

TYPICAL

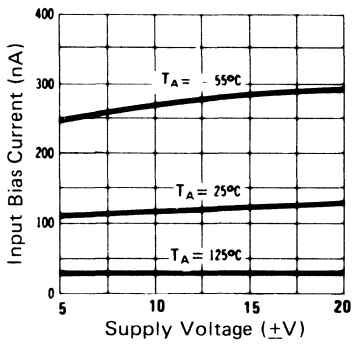
SUPPLY CURRENT



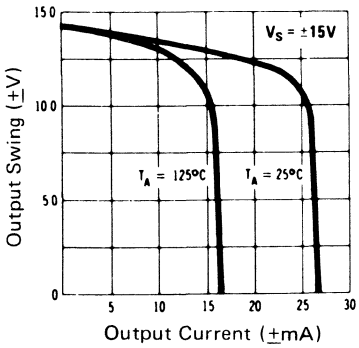
VOLTAGE GAIN



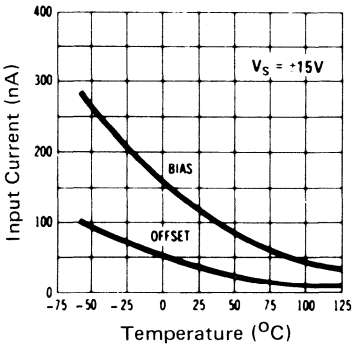
INPUT BIAS CURRENT



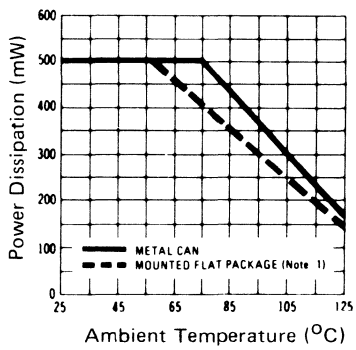
CURRENT LIMITING



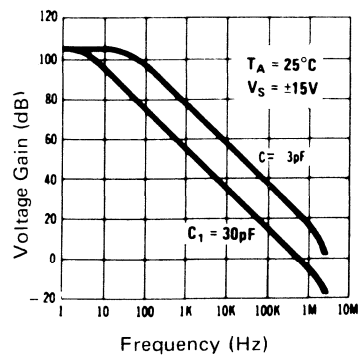
INPUT CURRENT



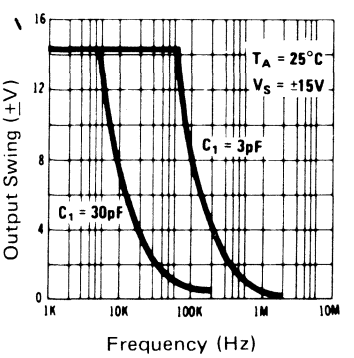
MAXIMUM POWER DISSIPATION



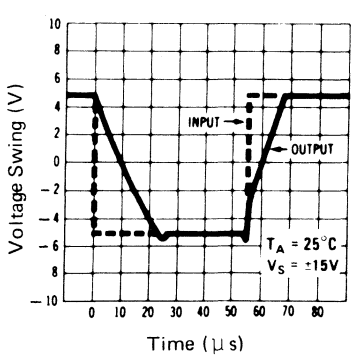
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



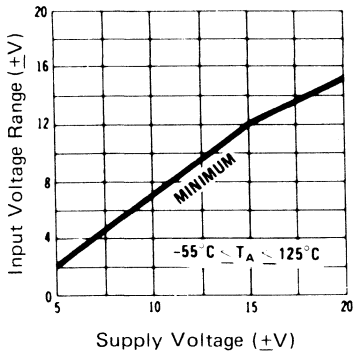
VOLTAGE FOLLOWER PULSE RESPONSE



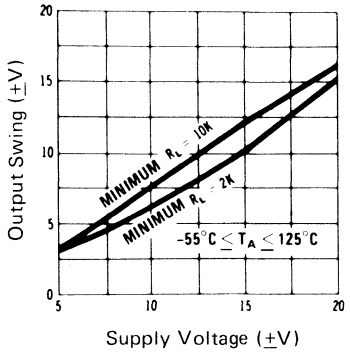
PERFORMANCE CURVES(continued)

GUARANTEED

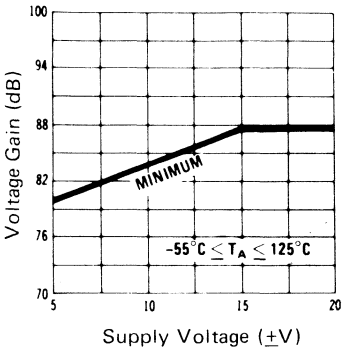
INPUT VOLTAGE RANGE



OUTPUT SWING

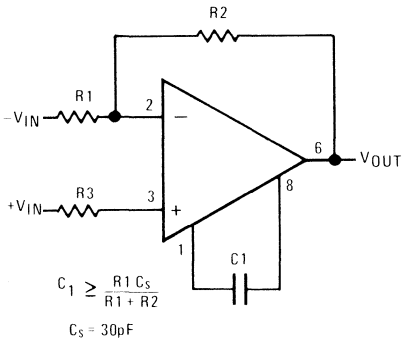


VOLTAGE GAIN

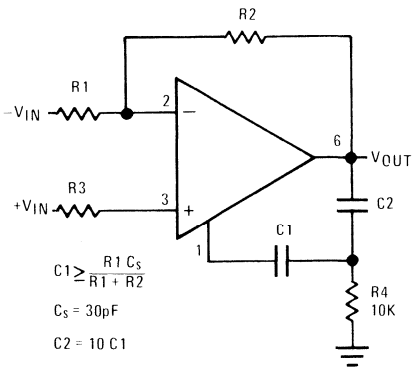


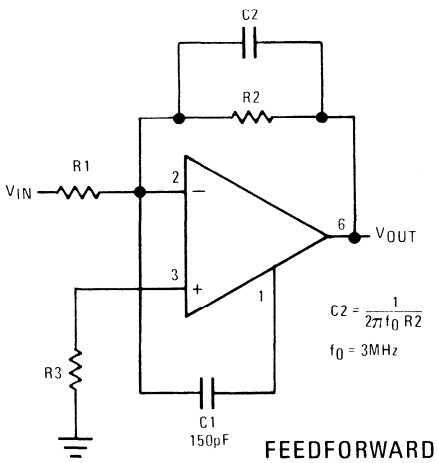
APPLICATION INFORMATION

SINGLE POLE COMPENSATION



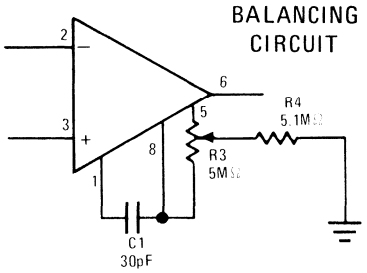
TWO POLE COMPENSATION

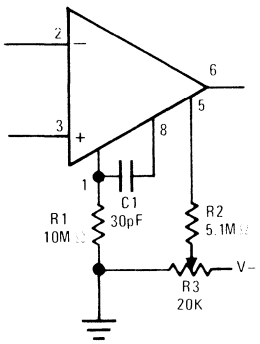




FEEDFORWARD COMPENSATION

BALANCING CIRCUIT





ALTERNATE BALANCING CIRCUIT

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2101A/2201A

Operational Amplifiers

LINEAR DATA

FEATURES

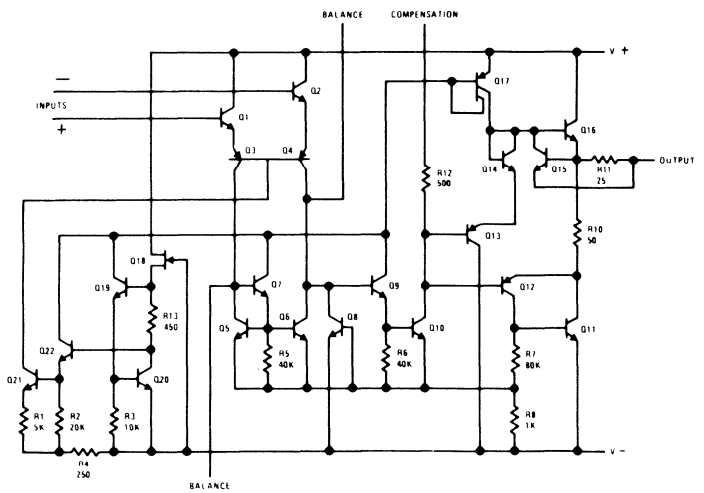
- LOW OFFSET VOLTAGE OVER TEMPERATURE — 3mV MAXIMUM
- LOW BIAS CURRENT OVER TEMPERATURE — 100nA MAXIMUM
- LOW OFFSET CURRENT OVER TEMPERATURE — 20nA MAXIMUM
- LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT — 3μV/°C

GENERAL DESCRIPTION

The HA-2101A and HA-2201A are high performance general purpose operational amplifiers which can be compensated for unity gain stability with a single 30pF capacitor.

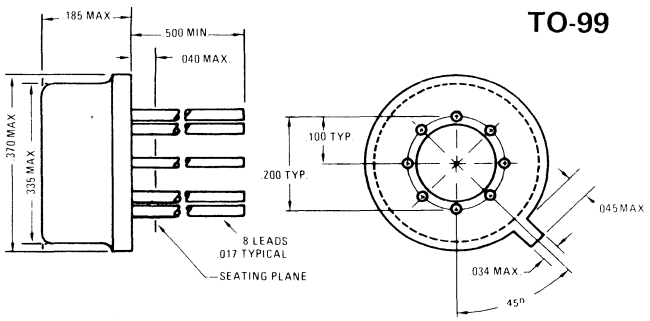
These amplifiers have input and output overload protection. Large common mode signals do not cause latch-up. The HA-2101A and HA-2201A have guaranteed operating temperature ranges of −55°C to +125°C and −25°C to +85°C respectively.

SCHEMATIC

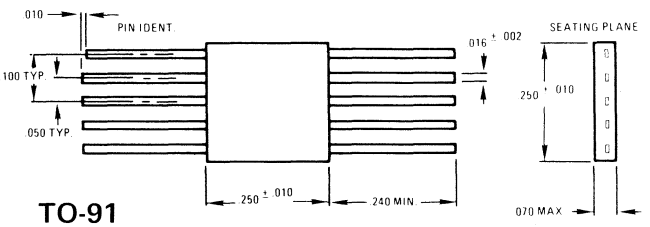


PACKAGE

TO-99

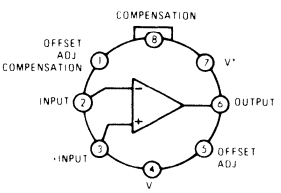


NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



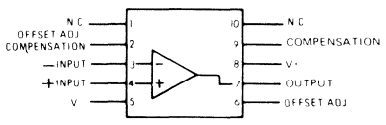
TO-91

NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



TO-99

TO-91



Note:
V- connected to case

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.0V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30.0V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration	Indefinite
Operating Temperature Range – HA-2101A	−55°C to +125°C
HA-2201A	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 Seconds)	300°C

ELECTRICAL CHARACTERISTICS

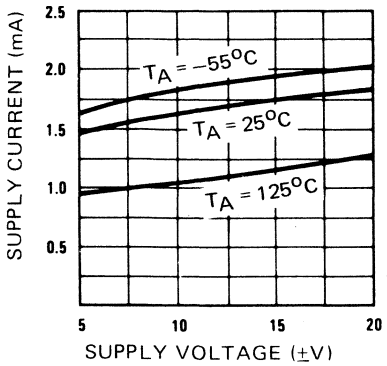
PARAMETER	TEMPERATURE (Note 7)	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C Full		0.7	2.0 3.0	mV mV
Average Offset Voltage Temperature Coefficient	Full		3.0	15	μV/°C
Bias Current	+25°C Full		30	75 100	nA nA
Offset Current	+25°C Full		1.5	10 20	nA nA
Offset Current Temperature Coefficient	T_{Low} to +25°C +25°C to T_{High}		0.02 0.01	0.2 0.1	nA/°C nA/°C
Input Resistance	+25°C	1.5	4		MΩ
Input Voltage Range (Note 4)	Full	±15.0			V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 5 & 6)	+25°C Full	50K 25K	160K		V/V V/V
Common Mode Rejection Ratio	Full	80	96		dB
Output Voltage Swing R_L = 10KΩ (Note 6) R_L = 2KΩ	 Full Full	 12.0 10.0	 14.0 13.0		 V V
POWER SUPPLY CHARACTERISTICS					
Supply Current (Note 4)	+25°C +125°C		1.8 1.2	3.0 2.5	mA mA
Supply Voltage Rejection Ratio	Full	80	96		dB

NOTES:
1. Derate TO-99 package at 6.8mW/°C for operation ambient temperature above 75°C and 4.9mW/°C above 50°C for the TO-91 package.
2. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
3. These specifications apply for $\pm 5.0V \leq V_S \leq +20.0V$ and C_1=30pF unless otherwise specified.
4. $V_S = \pm 20.0V$
5. $R_L = 2K\Omega$, $V_{OUT} = \pm 10.0V$
6. $V_S = \pm 15.0V$
7. Full = T_{Low} to T_{High} = −55°C to +125°C (HA-2101A)
= −25°C to +85°C (HA-2201A)

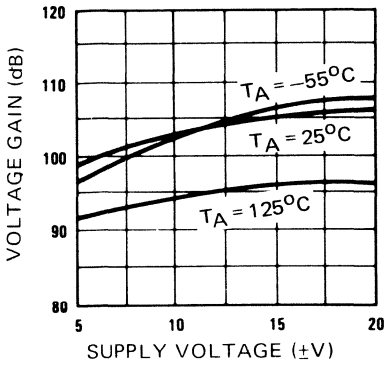
PERFORMANCE CURVES

TYPICAL

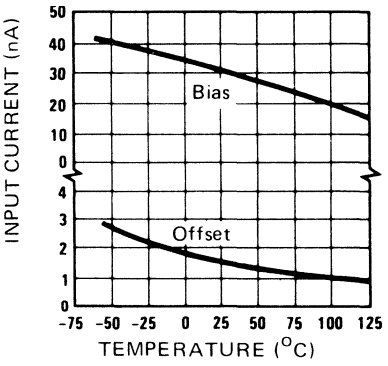
SUPPLY CURRENT



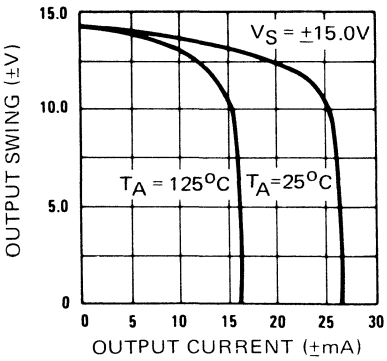
VOLTAGE GAIN



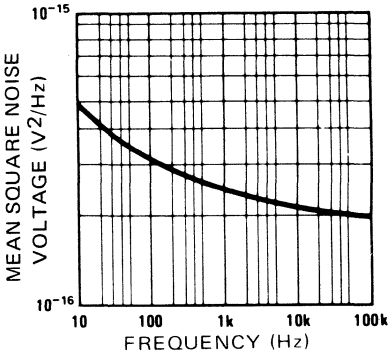
INPUT CURRENT



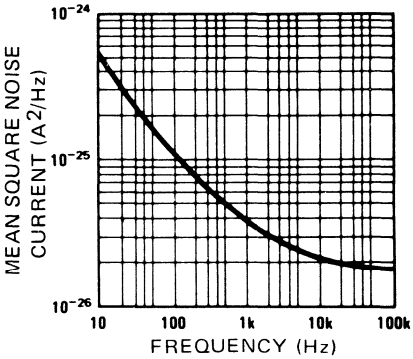
CURRENT LIMITING



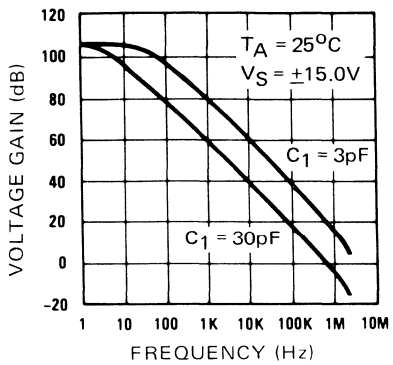
INPUT NOISE VOLTAGE



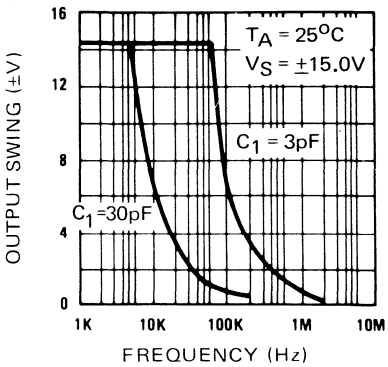
INPUT NOISE CURRENT



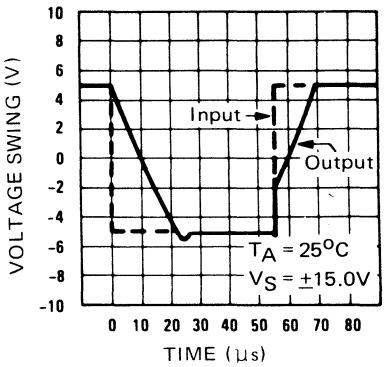
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



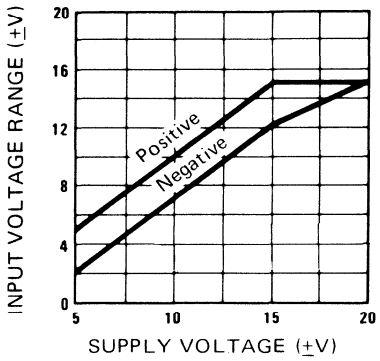
VOLTAGE FOLLOWER PULSE RESPONSE



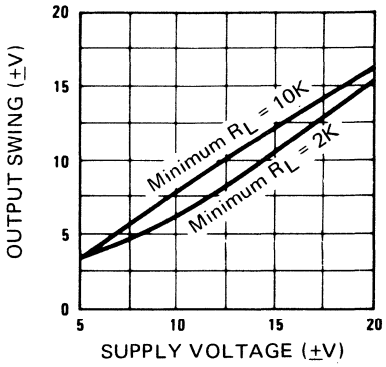
PERFORMANCE CURVES (continued)

GUARANTEED
full operating temperature range (HA-2101A: −55°C to +125°C; HA-2201A: −25°C to +85°C)

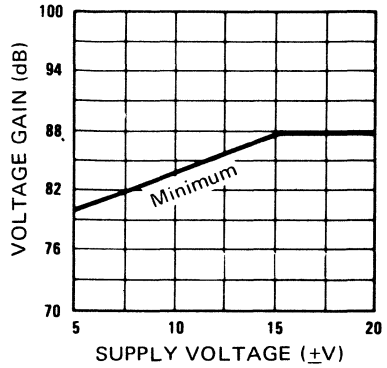
INPUT VOLTAGE RANGE



OUTPUT SWING

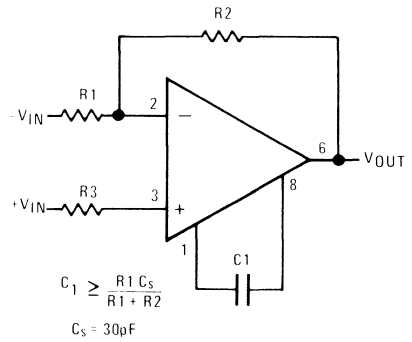


VOLTAGE GAIN

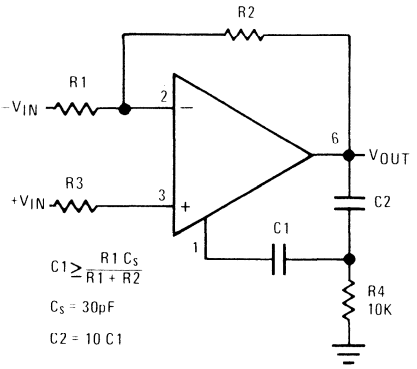


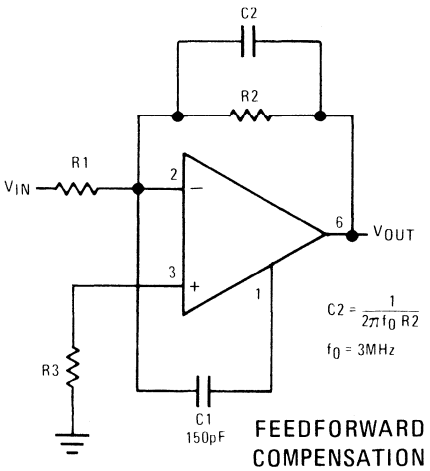
APPLICATION INFORMATION

SINGLE POLE COMPENSATION



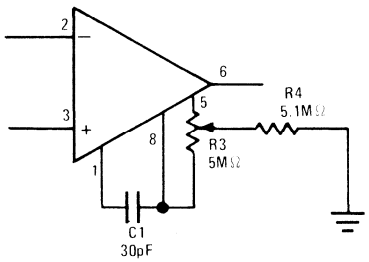
TWO POLE COMPENSATION



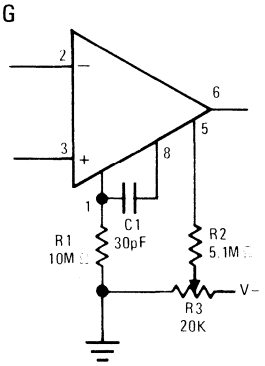


FEEDFORWARD COMPENSATION

BALANCING CIRCUIT



ALTERNATE BALANCING CIRCUIT



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2107/2207

Operational Amplifiers

LINEAR DATA

FEATURES

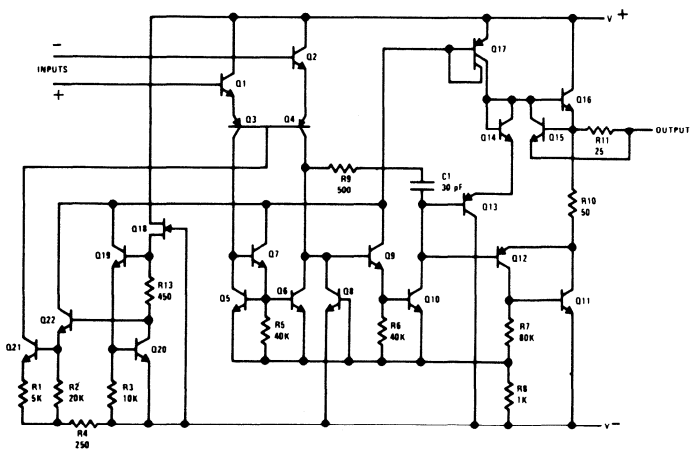
- LOW OFFSET VOLTAGE OVER TEMPERATURE — 3mV MAXIMUM
- LOW BIAS CURRENT OVER TEMPERATURE — 100nA MAXIMUM
- LOW OFFSET CURRENT OVER TEMPERATURE — 20nA MAXIMUM
- LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT — 3μV/^{o}C

GENERAL DESCRIPTION

The HA-2107 and HA-2207 are high performance general purpose operational amplifiers which are internally compensated for unity gain stability.

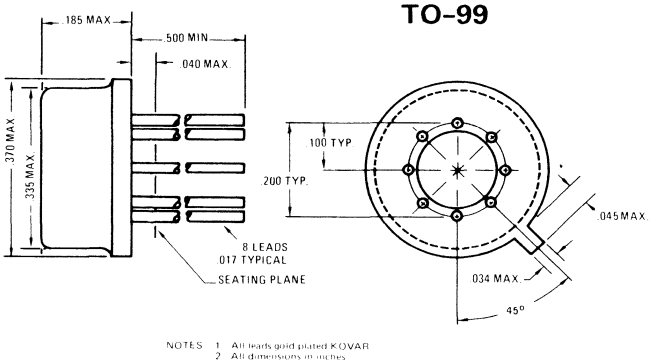
These amplifiers have input and output overload protection. Large common mode signals do not cause latch-up. The HA-2107 and HA-2207 have guaranteed operating temperature ranges of −55^{o}C to +125^{o}C and −25^{o}C to +85^{o}C respectively.

SCHEMATIC

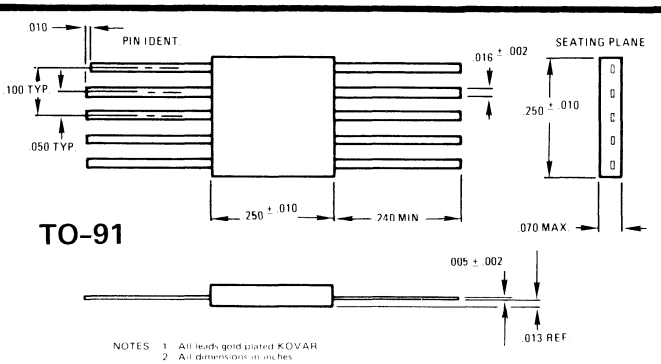


PACKAGES

TO-99

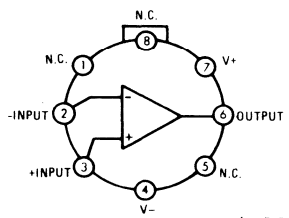


NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



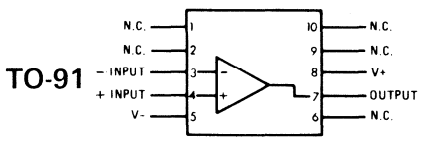
TO-91

NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches



TO-99

(TOP VIEW)



TO-91

Note:
V- connected to case

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.0V	Operating Temperature Range	
Power Dissipation (Note 1)	500mW	HA-2107	−55°C to +125°C
Differential Input Voltage	±30.0V	HA-2207	−25°C to +85°C
Input Voltage (Note 2)	±15.0V	Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration	Indefinite	Lead Temperature (Soldering 60 seconds)	300°C

ELECTRICAL CHARACTERISTICS

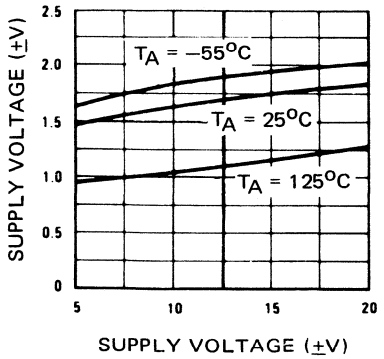
PARAMETER	TEMPERATURE (Note 7)	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		0.7	2.0	mV
	Full			3.0	mV
Average Offset Voltage Temperature Coefficient	Full		3.0	15	µV/°C
Bias Current	+25°C		30	75	nA
	Full			100	nA
Offset Current	+25°C		1.5	10	nA
	Full			20	nA
Offset Current Temperature Coefficient	T_{Low} to +25°C		0.02	0.2	nA/°C
	+25°C to T_{High}		0.01	0.1	nA/°C
Input Resistance	+25°C	1.5	4		MΩ
Input Voltage Range (Note 4)	Full	±15.0			V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 5 & 6)	+25°C	50K	160K		V/V
	Full	25K			V/V
Common Mode Rejection Ratio	Full	80	96		dB
Output Voltage Swing					
R_L = 10KΩ (Note 6)	Full	12.0	14.0		V
R_L = 2KΩ (Note 6)	Full	10.0	13.0		V
POWER SUPPLY CHARACTERISTICS					
Supply Current (Note 4)	+25°C		1.8	3.0	mA
	125°C		1.2	2.5	mA
Supply Voltage Rejection Ratio	Full	80	96		dB

NOTES:
1. Derate TO-99 package at 6.8mW/°C for operation ambient temperature above 75°C and 4.9mW/°C above 50°C for the TO-91 package.
2. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
3. These specifications apply for $\pm 5.0V \leq V_S \leq +20.0V$ unless otherwise specified.
4. $V_S = \pm 20.0V$
5. $R_L = 2K\Omega$, $V_{OUT} = \pm 10.0V$
6. $V_S = \pm 15.0V$
7. Full = T_{Low} to T_{High} = −55°C to +125°C (HA-2107)
   −25°C to +85°C (HA-2207)

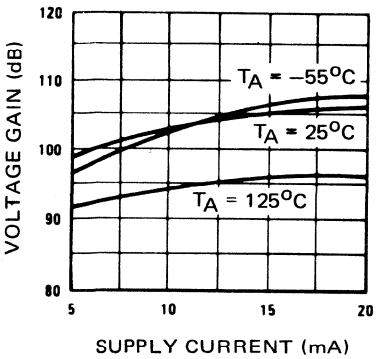
PERFORMANCE CURVES

TYPICAL

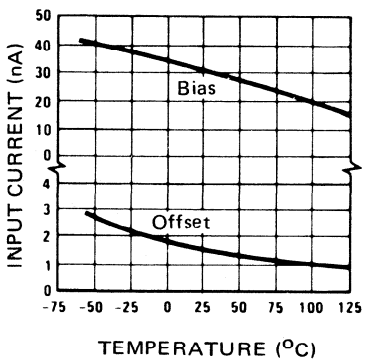
SUPPLY CURRENT



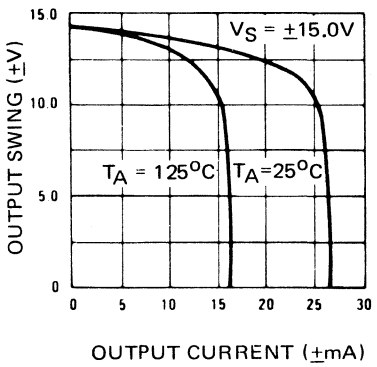
VOLTAGE GAIN



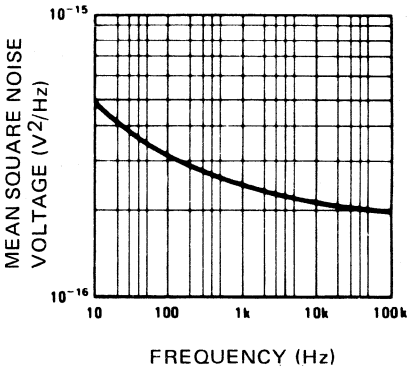
INPUT CURRENT



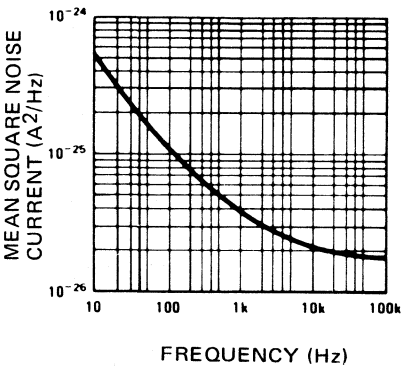
CURRENT LIMITING



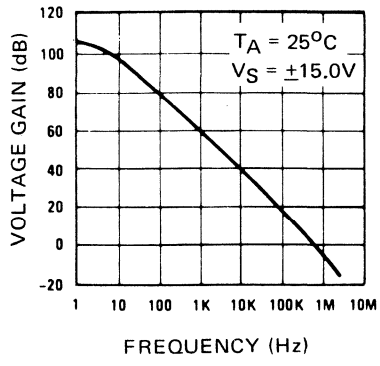
INPUT NOISE VOLTAGE



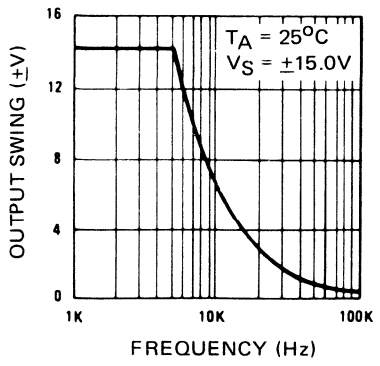
INPUT NOISE CURRENT



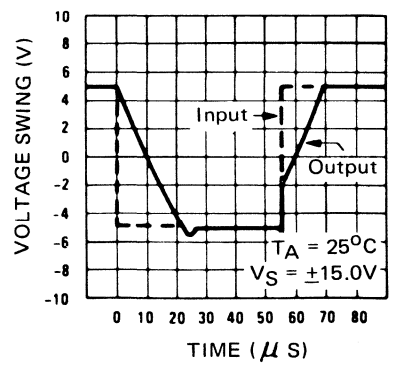
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



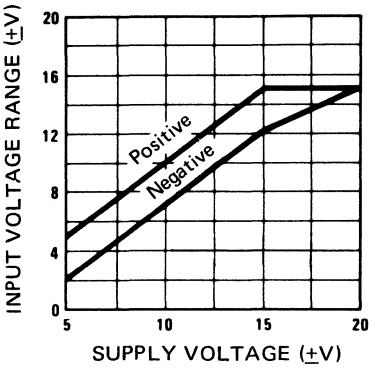
VOLTAGE FOLLOWER PULSE RESPONSE



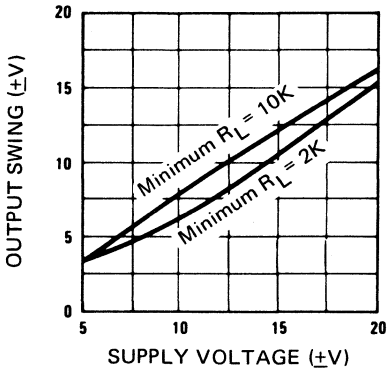
PERFORMANCE CURVES (continued)

GUARANTEED
full operating temperature range (HA-2107: −55°C to +125°C; HA-2207: −25°C to +85°C)

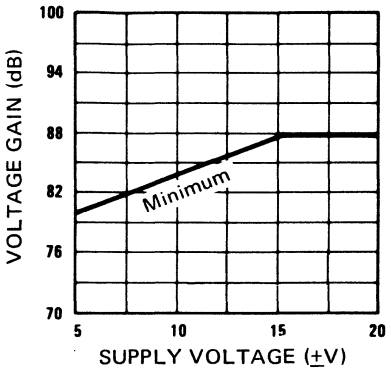
INPUT VOLTAGE RANGE



OUTPUT SWING



VOLTAGE GAIN



DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) ..restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2107-3

Operational Amplifier

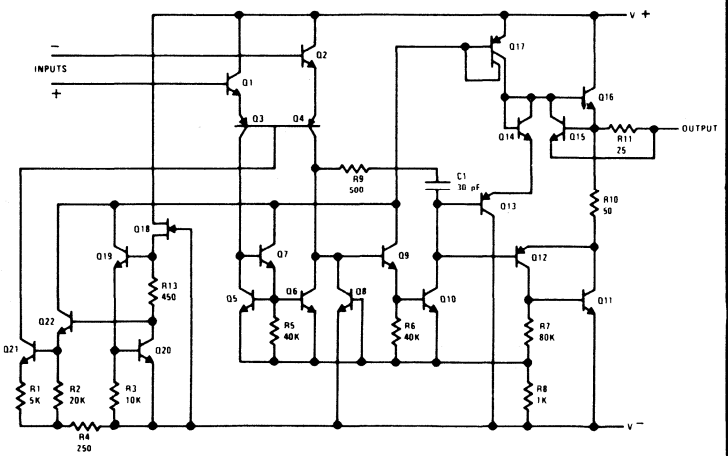
FEATURES

- INTERNAL COMPENSATION
- OPERATION FROM ±5.0V TO ±20.0V SUPPLIES
- CONTINUOUS SHORT-CIRCUIT PROTECTION
- LOW CURRENT DRAIN: 1.8mA AT ±20.0V

GENERAL DESCRIPTION

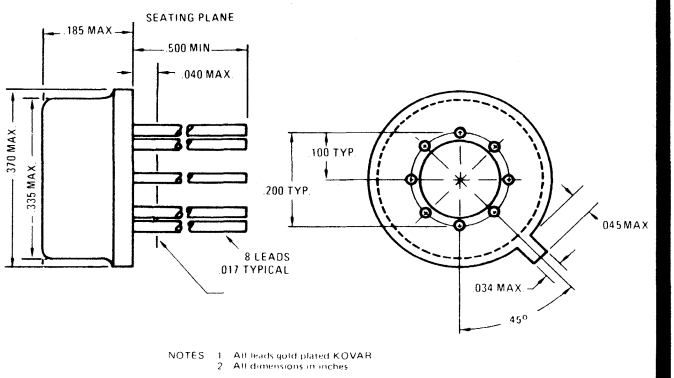
The HA-2107-3 is a general purpose operational amplifier which is internally compensated for unity gain stability. Large common mode signals do not cause latch-up. The HA-2107-3 has a guaranteed operating temperature range of −55°C to +125°C.

SCHEMATIC



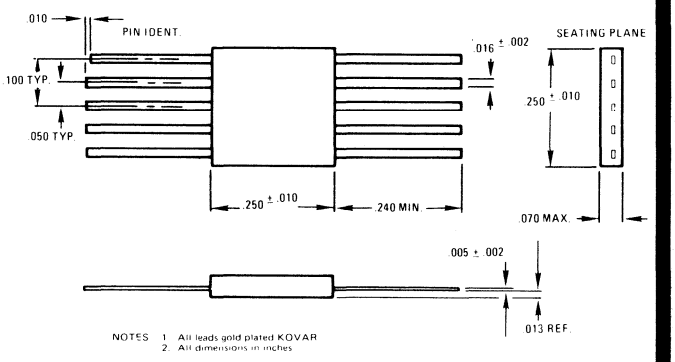
PACKAGES

TO-99

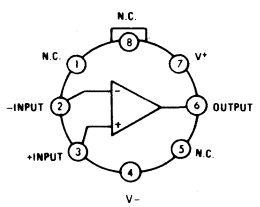


NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

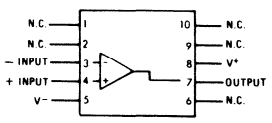
TO-91



NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches



TO-99



TO-91

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.0V	Output Short Circuit Duration	Indefinite
Power Dissipation (Note 1)	500mW	Operating Temperature Range	−55°C to +125°C
Differential Input Voltage	±30.0V	Storage Temperature Range	−65°C to +150°C
Input Voltage (Note 2)	±15.0V	Lead Temperature (Soldering 60 Seconds)	300°C

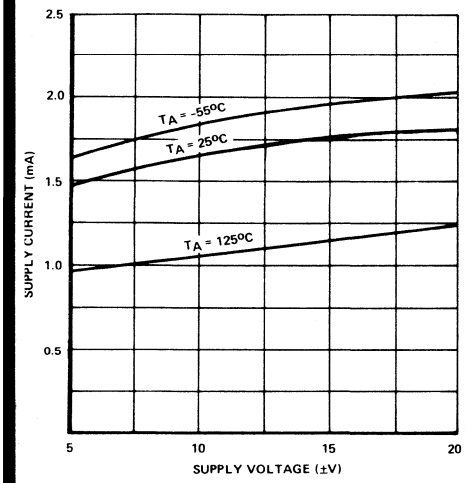
ELECTRICAL CHARACTERISTICS

PARAMETER	TEMPERATURE	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		1.0	5.0	mV
	−55°C to +125°C			6.0	
Average Offset Voltage Temperature Coefficient	−55°C to +125°C		6.0		μV/°C
Bias Current	+25°C		120	500	nA
	−55°C to +125°C		0.28	1.5	μA
Offset Current	+25°C		40	200	nA
	−55°C to +125°C		100	500	nA
Input Resistance	+25°C	300	800		KΩ
Input Voltage Range (Note 6)	−55°C to +125°C	±12.0			V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 5 & 6)	+25°C	50K	160K		V/V
	−55°C to +125°C	25K			V/V
Common Mode Rejection Ratio	−55°C to +125°C	70	90		dB
Output Voltage Swing					
R_L = 10K Ω (Note 6)	−55°C to +125°C	12	14		V
R_L = 2K Ω (Note 6)	−55°C to +125°C	10	13		V
POWER SUPPLY CHARACTERISTICS					
Supply Current (Note 4)	+25°C		1.8	3.0	mA
	+125°C		1.2	2.5	mA
Supply Voltage Rejection Ratio	−55°C to +125°C	70	90		dB

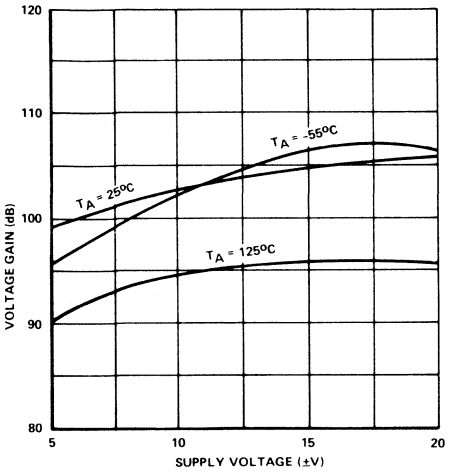
NOTES:
1. Derate TO-99 package at 6.8mW/°C for operation ambient temperature above 75°C and 4.9mW/°C above 50°C for the TO-91 package.
2. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
3. These specifications apply for $\pm 5.0V \leq V_S \leq +20.0V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise specified.
4. $V_S = \pm 20.0V$
5. $R_L = 2k\,\Omega, V_{OUT} = \pm 10.0V$
6. $V_S = \pm 15.0V$

TYPICAL PERFORMANCE CURVES

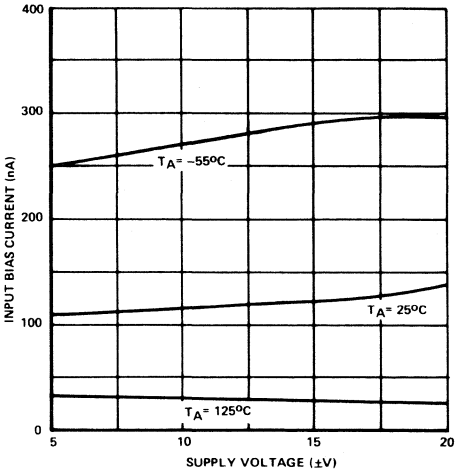
SUPPLY CURRENT



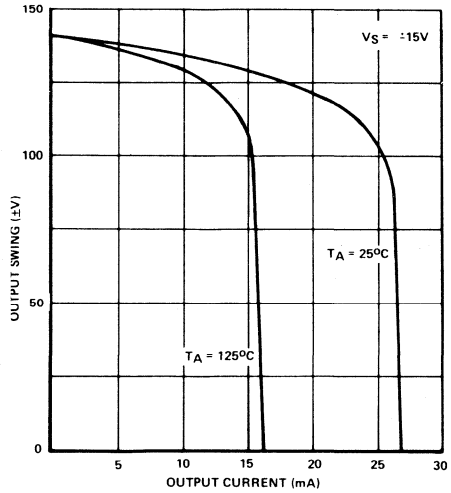
VOLTAGE GAIN



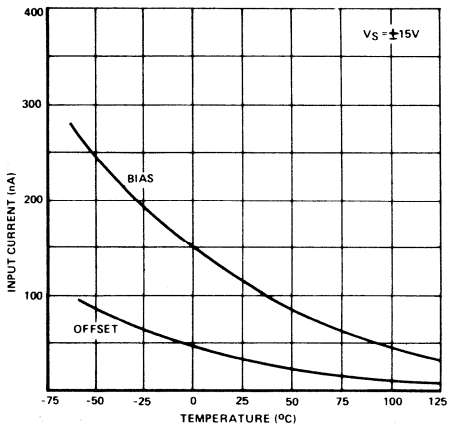
INPUT BIAS CURRENT



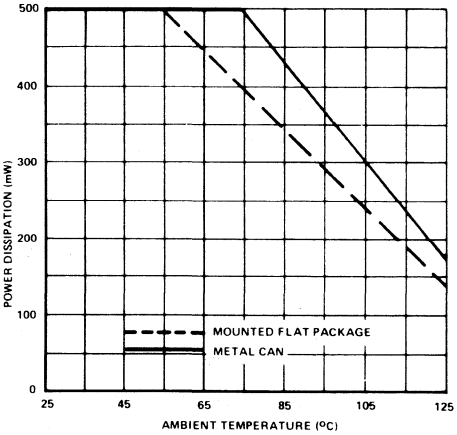
CURRENT LIMITING



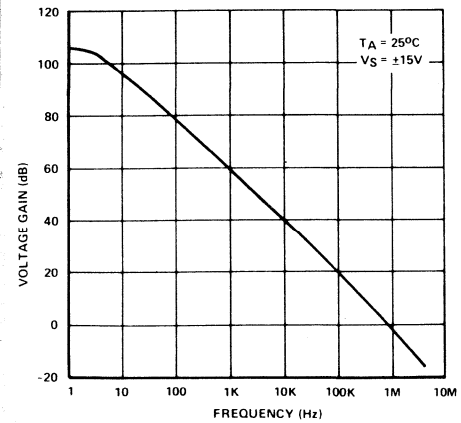
INPUT CURRENT



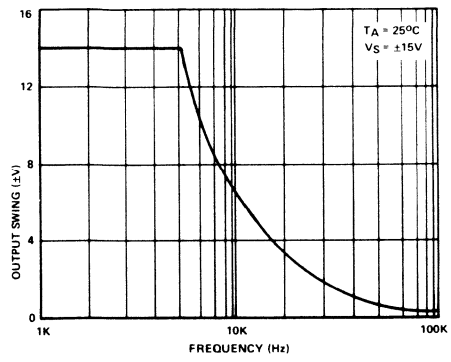
MAXIMUM POWER DISSIPATION



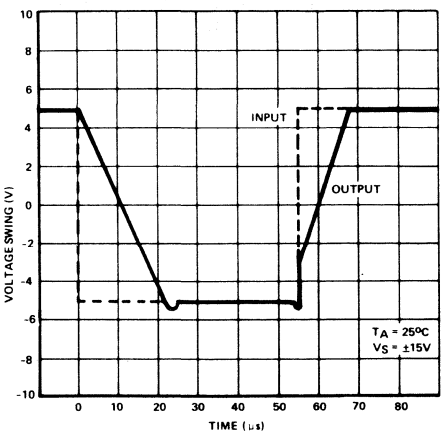
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

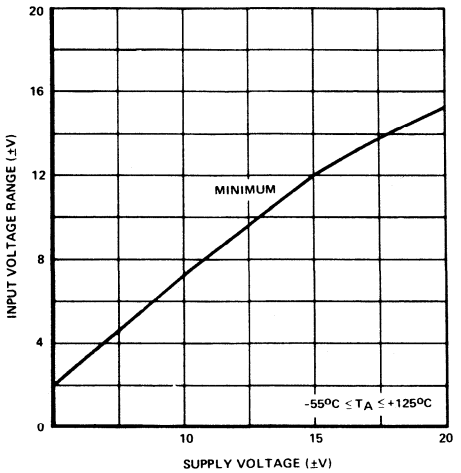


VOLTAGE FOLLOWER PULSE RESPONSE

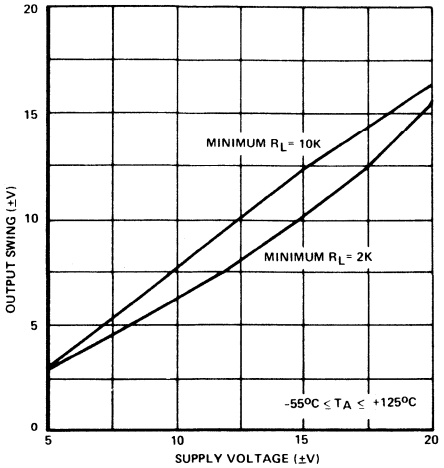


GUARANTEED PERFORMANCE CURVES

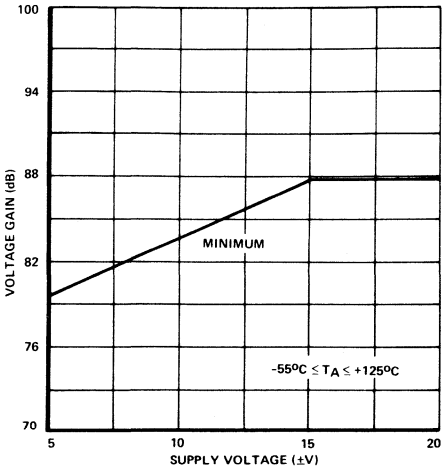
INPUT VOLTAGE RANGE



OUTPUT SWING



VOLTAGE GAIN



DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which if exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) ..restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2111/2211

Voltage Comparators

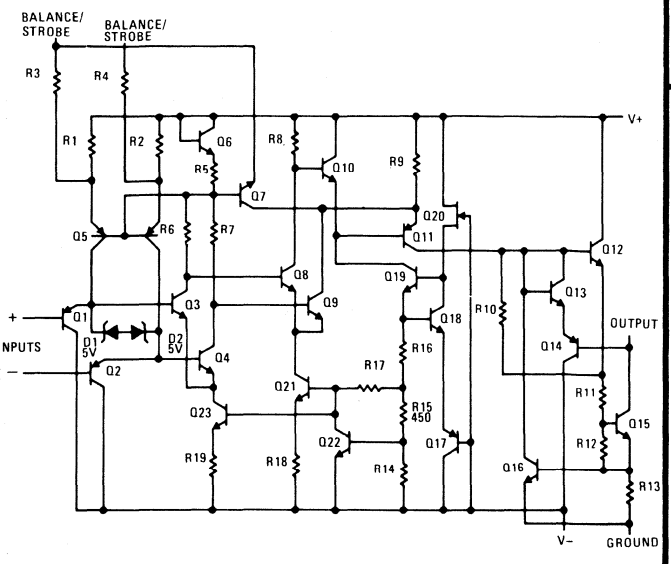
FEATURES

- INPUT BIAS CURRENT — 60nA
- INPUT OFFSET CURRENT — 4nA
- DIFFERENTIAL INPUT VOLTAGE — ±30.0V
- POWER SUPPLY VOLTAGES — A SINGLE 5.0V SUPPLY TO ±15.0V
- OFFSET VOLTAGE NULL CAPABILITY
- STROBE CAPABILITY

GENERAL DESCRIPTION

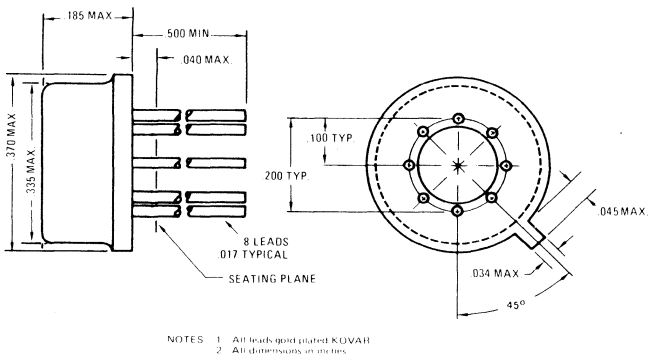
The HA-2111 and HA-2211 are voltage comparators which have low input bias currents. They operate over a wide range of power supply voltages, from the standard ±15.0V down to a single 5.0V power supply. A very flexible output stage is employed, which is compatible with RTL, DTL, TTL and MOS logic circuits.

SCHEMATIC



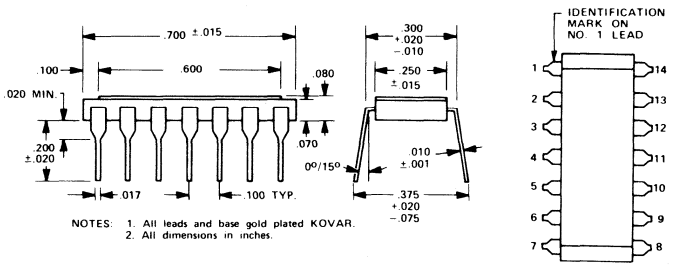
PACKAGES

TO-99



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

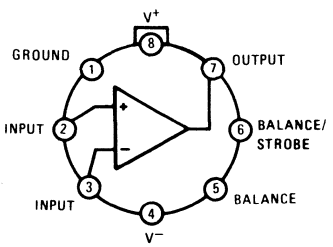
TO-116



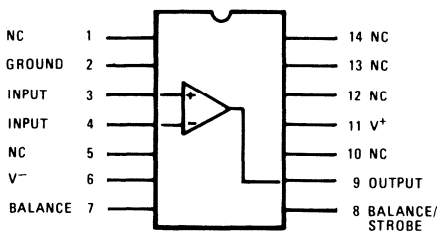
NOTES: 1. All leads and base gold plated KOVAR.
2. All dimensions in inches.

TOP VIEW

TO-99



TO-116



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	36.0V
Output to V^-	50.0V
Ground to V^-	30.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Internal Power Dissipation	500mW
Output Short Circuit Duration	10 sec.
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

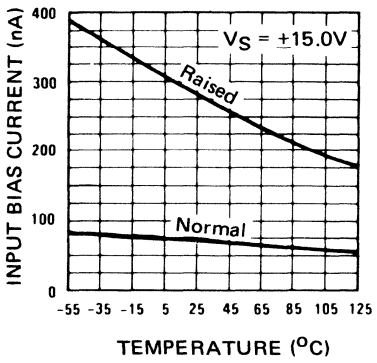
PARAMETER	TEMPERATURE	HA-2111 −55°C to +125°C			HA-2211 −25°C to +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.7	3.0		0.7	3.0	mV
(Note 2)	Full			4.0			4.0	mV
Bias Current	+25°C		60	100		60	100	nA
	Full			150			150	nA
Offset Current	+25°C		4.0	10.0		4.0	10.0	nA
(Note 2)	Full			20.0			20.0	nA
Common Mode Range	Full		±14.0			±14.0		V
Strobe Current	+25°C		3.0			3.0		mA
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C		200K			200K		V/V
Response Time (Note 3)	+25°C		200			200		ns
OUTPUT CHARACTERISTICS								
Leakage Current	+25°C		0.2	10.0		0.2	10.0	nA
(Note 4)	Full			500			500	nA
Saturation Voltage (Note 5)	+25°C		0.75	1.5		0.75	1.5	V
(Note 6)	Full		0.23	0.4		0.23	0.4	V
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current	+25°C		5.1	6.0		5.1	6.0	mA
Negative Supply Current	+25°C		4.1	5.0		4.1	5.0	mA

NOTES:

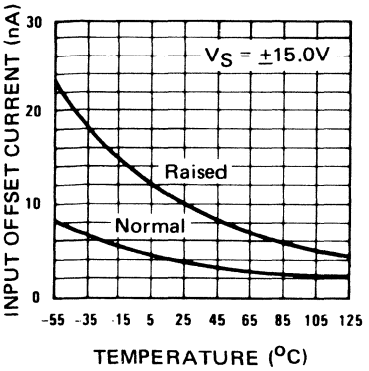
1. This rating applies for ±15.0V supplies. The positive input voltage limit is 30.0V above the negative supply. The negative input voltage is equal to the negative supply voltage or 30.0V below the positive supply, whichever is less.
2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
3. 100mV input step; 5mV overdrive.
4. $V_{OUT} = 35.0V$; $V_{IN} = 5mV$
5. $I_{OUT} = 50mA$; $V_{IN} = -5mV$
6. $I_{Sink} = 8mA$; $V^+ = 4.5V$; $V^- = 0V$; $V_{IN+} = +1.00V$; $V_{IN-} = +1.006V$

TYPICAL PERFORMANCE CURVES

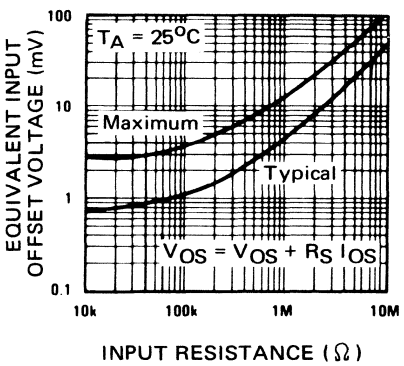
INPUT BIAS CURRENT



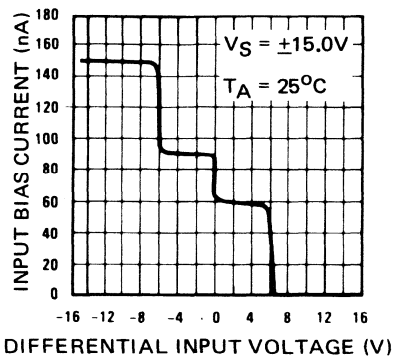
INPUT OFFSET CURRENT



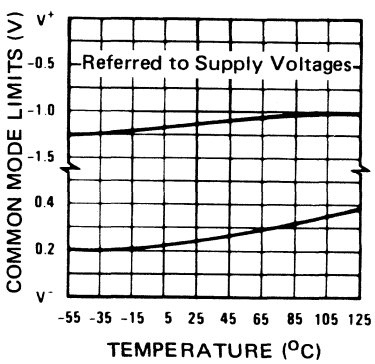
OFFSET ERROR



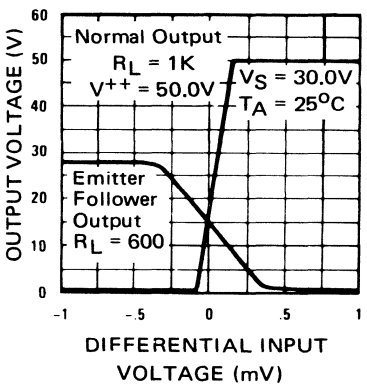
INPUT CHARACTERISTICS



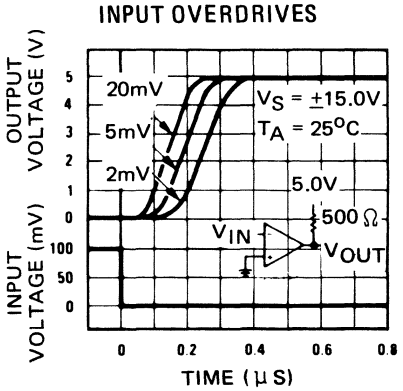
COMMON MODE LIMITS



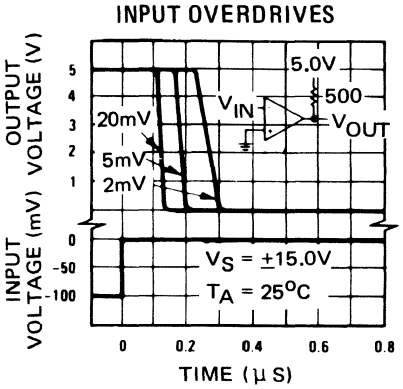
TRANSFER FUNCTION



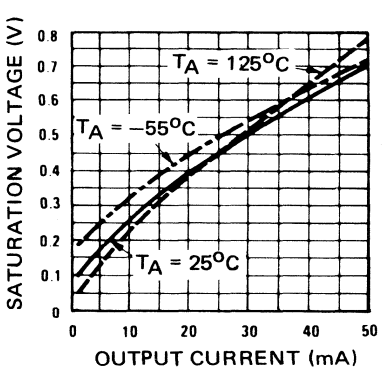
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



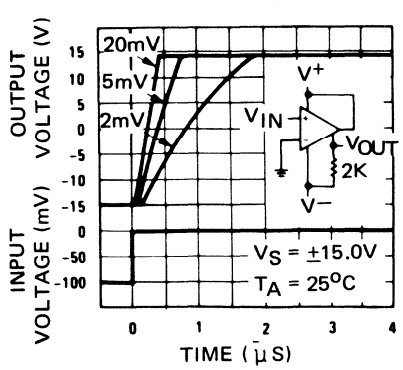
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



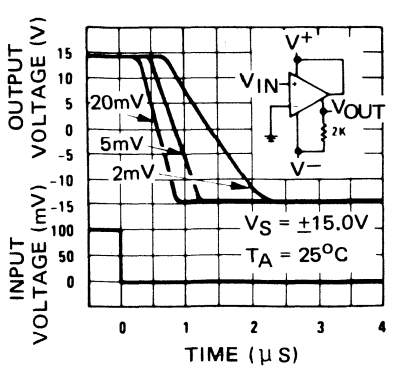
OUTPUT SATURATION VOLTAGE



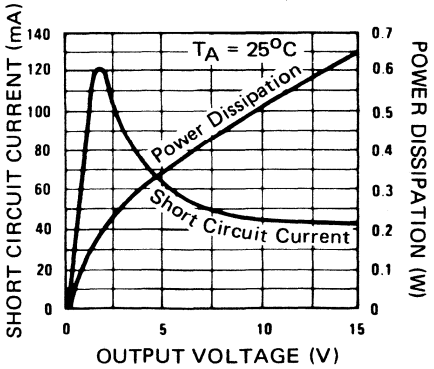
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

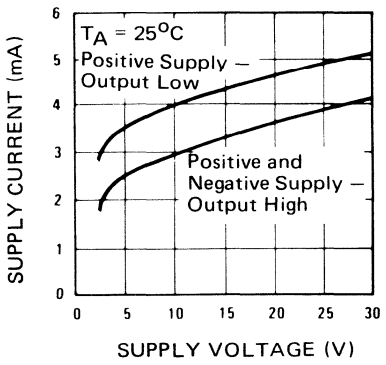


OUTPUT LIMITING CHARACTERISTICS

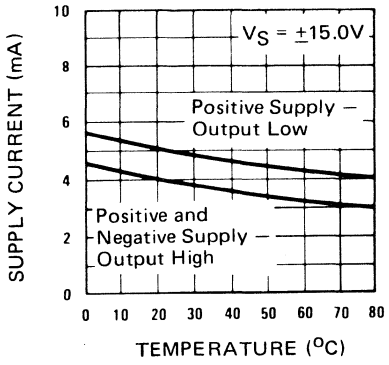


TYPICAL PERFORMANCE CURVES(continued)

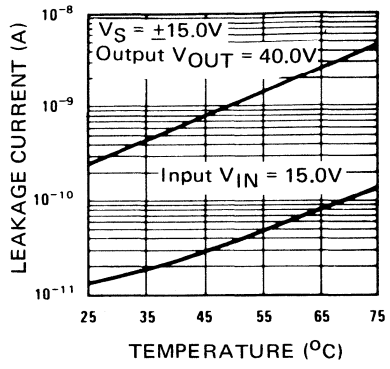
SUPPLY CURRENT



SUPPLY CURRENT

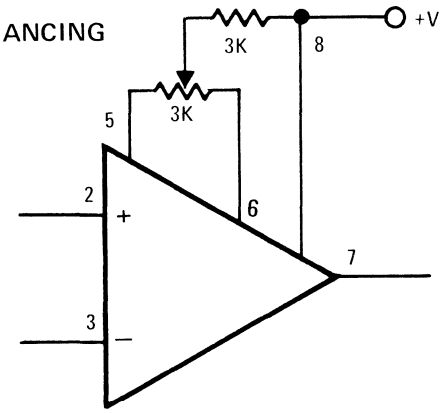


LEAKAGE CURRENTS

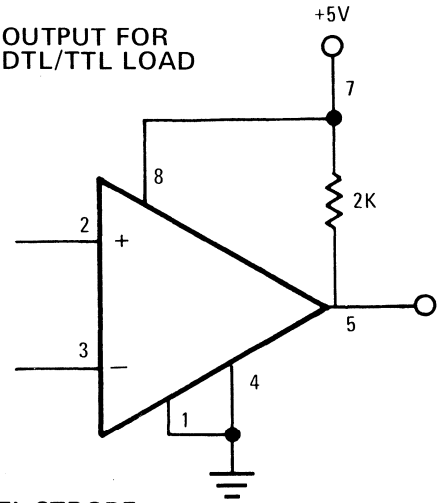


APPLICATION INFORMATION

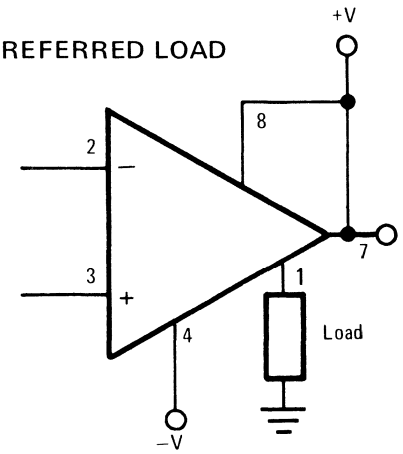
OFFSET BALANCING



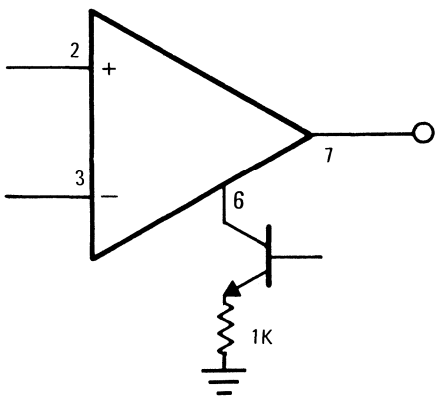
OUTPUT FOR DTL/TTL LOAD



GROUND REFERRED LOAD



TTL STROBE



NOTE: INPUT POLARITIES REVERSED

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2311

Voltage Comparator

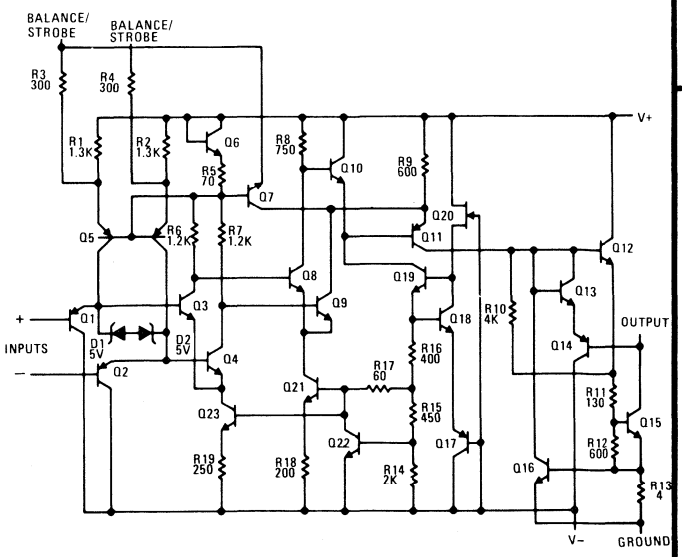
FEATURES

- INPUT BIAS CURRENT — 100nA
- INPUT OFFSET CURRENT — 6nA
- DIFFERENTIAL INPUT VOLTAGE — ±30.0V
- POWER SUPPLY VOLTAGES — A SINGLE +5.0V SUPPLY TO ±15.0V
- OFFSET VOLTAGE NULL CAPABILITY
- STROBE CAPABILITY

GENERAL DESCRIPTION

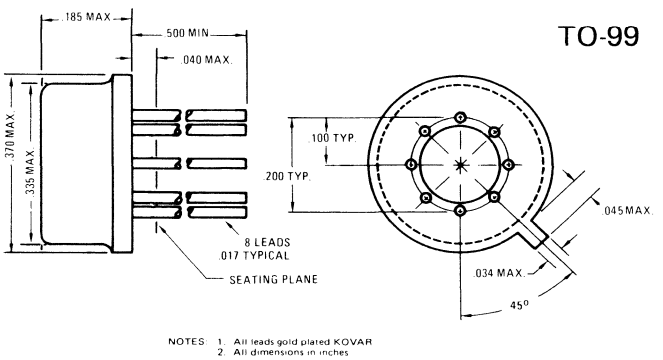
The HA-2311 is a voltage comparator which has low input bias currents. It operates over a wide range of power supply voltages, from the standard ±15.0V down to a single 5.0 V power supply. A very flexible output stage is employed which is compatible with RTL, DTL, TTL and MOS logic circuits.

SCHEMATIC



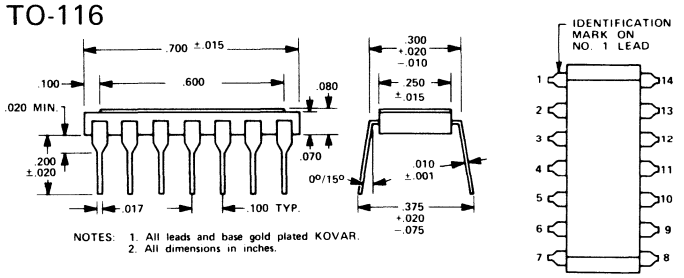
PACKAGES

TO-99



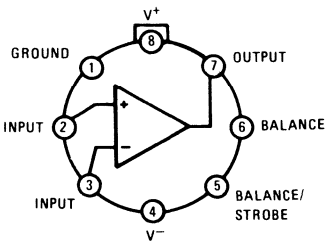
NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-116

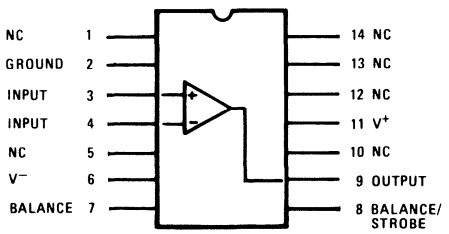


NOTES: 1. All leads and base gold plated KOVAR.
2. All dimensions in inches.

TO-99



TO-116



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	36.0V
Output to V^-	40.0V
Ground to V^-	30.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Internal Power Dissipation	500mW
Output Short Circuit Duration	10 sec.
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

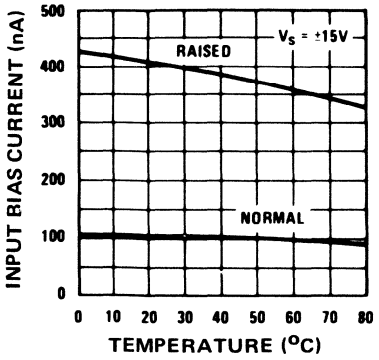
V^+ = +15.0 V.D.C. V^- = −15.0 V.D.C.

PARAMETER	TEMPERATURE	HA-2311 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage (Note 2)	+25°C		2.0	7.5	mV
	0°C to +75°C			10.0	mV
Bias Current	+25°C		100	250	nA
	0°C to +75°C			300	nA
Offset Current (Note 2)	+25°C		6.0	50.0	nA
	0°C to +75°C			70.0	nA
Common Mode Range	0°C to +75°C		±14.0		V
Strobe Current	+25°C		3.0		mA
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain	+25°C		200K		V/V
Response Time (Note 3)	+25°C		200		ns
OUTPUT CHARACTERISTICS					
Leakage Current (Note 4)	+25°C		0.2	50.0	nA
Saturation Voltage (Note 5)	+25°C		0.75	1.5	V
(Note 6)	0°C to +75°C		0.23	0.4	V
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current	+25°C		5.1	7.5	mA
Negative Supply Current	+25°C		4.1	5.0	mA

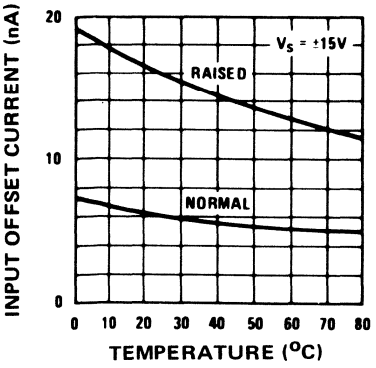
NOTES:
1. This rating applies for ±15.0V supplies. The positive input voltage limit is 30.0V above the negative supply. The negative input voltage is equal to the negative supply voltage or 30.0V below the positive supply, whichever is less.
2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
3. 100mV input step; 5mV overdrive.
4. V_{OUT} = 35.0V; V_{IN} = 10mV
5. I_{OUT} = 50mA; V_{IN} = −10mV
6. I_{SINK} =8mA, V^+=4.5V, V^-=0.0V, V_{IN}^+= +1.0V V_{IN}^-=+1.01V

TYPICAL PERFORMANCE CURVES

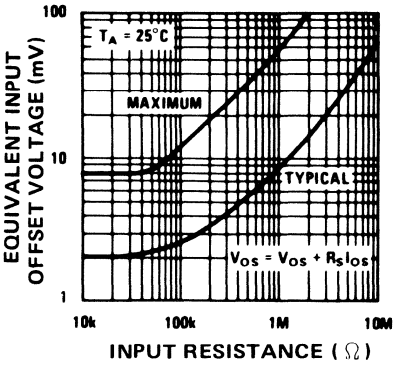
INPUT BIAS CURRENT



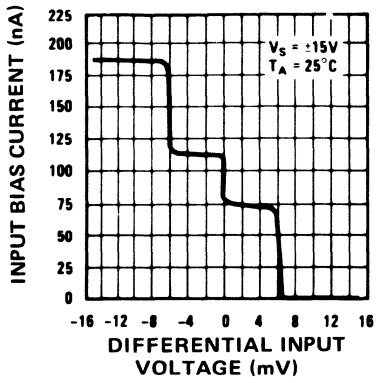
INPUT OFFSET CURRENT



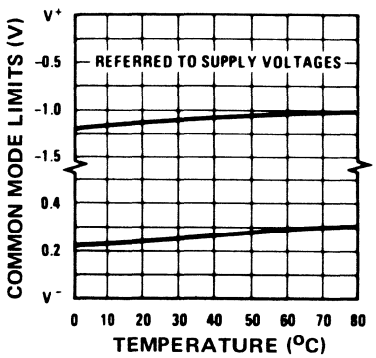
OFFSET ERROR



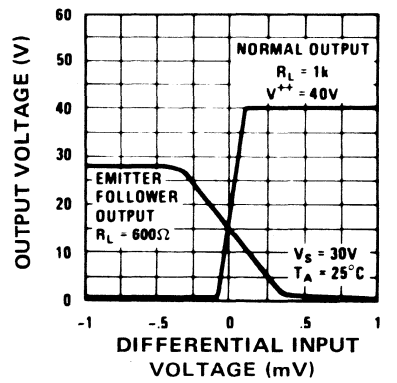
INPUT CHARACTERISTICS



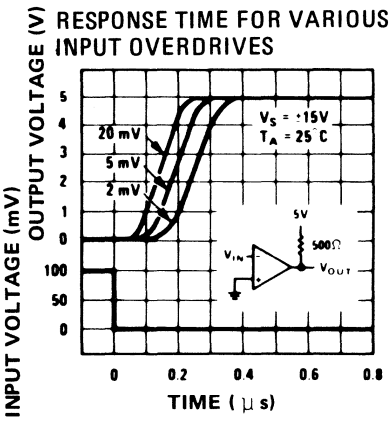
COMMON MODE LIMITS



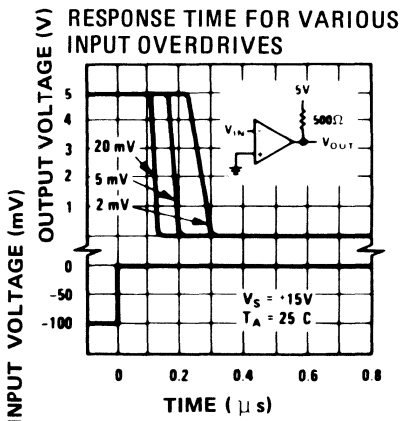
TRANSFER FUNCTION



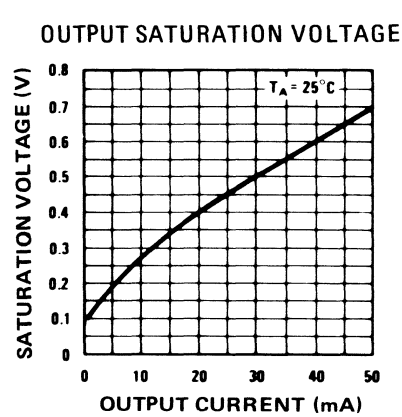
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



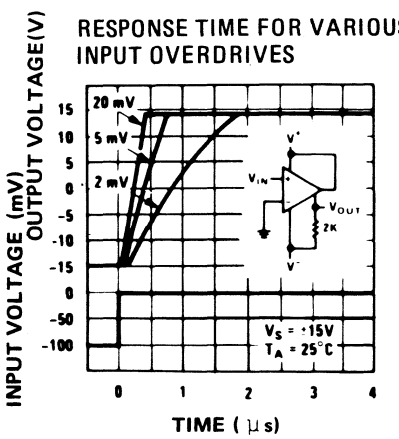
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



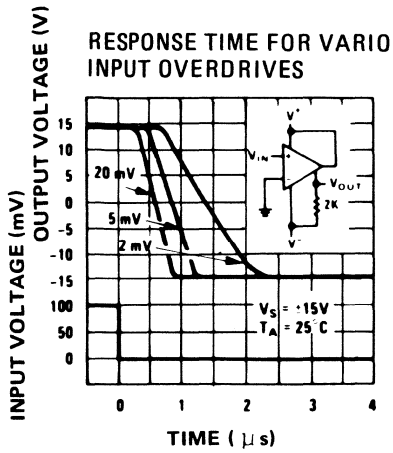
OUTPUT SATURATION VOLTAGE



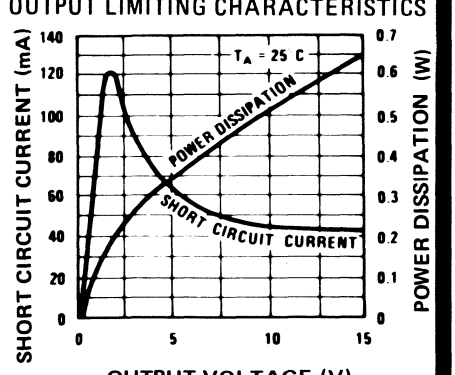
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

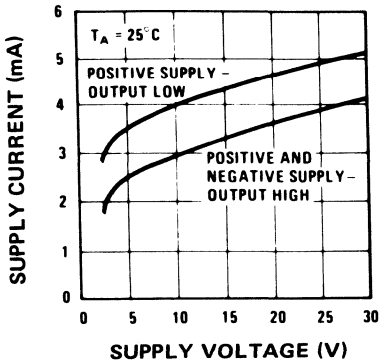


OUTPUT LIMITING CHARACTERISTICS

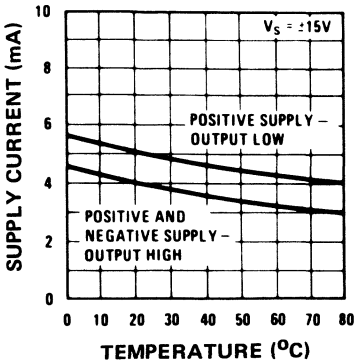


TYPICAL PERFORMANCE CURVES (continued)

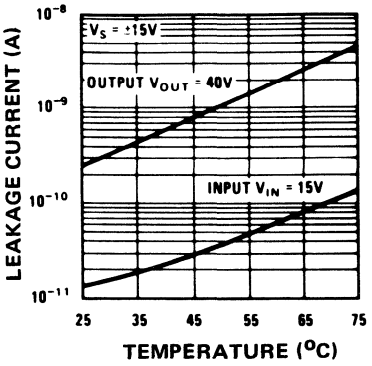
SUPPLY CURRENT



SUPPLY CURRENT

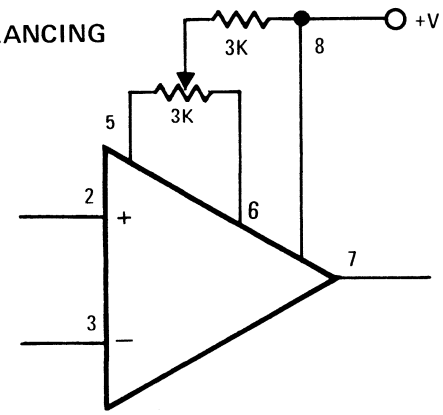


LEAKAGE CURRENTS

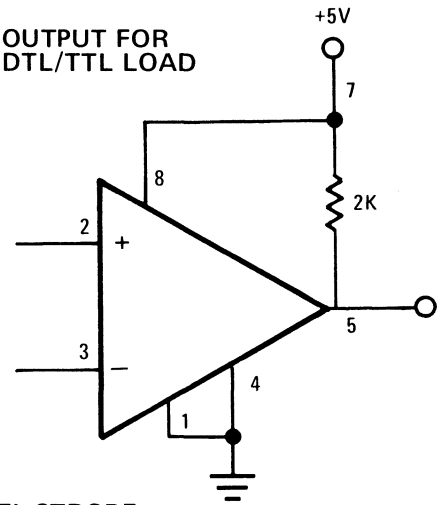


APPLICATION INFORMATION

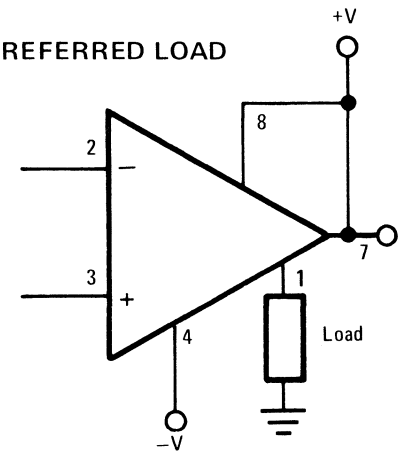
OFFSET BALANCING



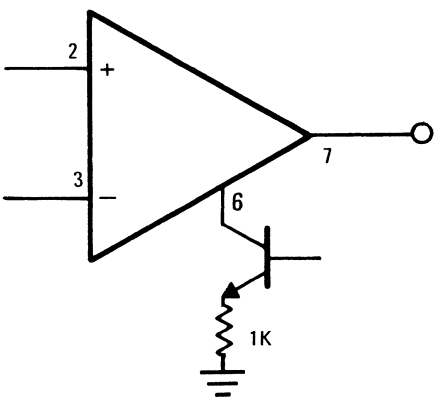
OUTPUT FOR DTL/TTL LOAD



GROUND REFERRED LOAD



TTL STROBE



NOTE: INPUT POLARITIES REVERSED

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2400/2404/2405

PRAM™ Four Channel Programmable Amplifier

LINEAR DATA

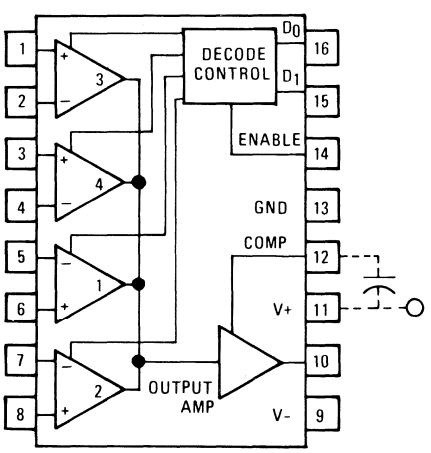
FEATURES

- THOUSANDS OF NEW APPLICATIONS; PROGRAM:
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS
  - ETC., ETC.
- HIGH SLEW RATE 50V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

GENERAL DESCRIPTION

The HA-2400 is an operational amplifier with four identical input stages, any one (or none) of which may be electronically connected to the single output stage. The "ON" channel is selected through DTL/TTL compatible address inputs. The amplifier formed by the output and the selected pair of amplifier inputs is a high performance operational amplifier which can be operated with suitable feedback networks in any of the well known op amp configurations. The unselected amplifier inputs are effectively "floating". The device is an extremely versatile analog building block. It can be used as an analog signal selector, sampler, or multiplexer with built in buffering or signal conditioning. By connecting different feedback networks from the output to each input pair, it can be used as a single or multiple channel amplifier with programmable feedback characteristics. The device is packaged in a hermetic 16 pin dual in-line package. The HA-2400 operates over the temperature range of $-55^{o}C$ to $+125^{o}C$, the HA-2404 operates over $-25^{o}C$ to $+85^{o}C$, while the HA-2405 operates over $0^{o}C$ to $+75^{o}C$.

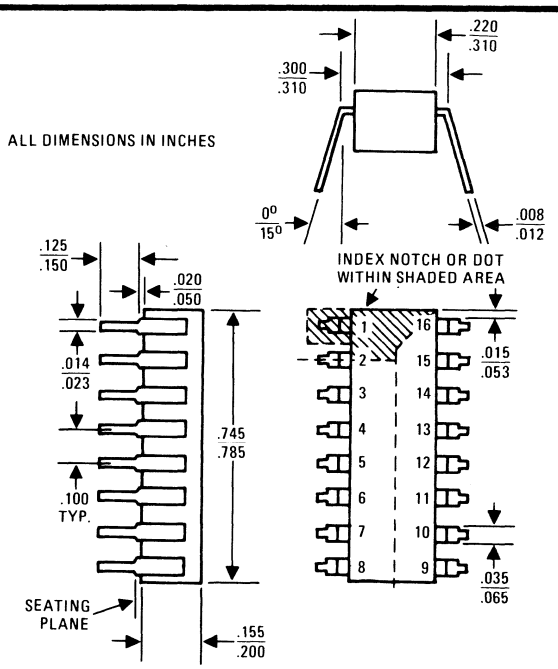
FUNCTIONAL DIAGRAM



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

PACKAGE



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V	Internal Power Dissipation	300mW
Differential Input Voltage	45.0V	Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2400)
Digital Input Voltage	−0.76V to +10.0V		$-25^{o}C \leq T_A \leq +85^{o}C$ (HA-2404)
Output Current	Short Circuit Protected		$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2405)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

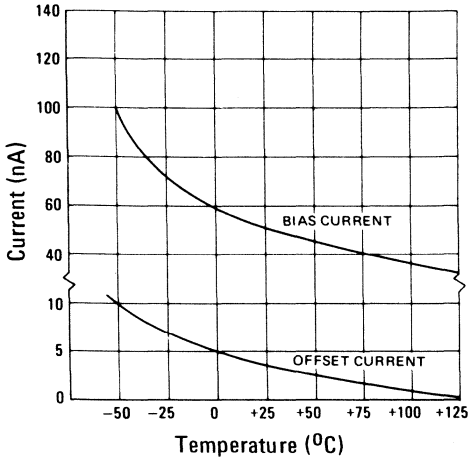
PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	5		4	9	mV
	Full			7			11	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C		40			40		MHz
(Note 4)	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C		20			20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C		500			500		kHz
(Notes 4,5)	+25°C		200			200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20			20		ns
Overshoot (Notes 4,6)	+25°C		25			25		%
Slew Rate (Notes 3,7)	+25°C		50			50		V/μs
(Notes 4,7)	+25°C		15			15		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5			1.5		μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1			1		mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100			100		ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	80	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5$ V.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 400$ mV peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10$V.D.C. to ± 20V.D.C.
12. Unselected channels have approximately the same input parameters.

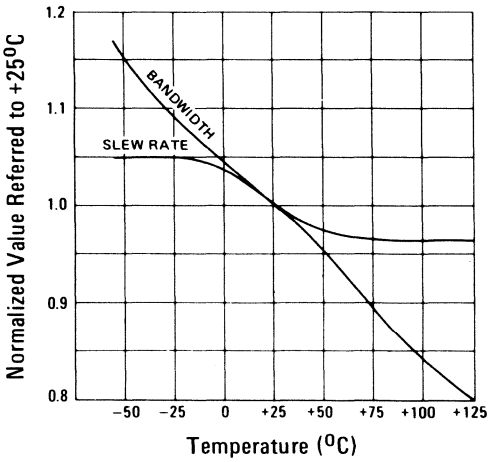
CHARACTERISTIC CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

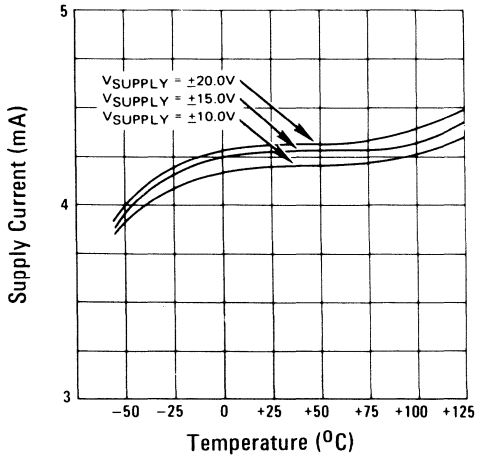
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



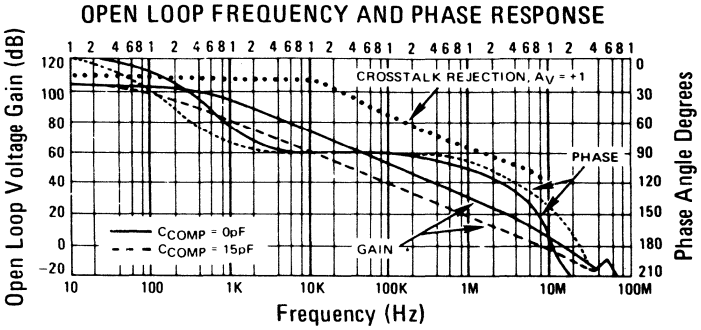
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



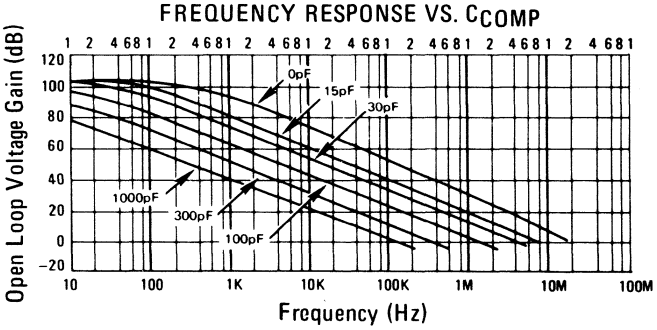
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



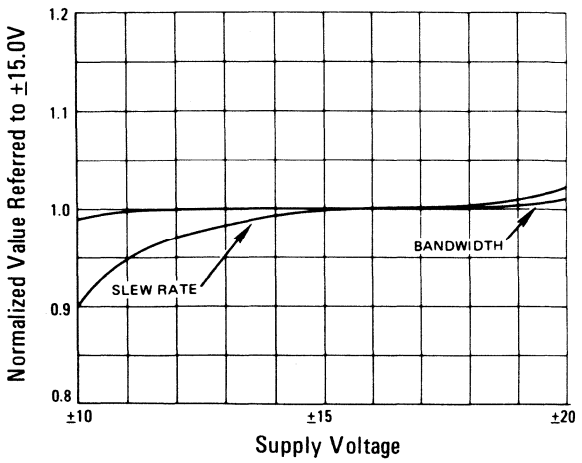
OPEN LOOP FREQUENCY AND PHASE RESPONSE



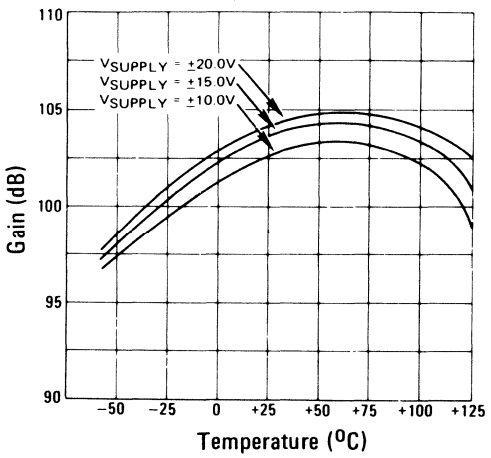
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE

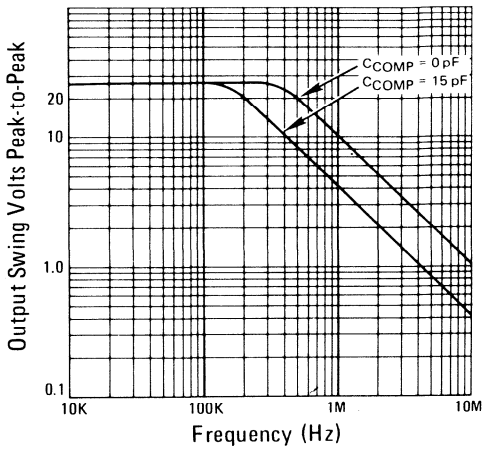


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

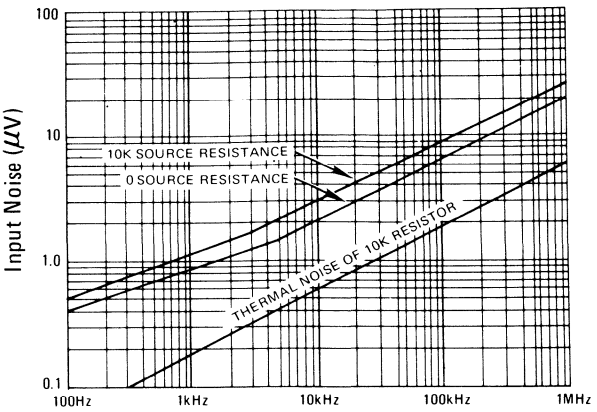


CHARACTERISTC CURVES (continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

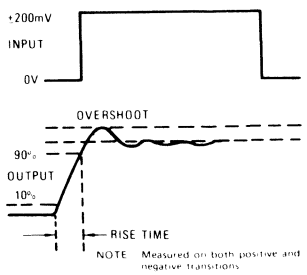


EQUIVALENT INPUT NOISE VS. BANDWIDTH

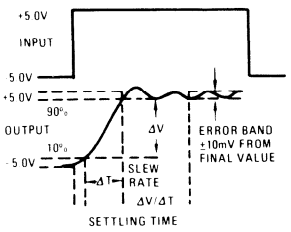


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

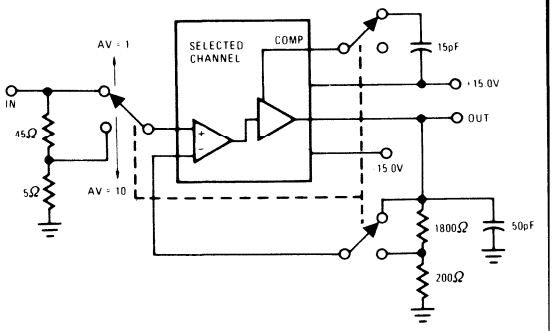
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

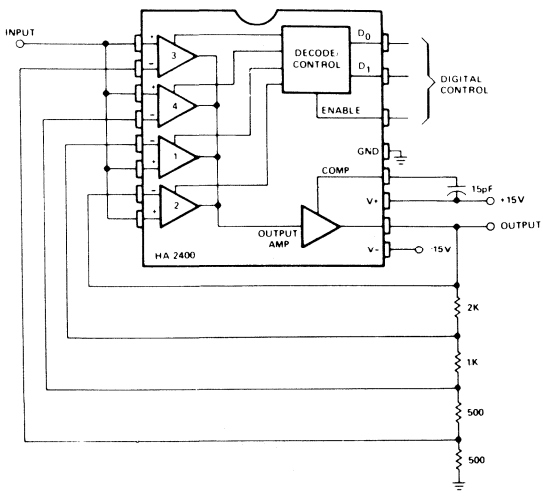


SLEW RATE AND TRANSIENT RESPONSE

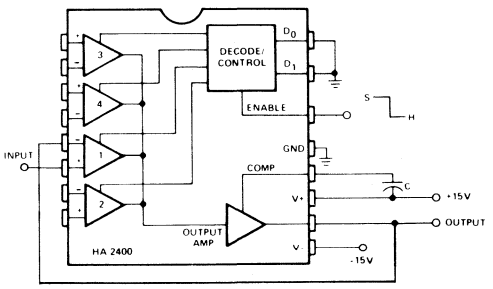


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedistal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A

$I_2 \approx 200 \times 10^{-9}$ A @ +25°C

$\approx 600 \times 10^{-9}$ A @ -55°C

$\approx 100 \times 10^{-9}$ A @ +125°C

$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2500/2502/2505

High Slew Rate Operational Amplifiers

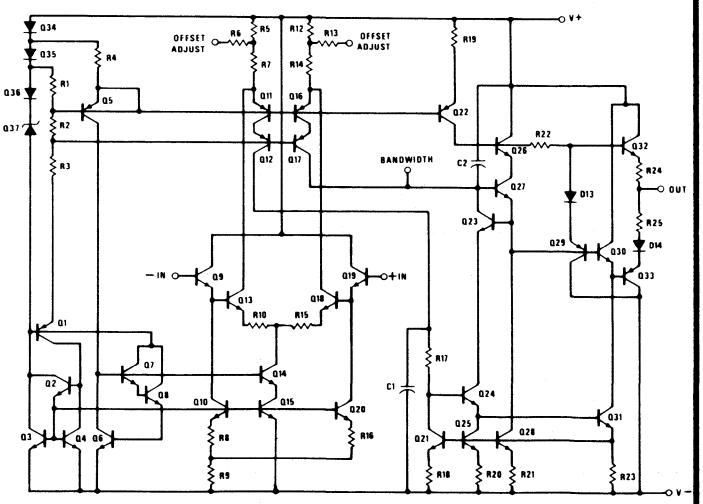
FEATURES

- HIGH SLEW RATE — 30V/μs
- FAST SETTLING — 330ns
- WIDE POWER BANDWIDTH — 500kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100mΩ
- LOW OFFSET CURRENT — 10nA
- TRUE OP-AMP – CAN BE OPERATED NON-INVERTING OR INVERTING
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

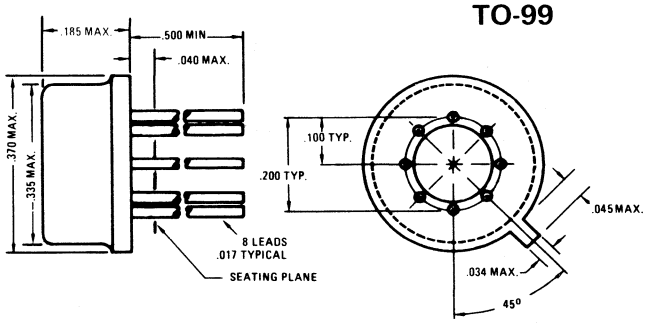
An operational amplifier with excellent D.C. characteristics, featuring high slew rate and fast settling time. Ideal for use in A/D, D/A, and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The HA-2500/02/05 is internally compensated.

SCHEMATIC



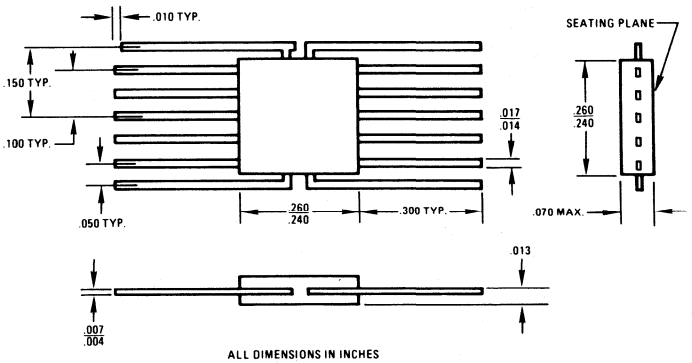
PACKAGES

TO-99



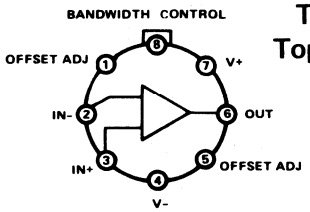
NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-86

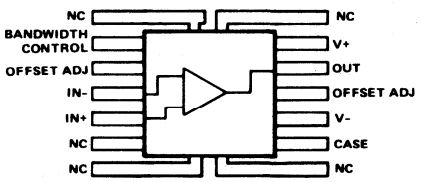


ALL DIMENSIONS IN INCHES

TO-99 Top View



TO-86



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

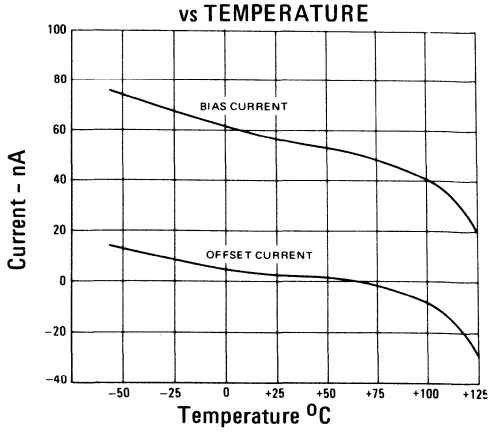
		HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1,4,5 & 8)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,4,5 & 8)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. A_V > 10
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±200mV
7. ΔV = ±5.0V
8. See transient response test circuits and waveforms page four.

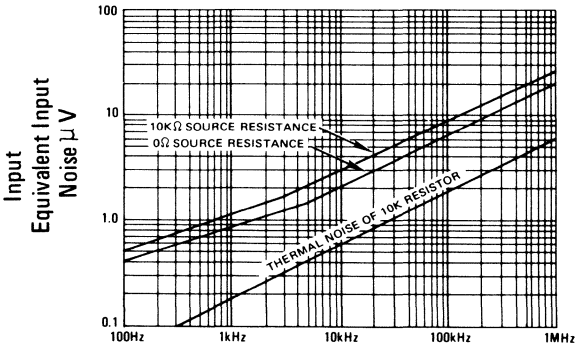
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

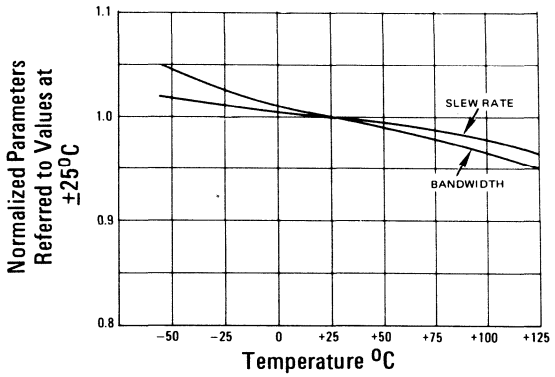
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



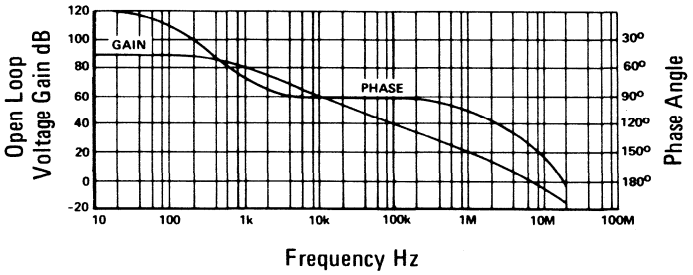
EQUIVALENT INPUT NOISE vs BANDWIDTH



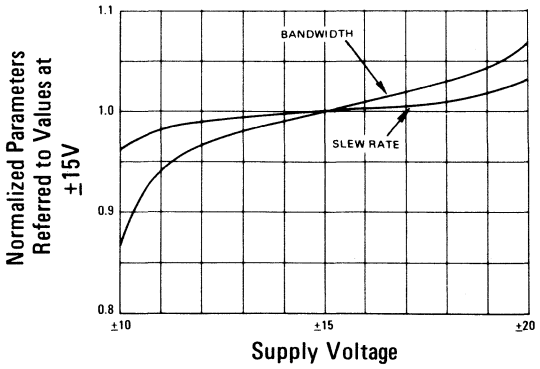
NORMALIZED AC PARAMETERS vs TEMPERATURE



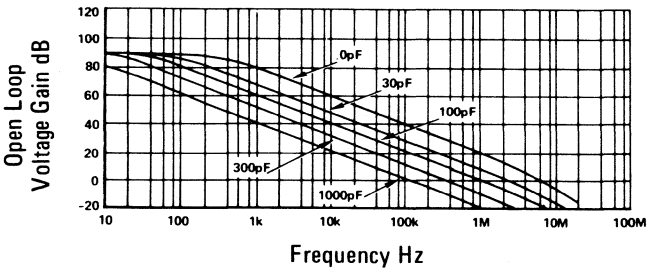
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

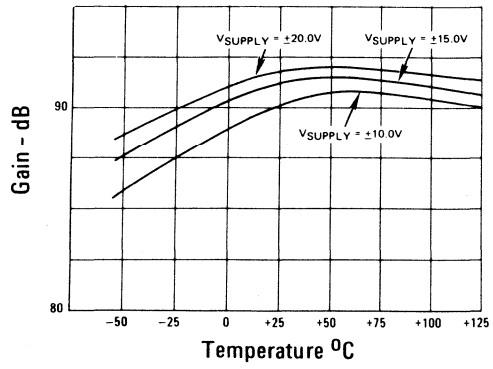


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

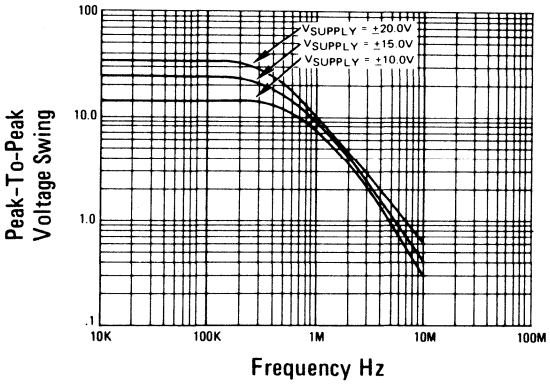


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

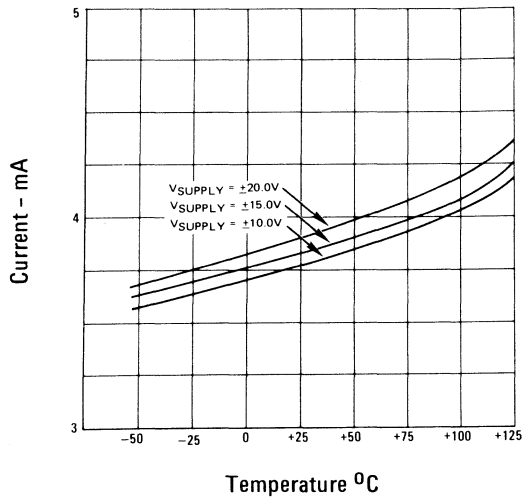


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

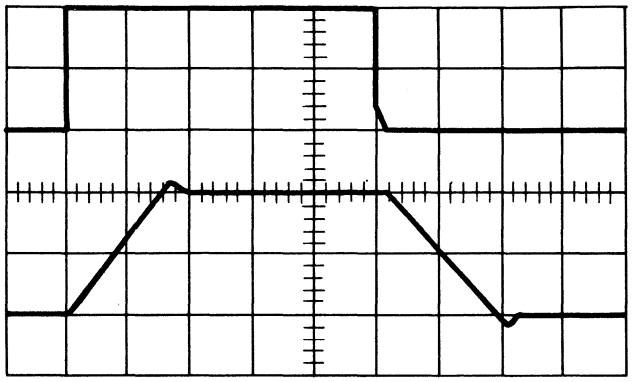


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



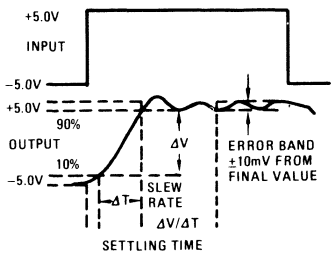
VOLTAGE FOLLOWER PULSE RESPONSE



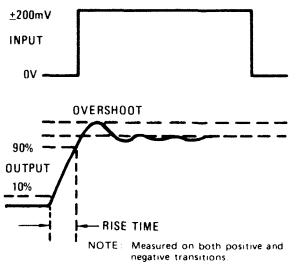
R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

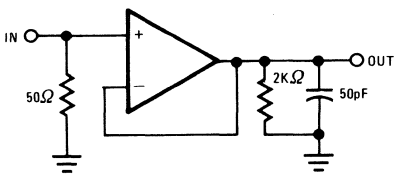
SLEW RATE AND SETTLING TIME



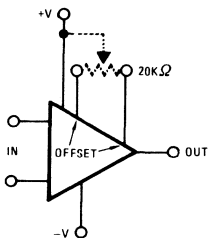
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rating Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME—Time required for output waveform to remain within 0.1 percent of final value.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

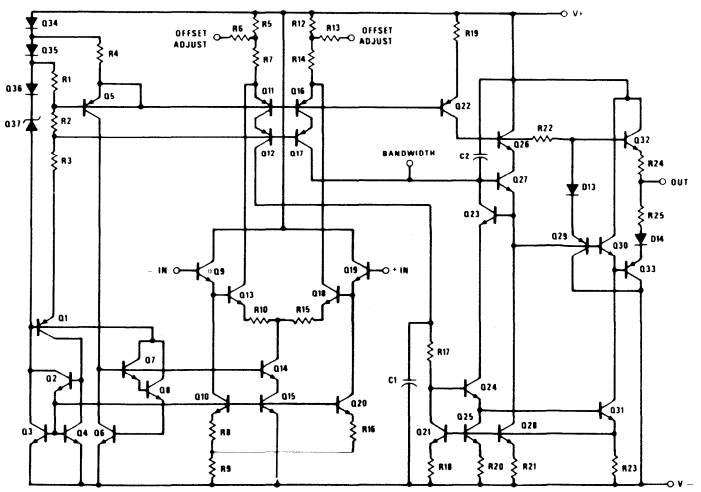
FEATURES

- HIGH SLEW RATE — 60V/μs
- FAST SETTLING — 250ns
- WIDE POWER BANDWIDTH — 1,000 kHz
- HIGH GAIN BANDWIDTH — 12 MHz
- HIGH INPUT IMPEDANCE — 100mΩ
- LOW OFFSET CURRENT — 10nA
- TRUE OP AMP – CAN BE OPERATED NON-INVERTING OR INVERTING
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

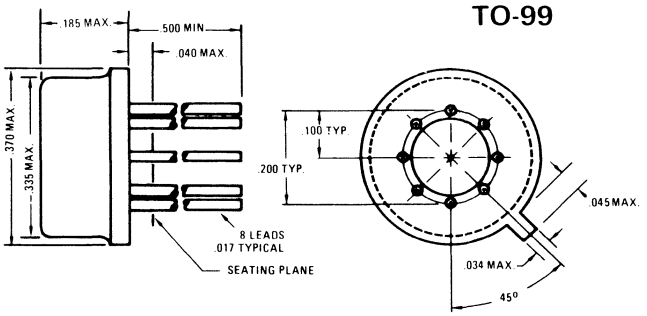
An operational amplifier with excellent D.C. characteristics, featuring high slew rate and fast settling time. Ideal for use in A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The HA-2510/12/15 is internally compensated.

SCHEMATIC



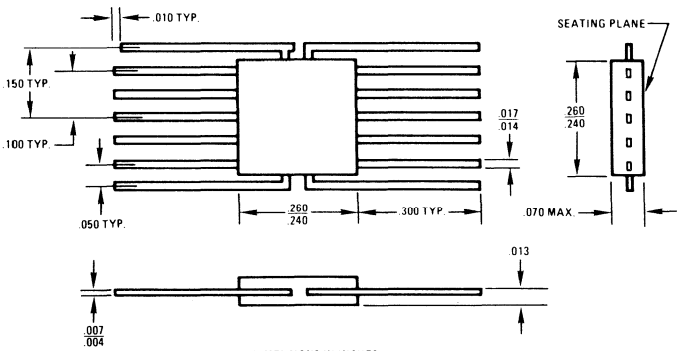
PACKAGES

TO-99



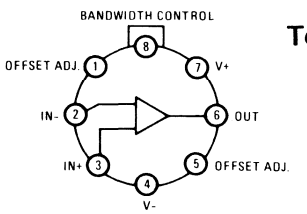
NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-86

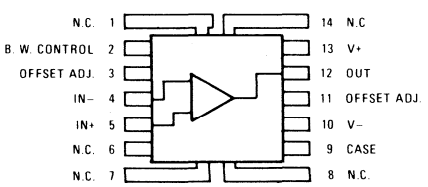


ALL DIMENSIONS IN INCHES

TO-99 Top View



TO-86



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

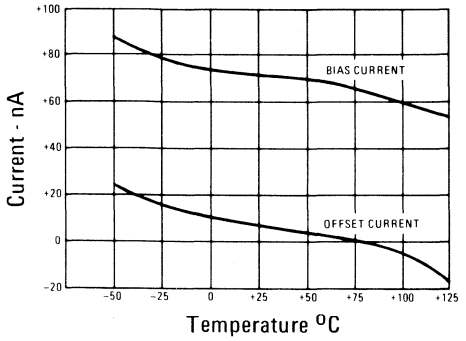
PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	HA-2510 TYP.	HA-2510 MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	HA-2512 TYP.	HA-2512 MAX.	HA-2515 0°C to +75°C LIMITS MIN.	HA-2515 TYP.	HA-2515 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms page four.

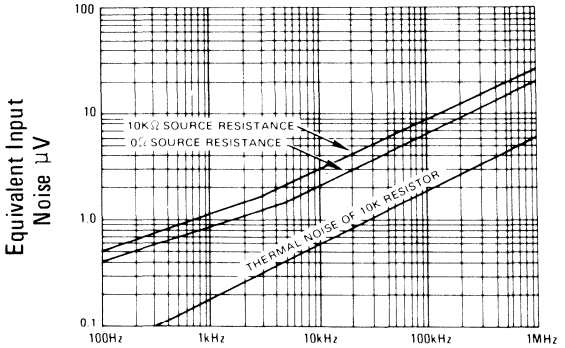
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

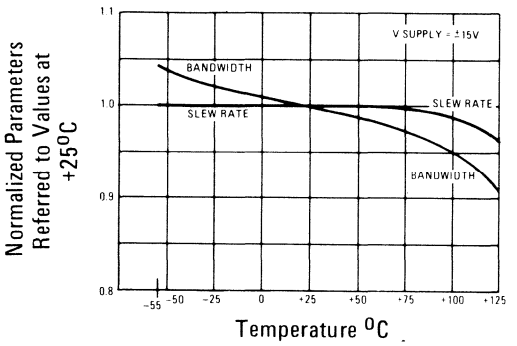
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



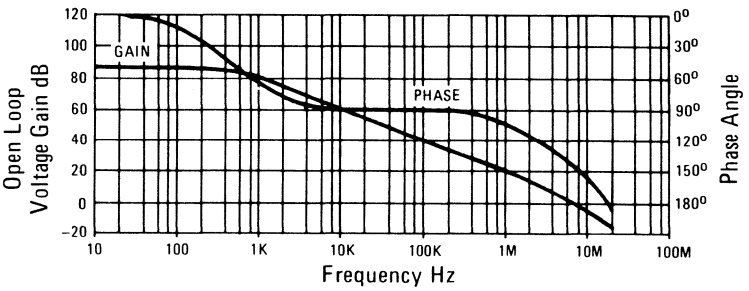
EQUIVALENT INPUT NOISE vs BANDWIDTH



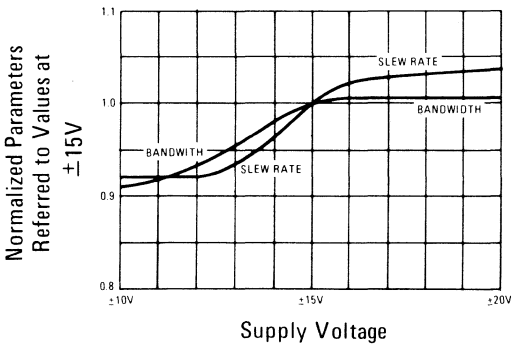
NORMALIZED AC PARAMETERS vs TEMPERATURE



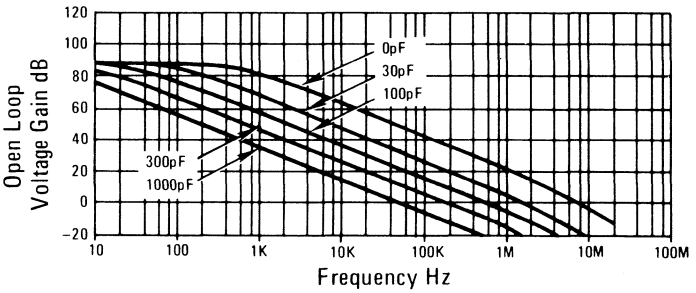
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

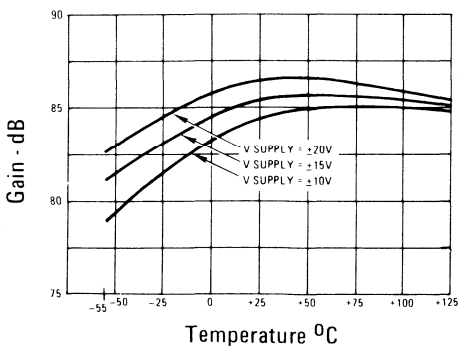


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

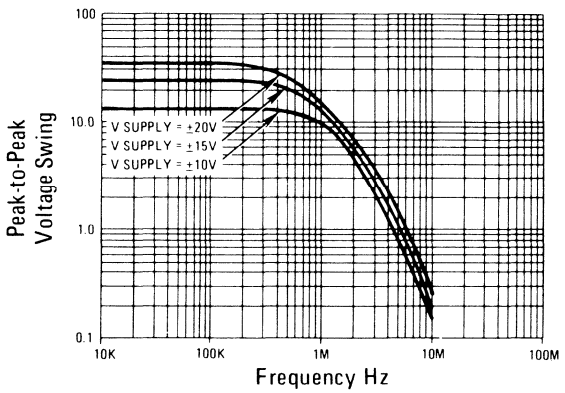


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

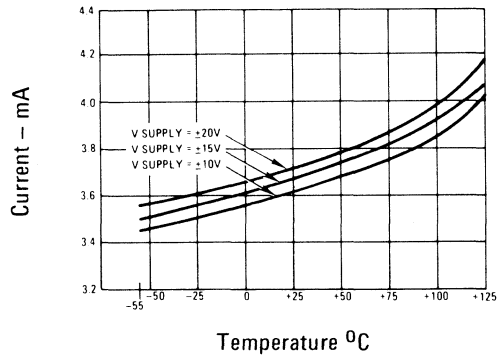


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

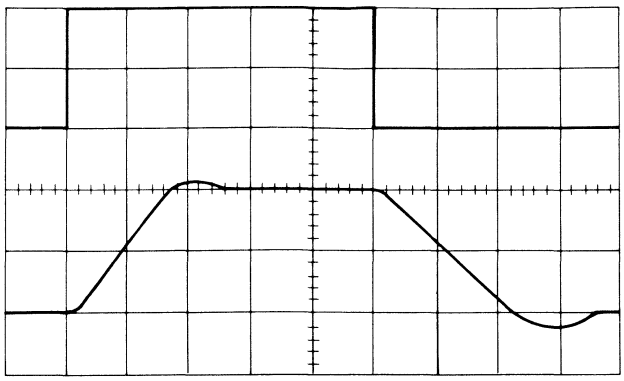


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS
TEMPERATURE



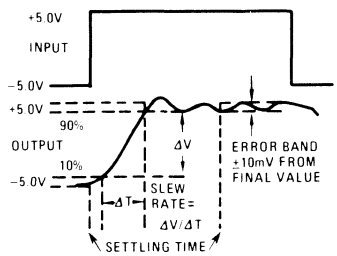
VOLTAGE FOLLOWER PULSE RESPONSE



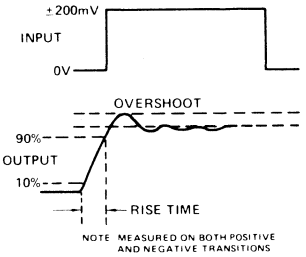
$R_L = 2K\,\Omega$, $C_L = 50pF$
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
$T_A = +25^0C$, $V_S = \pm 15.0V$

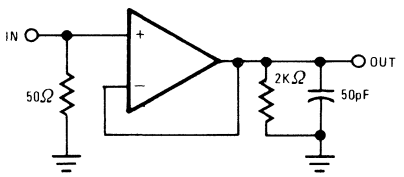
SLEW RATE AND SETTLING TIME



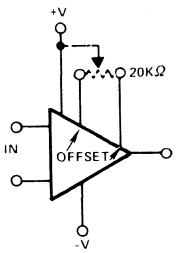
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2520/2522/2525

High Slew Rate Operational Amplifiers

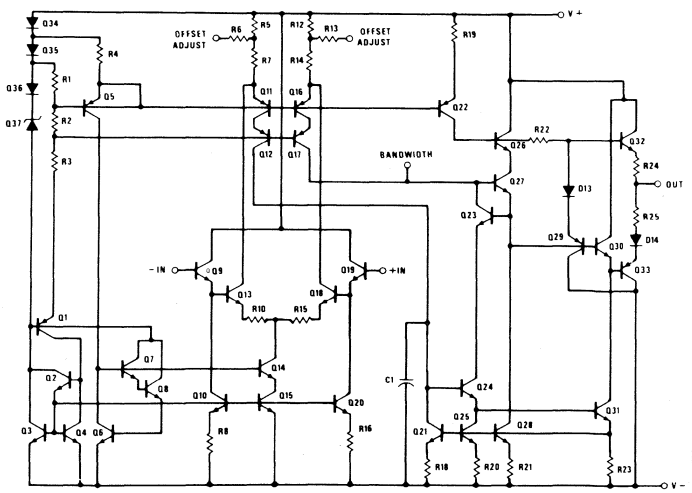
FEATURES

- HIGH SLEW RATE 120V/μs
- FAST SETTLING 200ns
- WIDE POWER BANDWIDTH 2,000 kHz
- HIGH GAIN BANDWIDTH 20 MHz
- HIGH INPUT IMPEDANCE 100mΩ
- LOW OFFSET CURRENT 10nA
- TRUE OP AMP – CAN BE OPERATED NON-INVERTING OR INVERTING
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

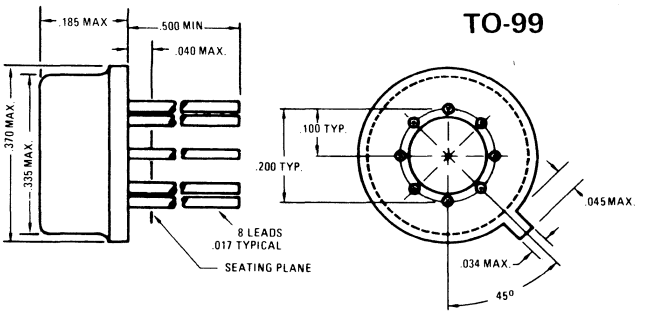
An operational amplifier with excellent D.C. characteristics, featuring high slew rate and fast settling time. Ideal for use in A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The HA-2520/22/25 is stable for closed loop gains greater than 3 without external compensation.

SCHEMATIC



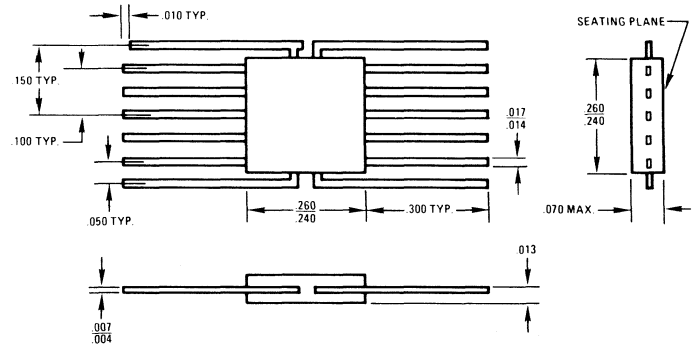
PACKAGES

TO-99



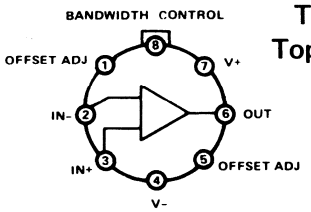
NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-86

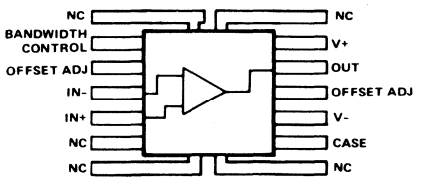


ALL DIMENSIONS IN INCHES

TO-99 Top View



TO-86



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

$V+ = +15V$ D.C., $V- = -15V$ D.C.

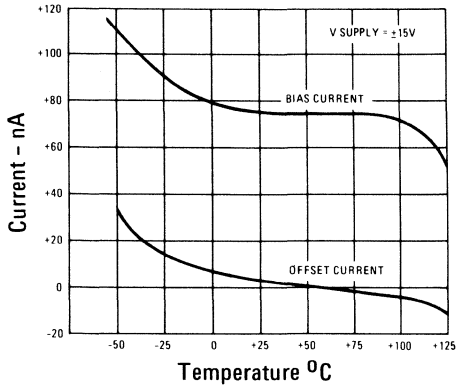
PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2525 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	150	2000		120	1600		120	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms page four.

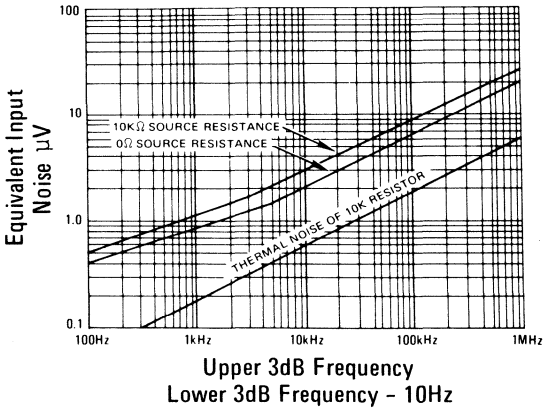
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

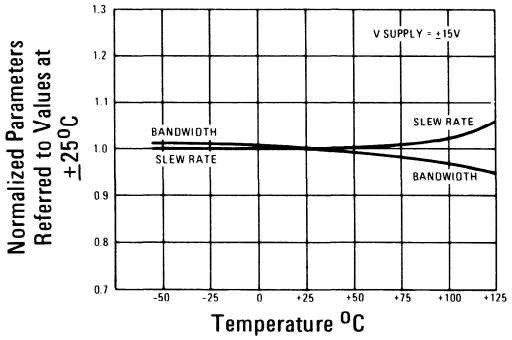
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



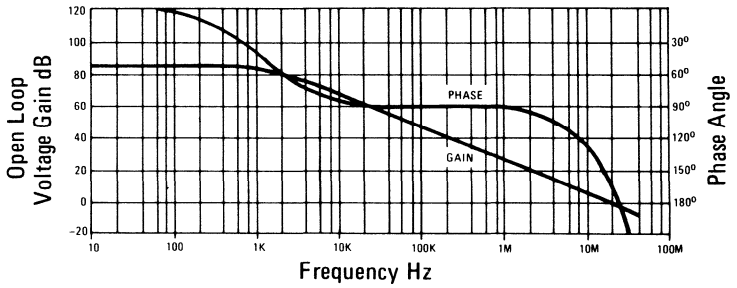
EQUIVALENT INPUT NOISE vs BANDWIDTH



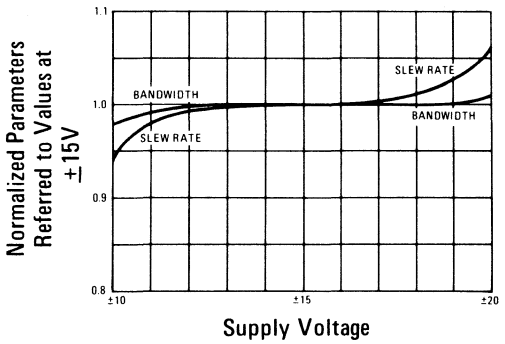
NORMALIZED AC PARAMETERS vs TEMPERATURE



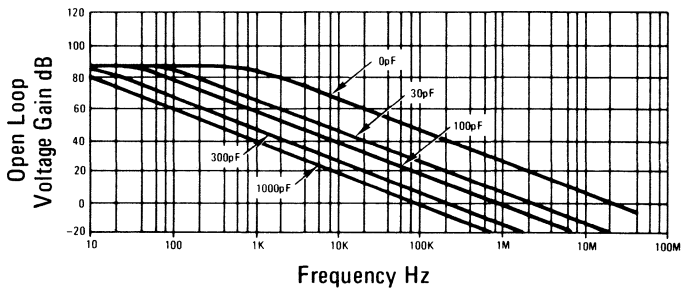
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



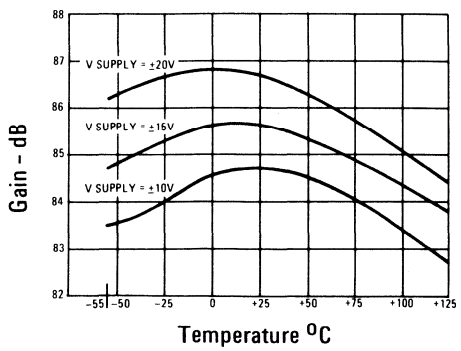
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



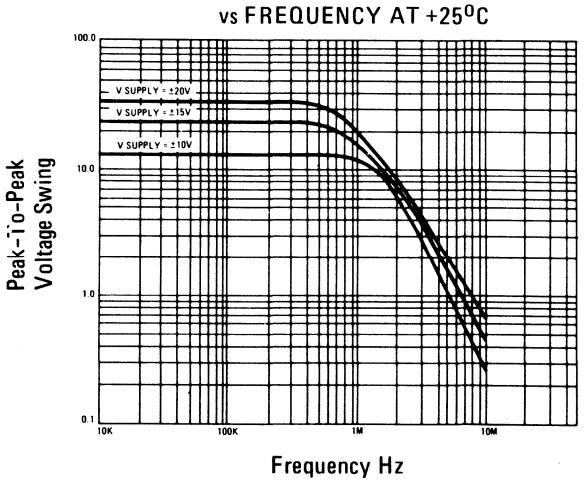
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

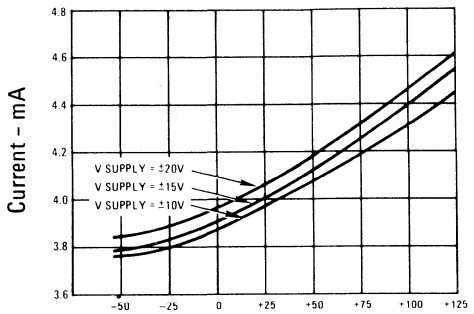


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

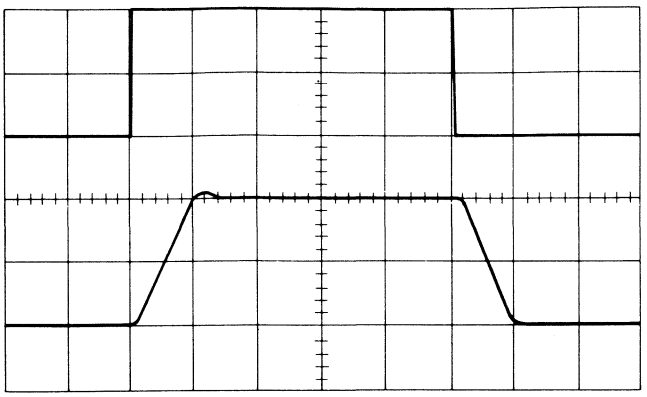


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



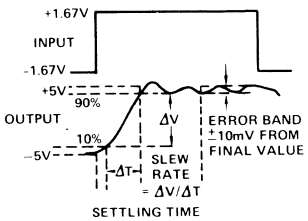
VOLTAGE FOLLOWER PULSE RESPONSE



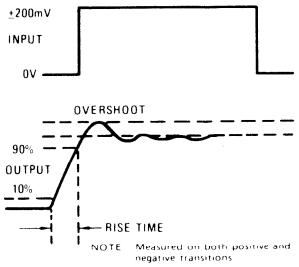
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.33V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

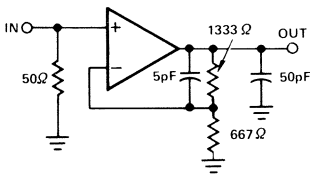
SLEW RATE AND SETTLING TIME



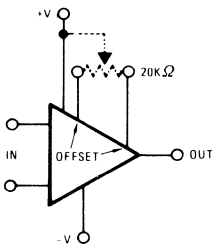
TRANSIENT RESPONSE



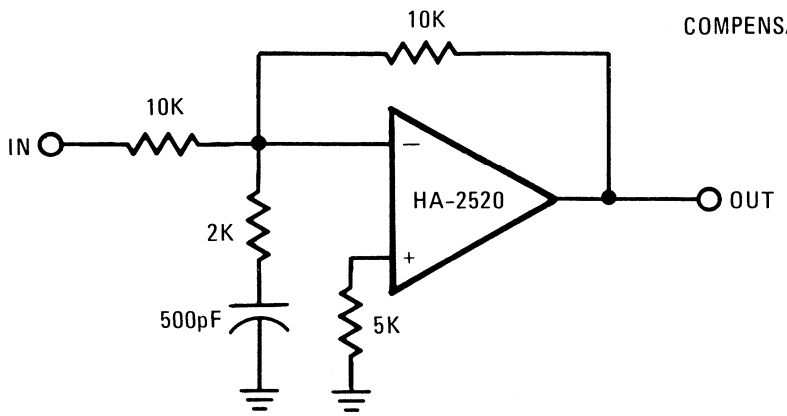
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN

Slew Rate	≈	120V/μs
Bandwidth	≈	10MHz
Settling Time	≈	500ns

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2600/02/05

High Impedance Operational Amplifier

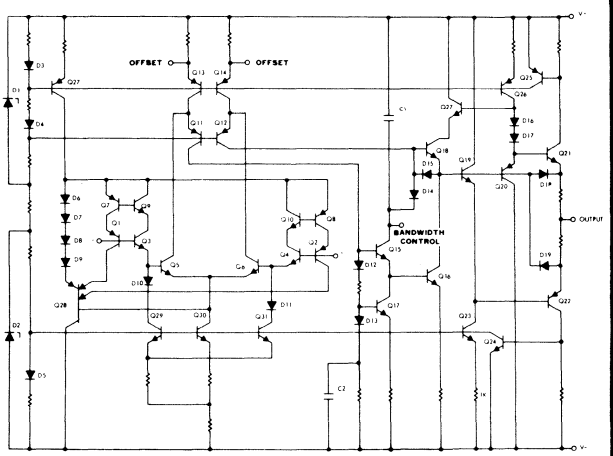
FEATURES

- HIGH INPUT IMPEDANCE
- LOW INPUT BIAS CURRENT
- LOW INPUT OFFSET CURRENT
- LOW INPUT OFFSET VOLTAGE
- HIGH GAIN
- HIGH SLEW RATE
- FAST RESPONSE TIME
- OUTPUT SHORT CIRCUIT PROTECTION
- MEETS OR EXCEEDS MIL-STD-883 REQUIREMENTS

GENERAL DESCRIPTION

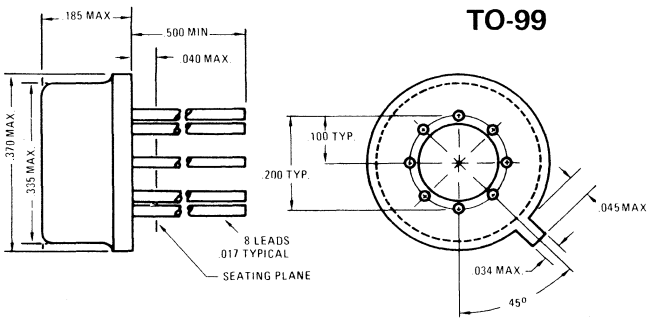
Internally compensated high impedance, high performance monolithic operational amplifier intended for use as a general purpose operational amplifier in precision instrumentation and signal processing.

SCHEMATIC



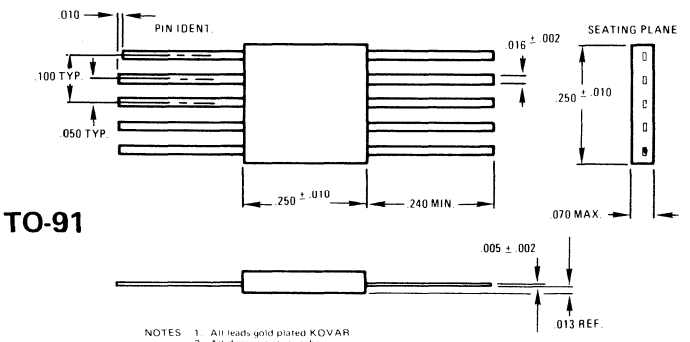
PACKAGES

TO-99



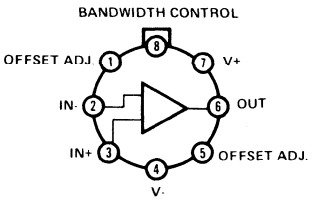
NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-91



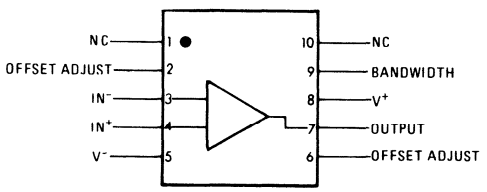
NOTES 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-99



(TOP VIEW)

TO-91



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

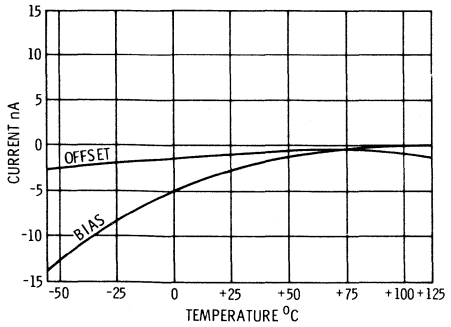
V+=+15VDC, V- = -15VDC

		HA-2600 −55°C to +125°C			HA-2602 −55°C to +125°C			HA-2605 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
Bias Current	+25°C		1	10		15	25		15	25	nA
	Full		10	30			60			40	nA
Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	±50	75		±50	75		±50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	40		25	40	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

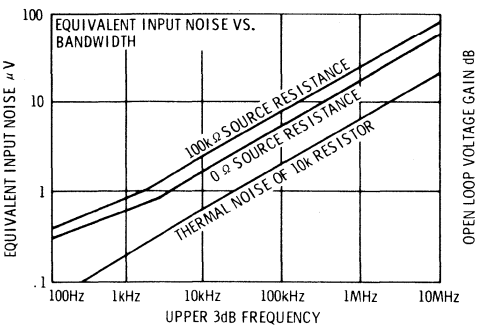
TEST CONDITIONS

NOTES:
1. R_L=2K
2. V_{CM}=±5.0V
3. V_O < 90mV
4. V_O=±10V
5. C_L= 100pF
6. V_O=±200mV
7. V_S = ±9.0V to ±15V
8. See transient response test circuits and waveforms page three.

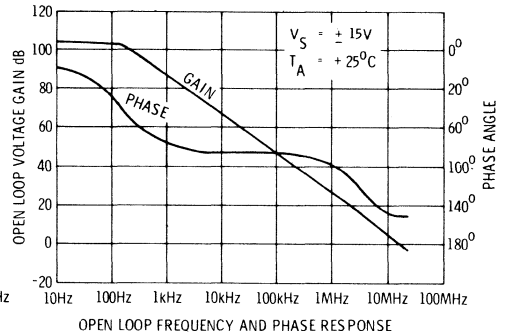
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



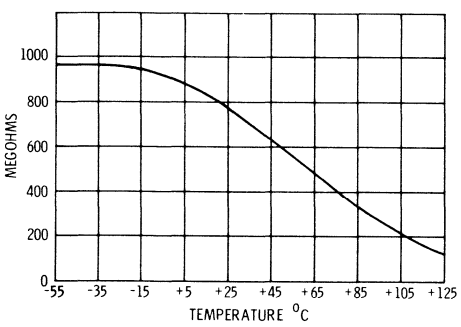
INPUT BIAS CURRENT AND OFFSET CURRENT
AS A FUNCTION OF TEMPERATURE



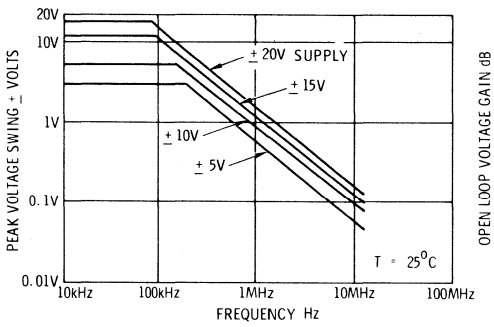
BROADBAND NOISE CHARACTERISTICS



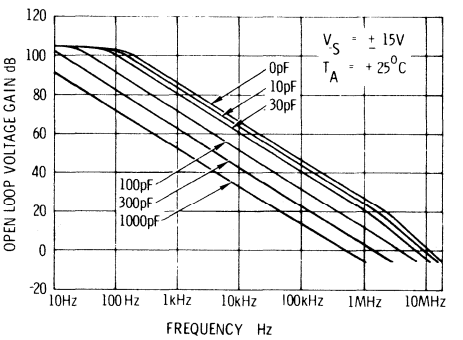
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

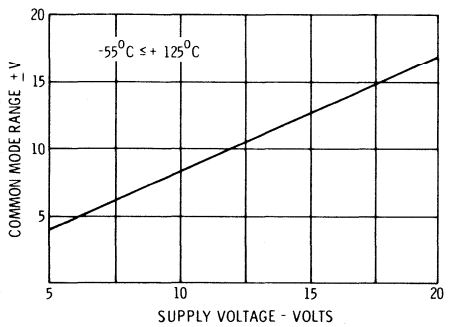


OUTPUT VOLTAGE SWING VS. FREQUENCY

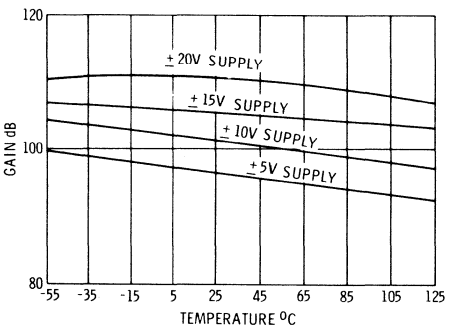


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

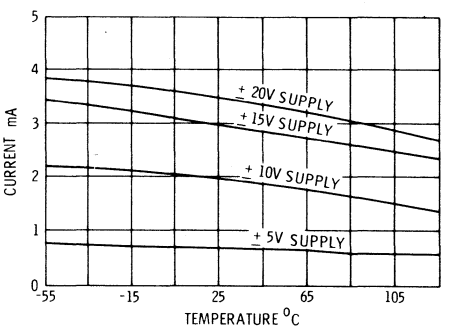
Note: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desired



COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE

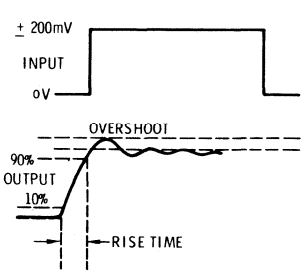


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE



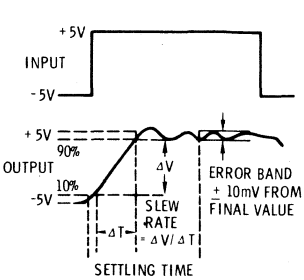
POWER SUPPLY CURRENT DRAIN
AS A FUNCTION OF TEMPERATURE

TRANSIENT RESPONSE

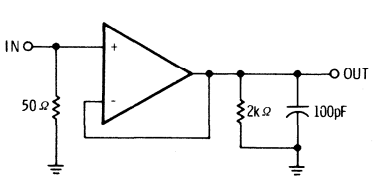


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

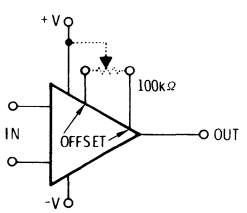
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE

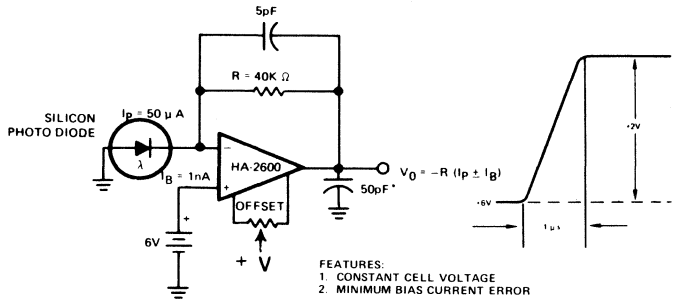


SUGGESTED OFFSET ZERO ADJUST HOOK-UP



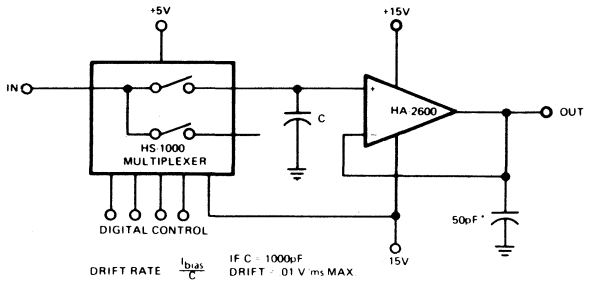
TYPICAL APPLICATIONS

PHOTO-CURRENT TO VOLTAGE CONVERTER



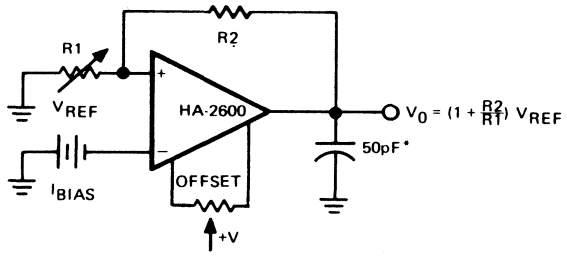
FEATURES:
1. CONSTANT CELL VOLTAGE
2. MINIMUM BIAS CURRENT ERROR

SAMPLE – AND – HOLD



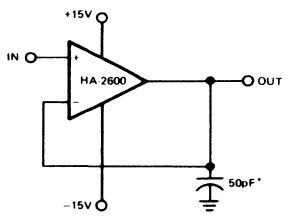
DRIFT RATE $\frac{I_{bias}}{C}$ IF C = 1000pF DRIFT = .01 V/ms MAX

REFERENCE VOLTAGE AMPLIFIER



FEATURES:
1. MINIMUM BIAS CURRENT IN REFERENCE CELL
2. SHORT CIRCUIT PROTECTION

VOLTAGE FOLLOWER



1.000 GAIN 0.9999
$Z_{in} = -10^{12}$ MIN.
Z_{out} = .01 MAX.
SLEW RATE = 4V/μs MIN.
B.W. = 12MHz TYP.
OUTPUT SWING = ± 10V MIN. TO 50kHz

*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3 dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $[180^o - (\Phi_1 - \Phi_2)]$ where Φ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity Φ_2 is the phase shift at a frequency much lower than the open-loop bandwidth.

SLEW RATE (Rate Limiting) – The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME – Time required for output waveform to remain within 0.1 percent of final value.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2620/2622/2625

Wide Band, High Impedance Operational Amplifiers

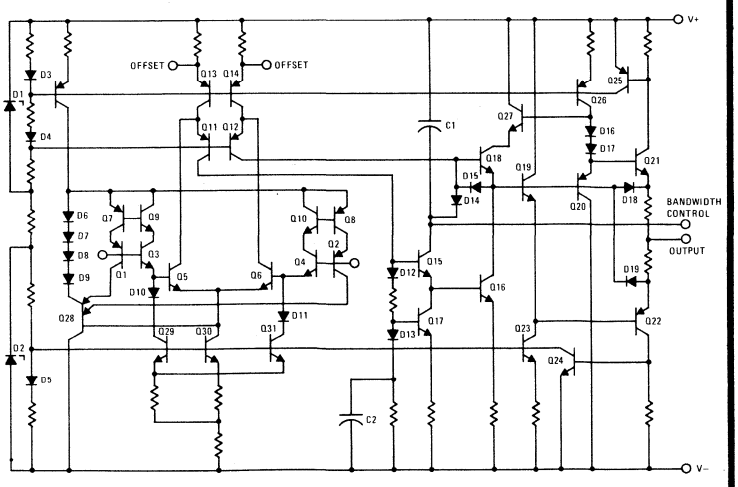
FEATURES

GAIN BANDWIDTH PRODUCT	100MHz
HIGH INPUT IMPEDANCE	500MΩ
LOW INPUT BIAS CURRENT	1nA
LOW INPUT OFFSET CURRENT	1nA
LOW INPUT OFFSET VOLTAGE	1mV
HIGH GAIN	150K
HIGH SLEW RATE	35V/μs
OUTPUT SHORT CIRCUIT PROTECTION	

GENERAL DESCRIPTION

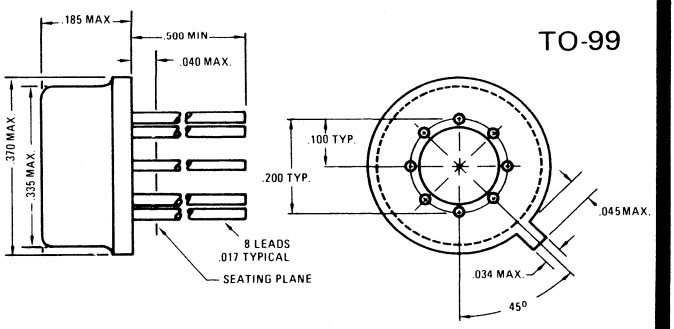
The HA-2620 family of operational amplifiers has very low input bias current and intended for use as high impedance comparators and wide band amplifiers. The HA-2620 family features very high gain, very high slew rate and output short circuit protection. The HA-2620 and HA-2622 operate over the full military temperature range from -55°C to +125°C. The HA-2625 operates over the temperature range of 0°C to +75°C.

SCHEMATIC



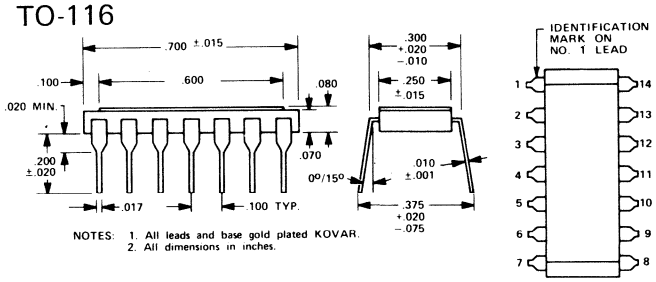
PACKAGES

TO-99



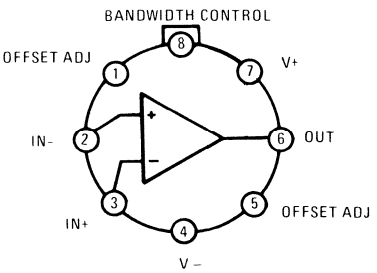
NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

TO-116

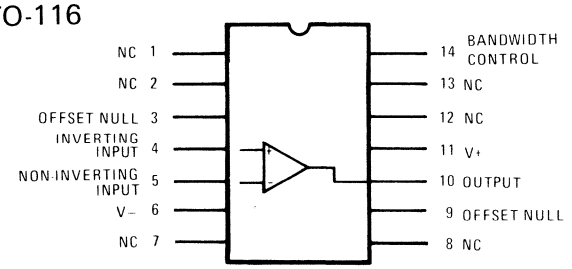


NOTES: 1. All leads and base gold plated KOVAR.
2. All dimensions in inches.

TO-99



TO-116



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

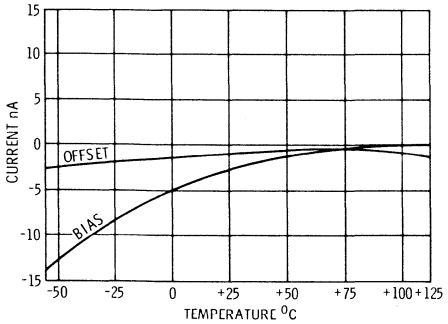
$V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	HA-2620 TYP.	HA-2620 MAX.	HA-2622 −55°C to +125°C MIN.	HA-2622 TYP.	HA-2622 MAX.	HA-2625 0°C to +75°C MIN.	HA-2625 TYP.	HA-2625 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3 & 7)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 5, 7 & 8)	+25°C		17	45		17	45		17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

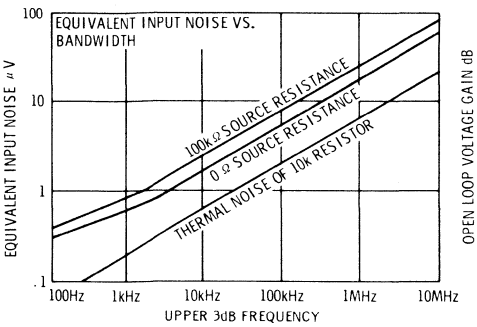
NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms page 3.
8. $A_V = 5.0V$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $V_{Sup} = \pm 9.0V$ to $\pm 15.0V$
10. $V_O = 5.0V$

TYPICAL PERFORMANCE CURVES

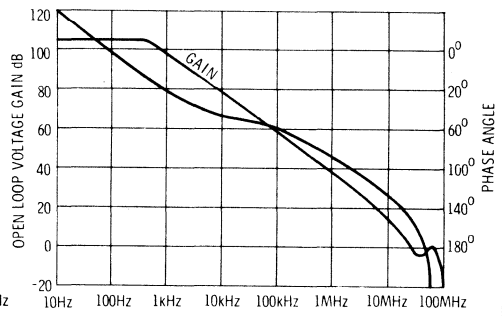
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



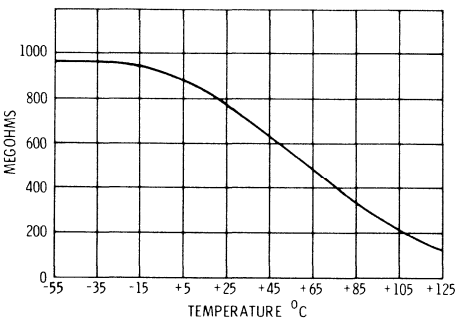
INPUT BIAS CURRENT AND OFFSET CURRENT-
AS A FUNCTION OF TEMPERATURE



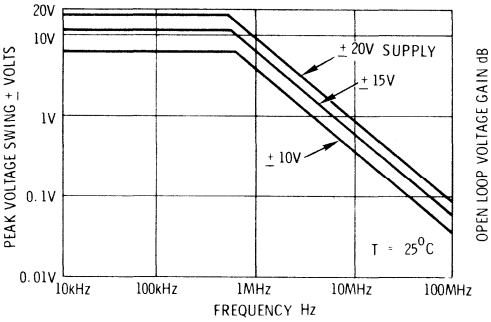
BROADBAND NOISE CHARACTERISTICS



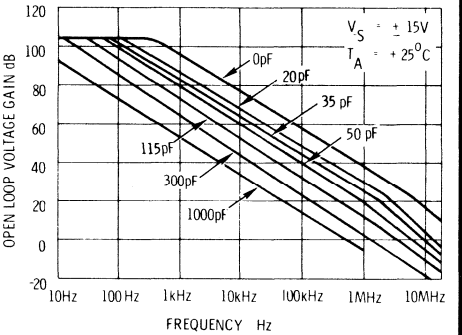
OPEN LOOP FREQUENCY AND PHASE RESPONSE



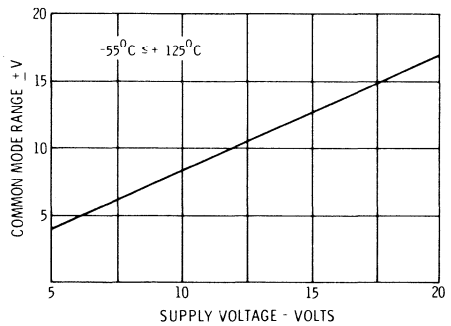
INPUT IMPEDANCE VS. TEMPERATURE, 100Hz



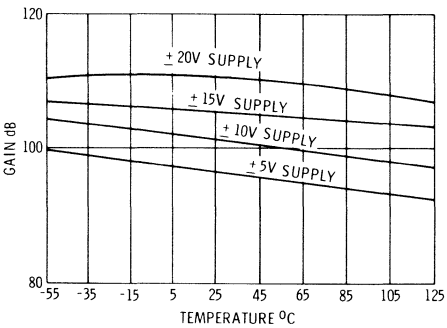
OUTPUT VOLTAGE SWING VS. FREQUENCY



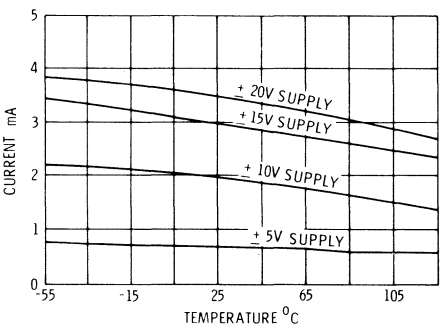
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE

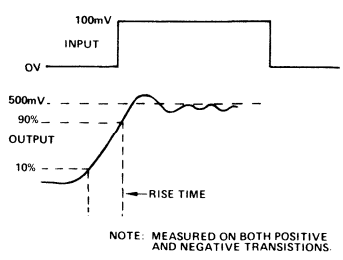


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

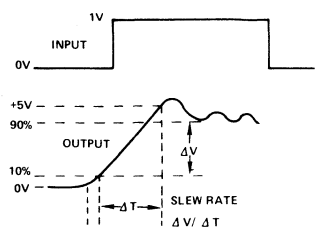


POWER SUPPLY CURRENT DRAIN
AS A FUNCTION OF TEMPERATURE

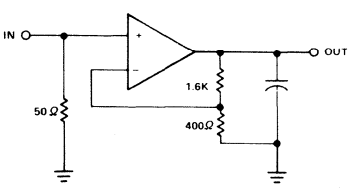
TRANSIENT RESPONSE



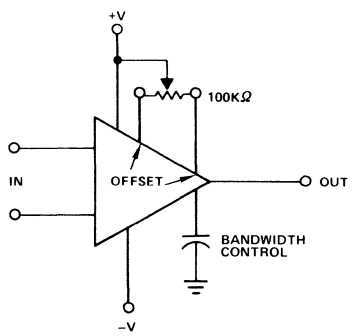
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE

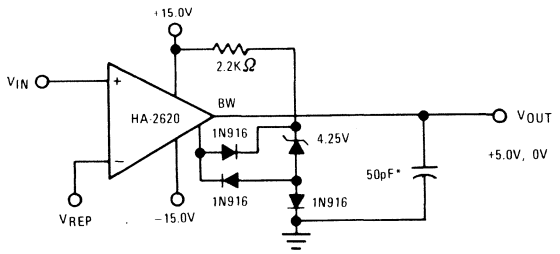


SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP

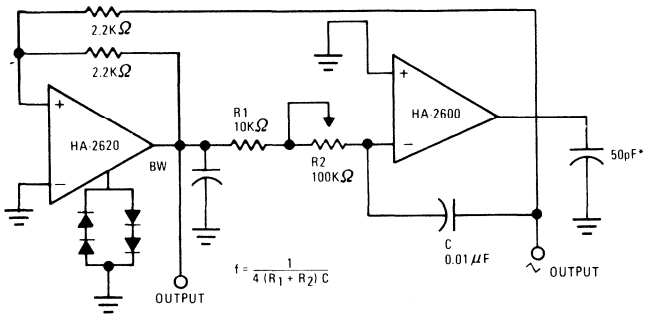


TYPICAL APPLICATIONS

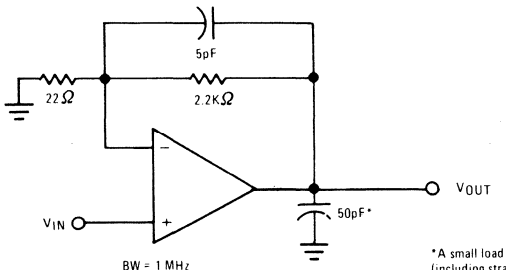
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2700/2704/2705

High Performance Operational Amplifiers

LINEAR DATA

FEATURES

• HIGH SLEW RATE	20V/μs	• HIGH CM_{rr}	106dB
• LOW POWER DISSIPATION	2.25mW AT ±15.0V	• WIDE POWER SUPPLY RANGE	±5.5V TO ±20.0V
• HIGH OPEN LOOP GAIN	2 MILLION (R_L = 2KΩ)	• FULLY INTERNALLY COMPENSATED	
• LOW INPUT BIAS CURRENT	5nA	• OUTPUT SHORT CIRCUIT PROTECTED	
• LOW OFFSET VOLTAGE	0.5mV	• OFFSET NULL CAPABILITY	

GENERAL DESCRIPTION

The HA-2700 is a general purpose amplifier which utilizes a revolutionary input circuit concept that makes possible operation at very low power levels without compromising large signal response characteristics or output drive capability. Advanced circuit design techniques and the use of vertical NPN and PNP transistors make possible the attainment of very high gain with a single stage of voltage amplification, thus ensuring closed loop stability even in the critical unity gain follower mode, without the use of external compensation components.

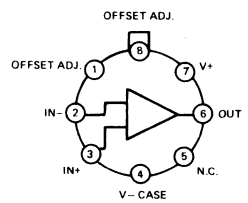
The circuit is intended for use in applications that require fast large signal response with low power dissipation and for instrumentation applications in which low offset voltage, current drift, large voltage gain and high common mode rejection are necessary. Full output short circuit protection and the large differential input breakdown enable the device to withstand a variety of fault conditions.

PACKAGES

CONNECTION DIAGRAMS

TO-99:

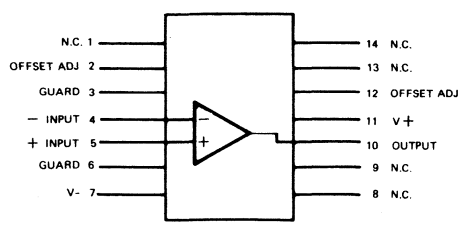
HA2-2700/HA2-2704/HA2-2705



(TOP VIEW)

TO-116:

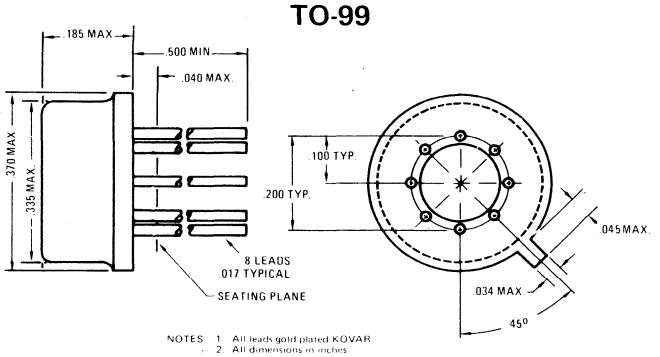
HA1-2700/HA1-2704/HA1-2705



(TOP VIEW)

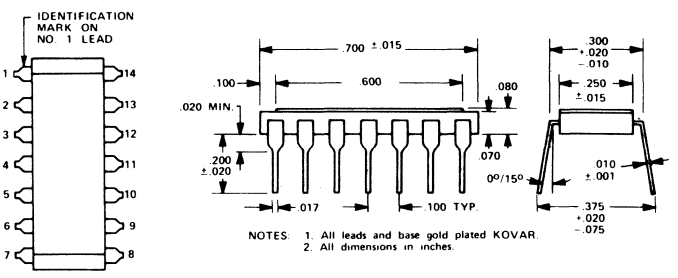
PHYSICAL DIMENSIONS

TO-99



NOTES: 1. All leads gold plated KOVAR.
2. All dimensions in inches.

TO-116



NOTES: 1. All leads and base gold plated KOVAR.
2. All dimensions in inches.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±18.0V
Internal Power Dissipation	300mW
Storage Temperature	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

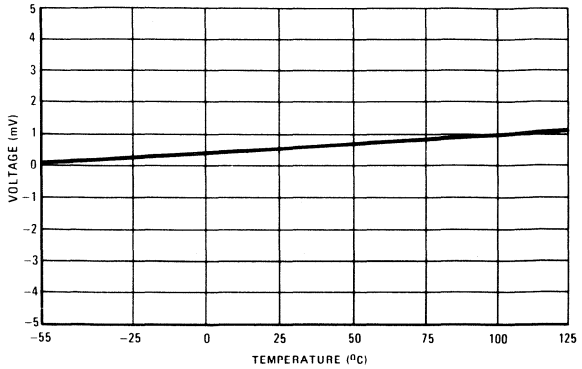
$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

		HA-2700 −55°C to +125°C			HA-2704 −25°C to +85°C			HA-2705 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	3.0		0.5	3.0		1.0	5.0	mV
	Full			5.0			6.0			7.0	mV
Bias Current	+25°C		5.0	20.0		5.0	20.0		5.0	40.0	nA
	Full			50.0			50.0			70.0	nA
Offset Current	+25°C		2.5	10.0		2.5	10.0		2.5	15.0	nA
	Full			30.0			30.0			40.0	nA
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	400K	2M		400K	2M		200K	2M		V/V
	Full	150K			200K			150K			V/V
Common Mode Rejection Ratio (Note 4)	Full	86	106		86	106		80	106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12.0	±13.0		±12.0	±13.0		±12.0	±13.0		V
	Full	±11.0			±11.0			±11.0			V
Output Current (Note 3)	+25°C		22			22			22		mA
TRANSIENT RESPONSE CHARACTERISTICS											
Slew Rate (Notes 2 & 6)	+25°C	10	20		10	20		10	20		V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		75	150		75	150		75	150	µA
Power Supply Rejection Ratio (Note 5)	Full	86	100		86	100		80	100		dB

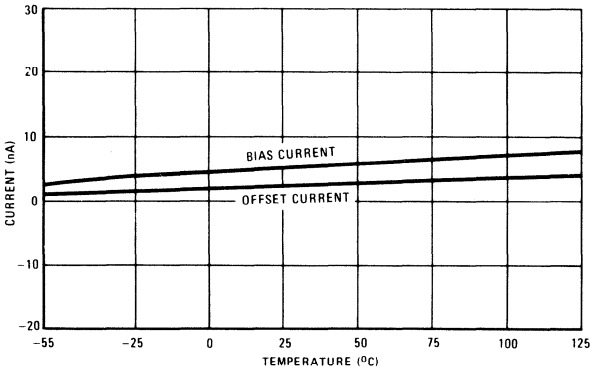
NOTES:
1. Can be adjusted to zero with 1 megohm pot between Pins 1 and 8 with the tap to Pin 7.
2. $R_L = 2K$, $C_L = 100pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_S = \pm 10.0V$ to $\pm 20.0V$
6. Noninverting unity gain; output voltage swing is 10.0V.

TYPICAL PERFORMANCE CURVES

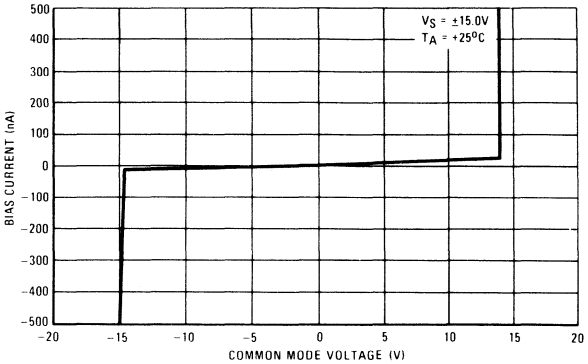
OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



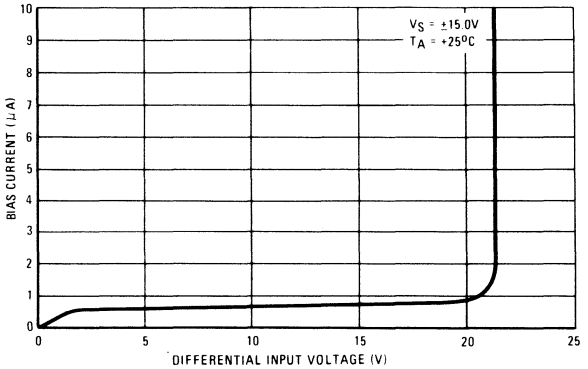
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



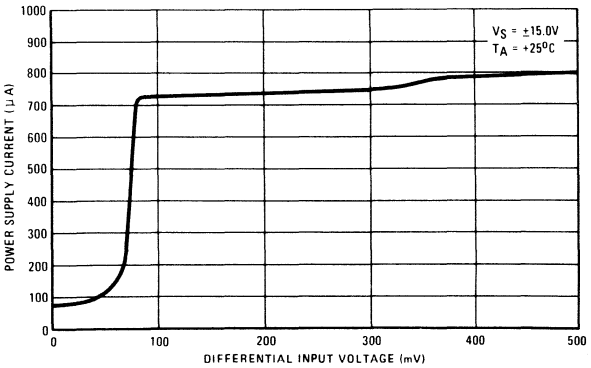
BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



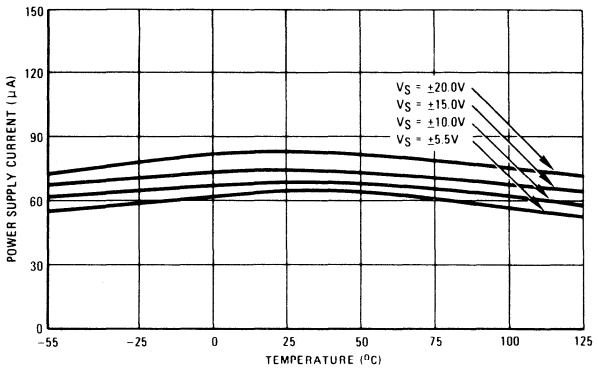
BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



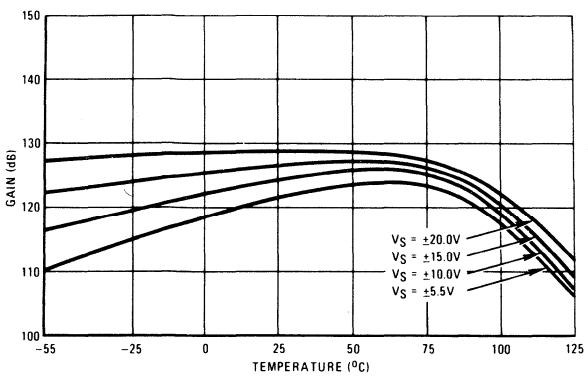
POWER SUPPLY CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



POWER SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

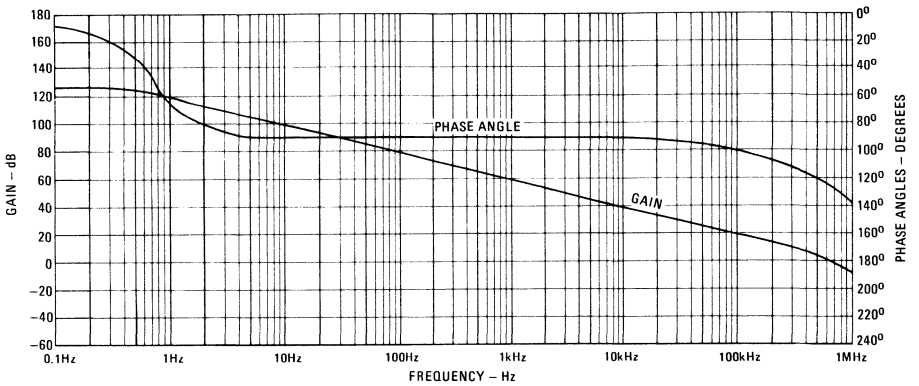


VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



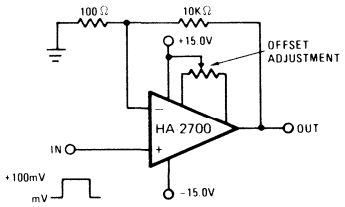
TYPICAL PERFORMANCE CURVES (continued)

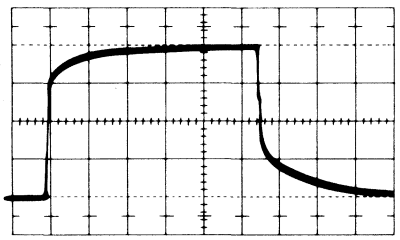
PHASE-FREQUENCY RESPONSE FOR THE HA-2700



TYPICAL APPLICATIONS

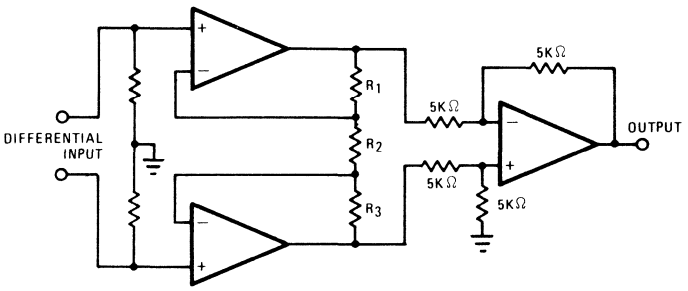
HIGH GAIN AMPLIFIER (100 V/V)





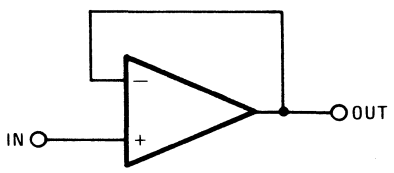
SCALE
Horizontal – 20μs/division
Vertical – 5.0V/division

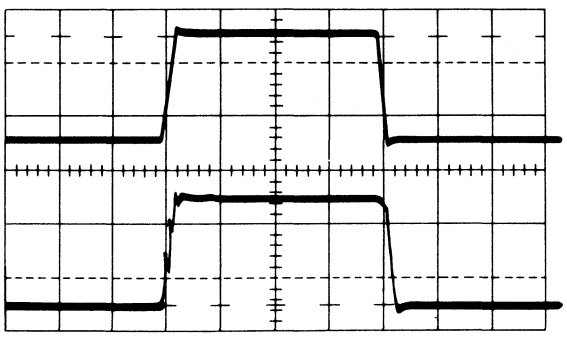
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



THE GAIN IS GIVEN BY: $\frac{(R_1 + R_2 + R_3)}{R_2} = G$

UNITY GAIN VOLTAGE FOLLOWER





Non-inverting unity gain with a 2KΩand 100pF load
TOP: V_{IN} = 10.0V Peak to Peak
BOTTOM: V_{OUT}
SCALE: Horizontal -1 μs/division
Vertical -5.0V/division

NOTE: Faster increase rise and fall time and increase distortion on output wave form.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2800/2805

Locked Loop

FEATURES

- FREQUENCY RANGE 5 MHz TO 25 MHz
- INDEPENDENT PHASE DETECTOR AND OSCILLATOR FOR VERSATILITY
- TWO ISOLATED PHASE DETECTOR OUTPUTS
- TTL/ECL COMPATIBLE OSCILLATOR OUTPUT
- OSCILLATOR STABILITY: 250ppm/^{0}C, 0.1%/V
- MEETS MIL-STD-883 REQUIREMENTS

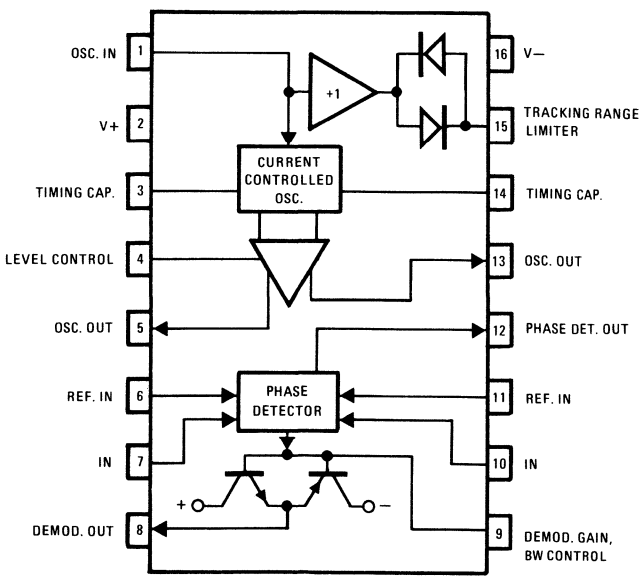
DESCRIPTION

The HA-2800/2805 Phase Locked Loop is useful for many operations in the frequency domain. It features a number of functional and parametric improvements over other similar monolithic circuits.

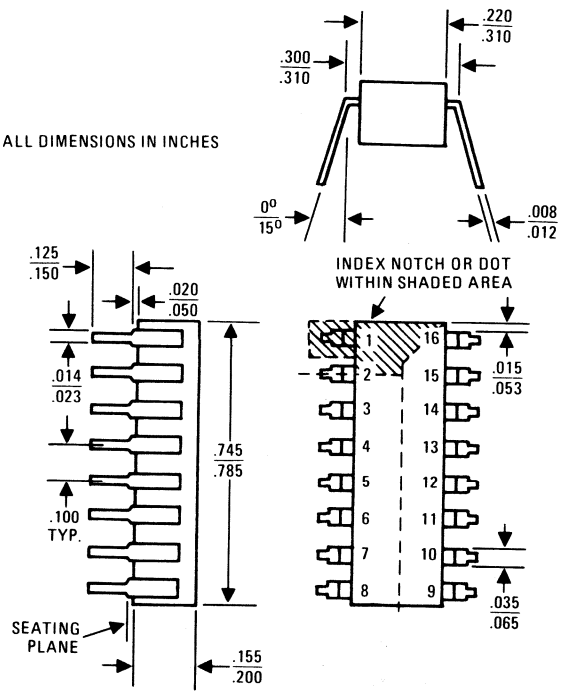
A major feature is a high impedance current source phase detector output with provisions for external connection to the oscillator input which is a low impedance current sink. This allows connection of complex passive or active filters, amplifiers, sweep circuits, etc. within the loop. Also, the two phase detector outputs are isolated from one another so that different filter functions can be connected at the two outputs without interaction. The capability of independently adjusting loop bandwidth and demodulated output bandwidth allows phase modulation detectors to be constructed.

Applications include modulators and demodulators for F.M., phase modulation, and F.S.K.; frequency multiplication; data synchronization; tracking filters; and frequency synthesizers.

FUNCTIONAL DIAGRAM



PACKAGE



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V– Terminals: 30 Volts (Note 5)
Input Voltage: 2 VRMS
Output Current, pin 5 & 13: 10mA
Power Dissipation: 500mW

Operating Temperature:
$-55^0 > T_A > +125^0$ C(HA–2800)
$0^0 > T_A > +75^0$ C(HA–2805)
Storage Temperature:
$-65^0 > T_A > +150^0$C

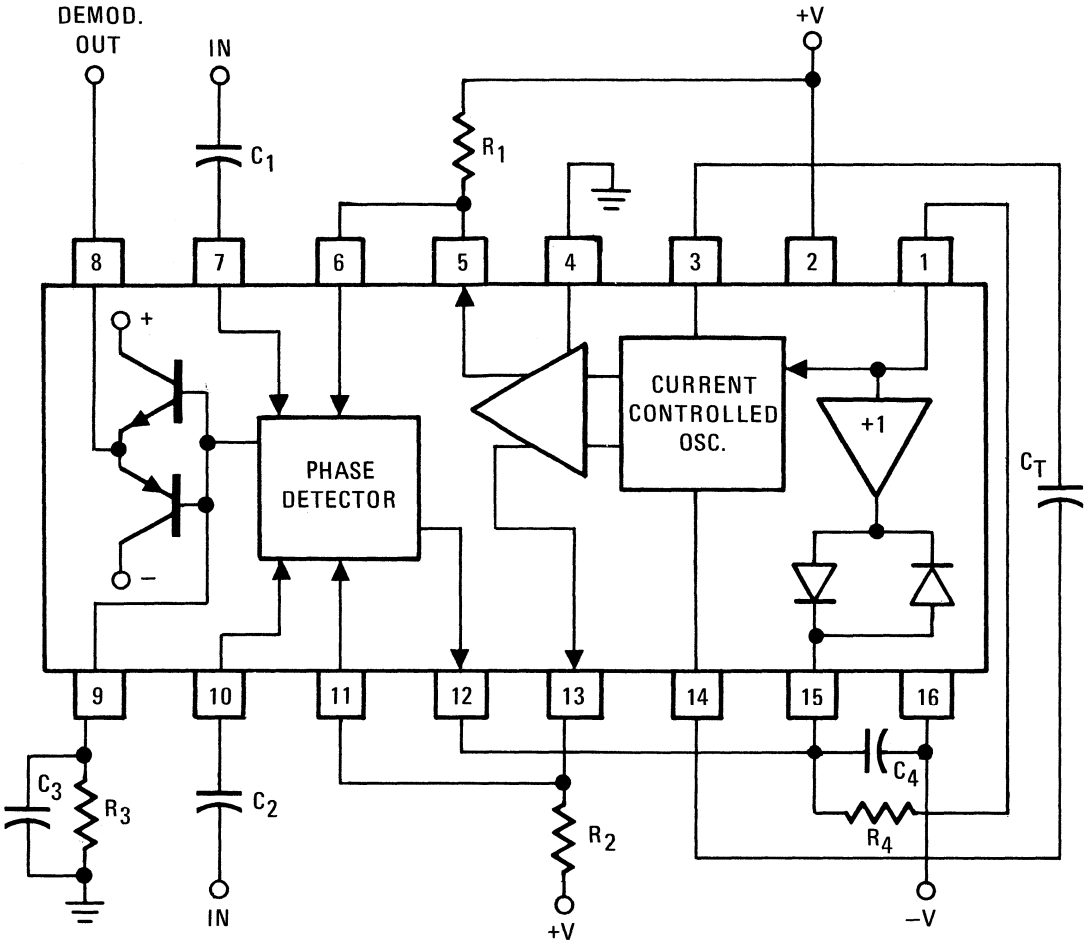
ELECTRICAL CHARACTERISTICS

V+= +5 Volts V–= –15 Volts Pin 4= Ground
(unless otherwise stated)

PARAMETER	TEMP.	HA-2800 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2805 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
PHASE DETECTOR								
Input Impedance, Pins 7 - 10	+25°C		2K			2K		Ω
Input Voltage Range, Pins 7 - 10	Full	.02		400	.02		400	m VRMS
Output Impedance, Pins 9 & 12	+25°C		8			8		MΩ
Output Offset Current, Pins 9 & 12	+25°C			30			40	μA
Output Offset Current, Pins 9 & 12	Full			40			50	μA
Conversion Gain, Pins 9 & 12 (Note 1)	+25°C			50		50		μA/Radian
CURRENT CONTROLLED OSCILLATOR								
Maximum Frequency (Note 6)	Full	25	30		20	30		MHz
Frequency Drift (Note 2)	Full		250			250		ppm/°C
Frequency Change with Supply Voltage (Note 2)	Full		0.1			0.1		%/V
Input Resistance, Pin 1	+25°C		850			850		Ω
Input Open Circuit Voltage, Pin 1	+25°C		-10			-10		V
Clipping Level, Pin 15 (with resp. to pin 1 voltage)	+25°C		±0.7			±0.7		V
Conversion Gain (Note 2)	+25°C		1.0			1.0		%Δf/μA
Output Voltage, High (Note 2)	+25°C	+1.9			+1.9			V
Output Voltage, Low (Note 2)	+25°C			+.72			+.72	V
Output Rise Time (Note 2)	+25°C		50			50		ns
Output Fall Time (Note 2)	+25°C		30			30		ns
CLOSED LOOP CHARACTERISTICS (NOTE 1, 2, 3)								
Loop Gain	+25°C		50			50		%Δf/Radian
Tracking Range	+25°C		50			50		%Δf
Demod. Output Swing, Pin 8	+25°C		± 150			± 150		mV
Frequency Drift (Note 4)	Full		250			250		ppm/°C
POWER SUPPLY CHARACTERISTICS								
Supply Current; V+	Full		8.0	11.5		8.0	11.5	mA
Supply Current; V–	Full		8.0	11.5		8.0	11.5	mA
Supply Voltage Range (Note 5)	Full	±5		±15	±5		±15	V

NOTES:
1. V_{IN} = 10mV RMS, balanced to ground, 10MHz; C1 = C2 = .01μF.
2. C_T = 200pF, R1 = R2 = 5KΩ; $f_o \approx$ 10MHz.
3. R3 = 10KΩ, R4 = 10KΩ; f_{in} swept about 10MHz.
4. See guaranteed temperature drift curve, page 3.
5. Device should not be operated with either power supply absent. Supplies should be decoupled close to the device with at least 0.1μF capacitors.
6. The HA-2820/2825 is recommended for operation at frequencies less than 5 MHz.

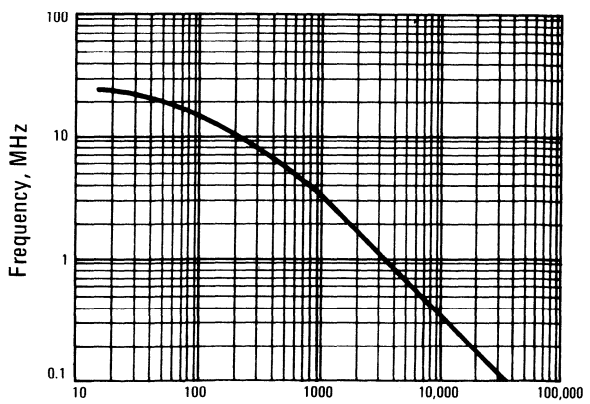
TEST CIRCUIT



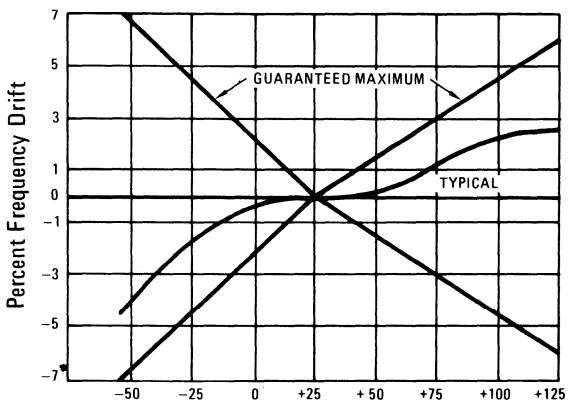
Unless otherwise specified, V+= +5 Volts; V−= −15 Volts; R1=R2= 5KΩ; R3= 10KΩ; R4= 10KΩ; C1=C2= .01 μF; C3=C4= .002 μF; $C_T \approx 200$ pF (f_o=10 MHz); V_{in}= 10m VRMS; $T_A = +25^{\circ}$ C.

PERFORMANCE CURVES

CENTER FREQUENCY, f_0 vs. TIMING CAPACITOR, C_t

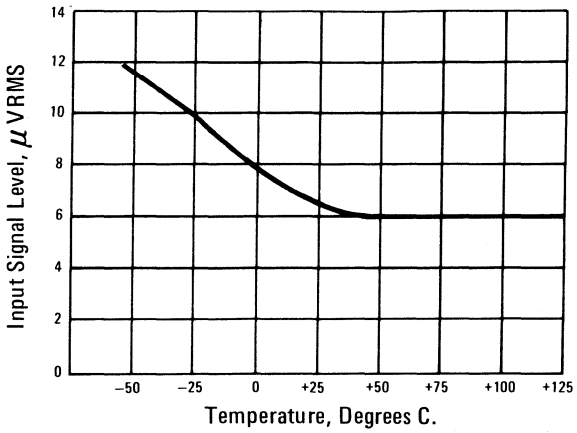


CENTER FREQUENCY DRIFT vs. TEMPERATURE

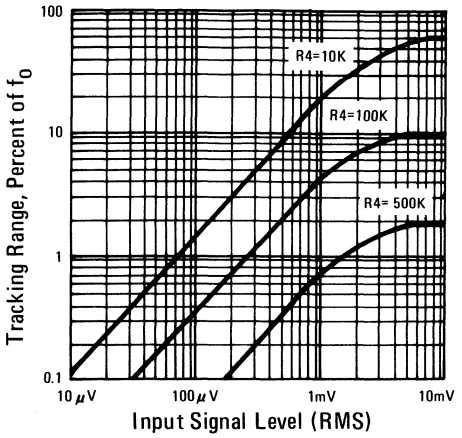


PERFORMANCE CURVES (continued)

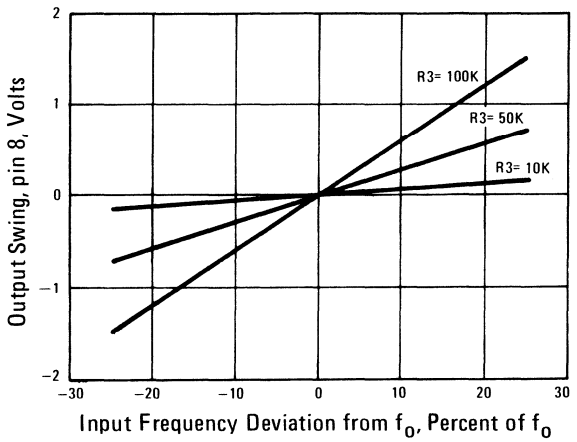
MINIMUM INPUT SIGNAL TO MAINTAIN LOCK
vs. TEMPERATURE



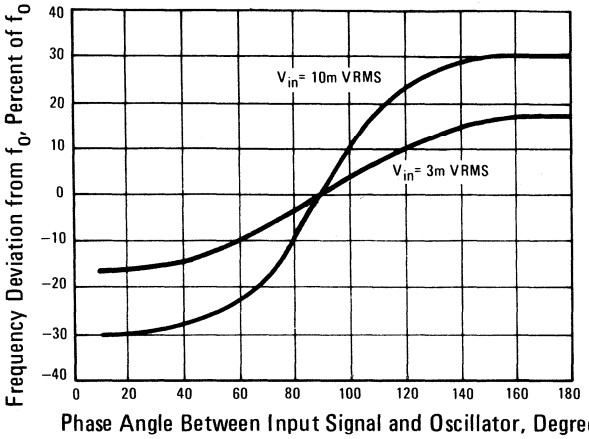
TRACKING RANGE
vs. INPUT SIGNAL LEVEL



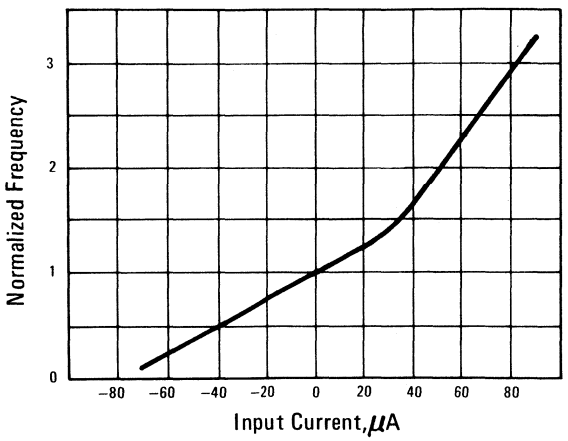
DEMODULATED OUTPUT SWING
vs. INPUT FREQUENCY DEVIATION



LOOP GAIN
CHARACTERISTIC



OSCILLATOR FREQUENCY
vs. INPUT CURRENT, PIN 1



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HA-2825

Phase Locked Loop

LINEAR DATA

FEATURES

- FREQUENCY RANGE 0.01 Hz TO 3 MHz
- INDEPENDENT PHASE DETECTOR AND OSCILLATOR FOR VERSATILITY
- TWO ISOLATED PHASE DETECTOR OUTPUTS
- DTL/TTL COMPATIBLE OSCILLATOR OUTPUT
- OSCILLATOR STABILITY: 100ppm/^{0}C, 0.1%/VOLT

DESCRIPTION

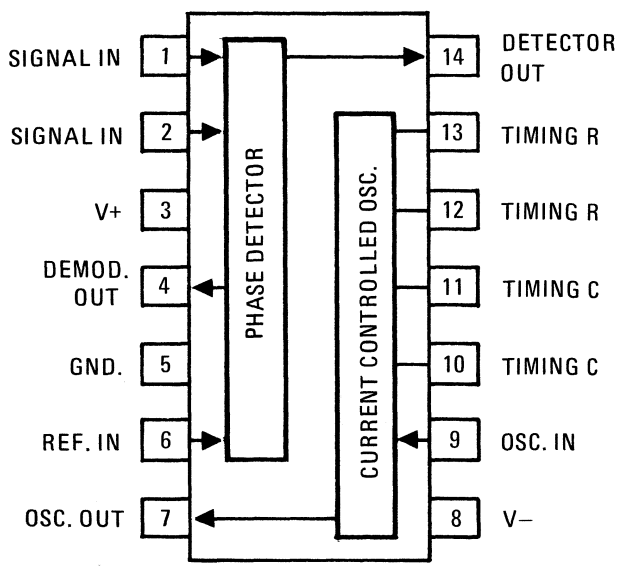
The HA-2825 Phase Locked Loop is useful for many operations in the frequency domain in the sub-audio to low R.F. bands. It features a number of functional and parametric improvements over other similar monolithic circuits.

A major feature is a high impedance current source phase detector output with provisions for external connection to the oscillator input which is a low impedance current sink. This allows connection of complex passive or active filters, amplifiers, sweep circuits, etc. within the loop. Also, the two phase detector outputs are isolated from one another so that different filter functions can be connected at the two outputs without interaction. The capability of independently adjusting loop bandwidth and demodulated output bandwidth allows phase modulation detectors to be constructed.

Applications include modulators and demodulators for F.M., phase modulation, and F.S.K.; frequency multiplication; data synchronization; tracking filters; and speed controls.

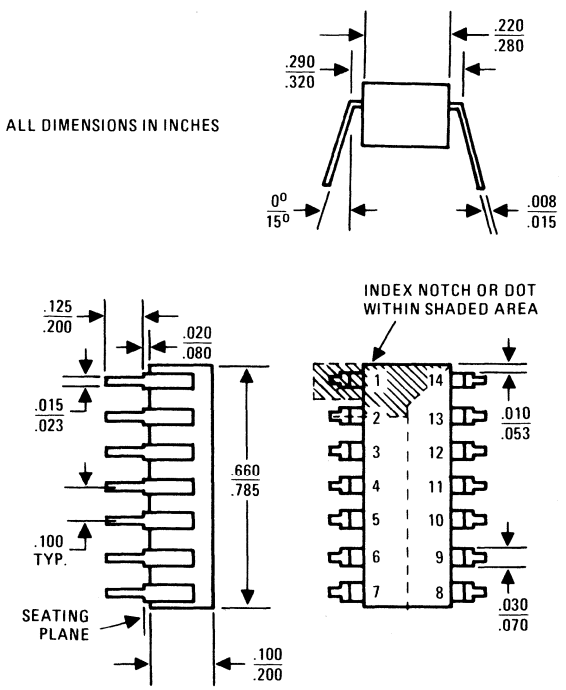
FUNCTIONAL DIAGRAM

(TOP VIEW)



PACKAGE

ALL DIMENSIONS IN INCHES



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	30.0V (Note 3)	Power Dissipation	300mW
Input Voltage	2 VRMS	Operating Temperature	$0^{o}C > T_A > +75^{o}C$
Output Current, Pin 7	10mA	Storage Temperature	$-65^{o}C > T_A > +150^{o}C$

ELECTRICAL CHARACTERISTICS

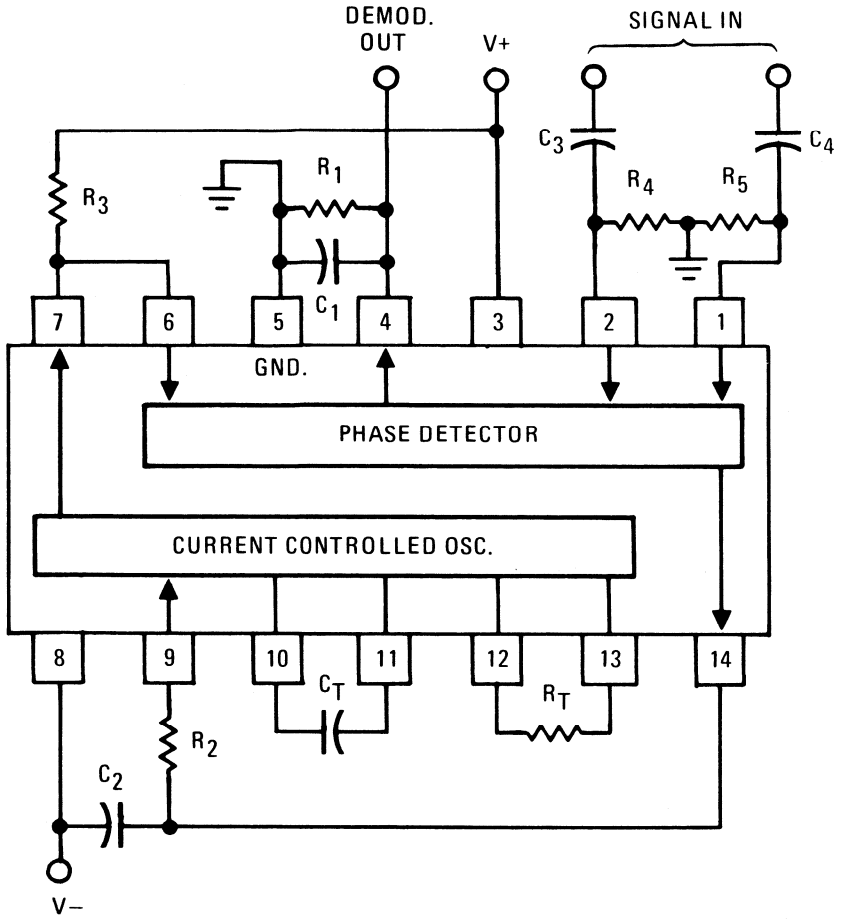
V+ = +6.0V
V- = -6.0V
Pin 5 = Ground
V_{IN} = 100mV RMS
$F_0 \approx$ 50kHz
See Test Circuit, Page 3

} Unless otherwise specified

PARAMETER	TEMP.	0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
PHASE DETECTOR					
Input Impedance, Pins 1 - 2	+25°C		100K		Ω
Input Voltage Range, Pins 1 - 2 (Note 1)	Full	10	5		mV RMS
Output Impedance, Pins 4 & 14	+25°C		10		MΩ
Output Offset Current, Pins 4 & 14	+25°C		10	15	μA
Output Offset Current, Pins 4 & 14	Full			20	μA
Conversion Gain, Pins 4 & 14	+25°C		50		μA/Radian
CURRENT CONTROLLED OSCILLATOR					
Maximum Frequency	Full	3	5		MHz
Frequency Drift	Full		100		ppm/°C
Frequency Change with Supply Voltage	Full		0.1		%/V
Input Resistance, Pin 9	+25°C		500		Ω
Input Open Circuit Voltage, Pin 9	+25°C		-3.5		V
Conversion Gain	+25°C		1.0		% Δf/μA
Output Voltage, High	+25°C	+1.9			V
Output Voltage, Low	+25°C			+0.4	V
Output Rise Time	+25°C		100		ns
Output Fall Time	+25°C		125		ns
CLOSED LOOP CHARACTERISTICS					
Loop Gain	+25°C		50		% Δf/Radian
Tracking Range	+25°C		50		%Δf
Demod. Output Swing, Pin 4	+25°C		±700		mV
Frequency Drift	Full		100		ppm/°C
POWER SUPPLY CHARACTERISTICS					
Supply Current, V+	Full		3	5	mA
Supply Current, V-	Full		7	10	mA
Supply Voltage Range (Notes 2, 3)	Full	±6		±12	V

NOTES: 1. For ±10% tracking range.
2. +5.0V, -7.0V may be used alternatively.
3. Device should not be operated in the absence of either power supply. Supply lines should be decoupled near the device with at least 0.1 μF capacitors.

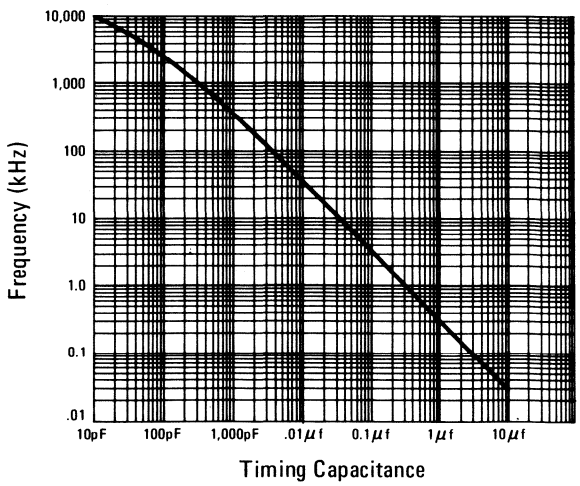
TEST CIRCUIT



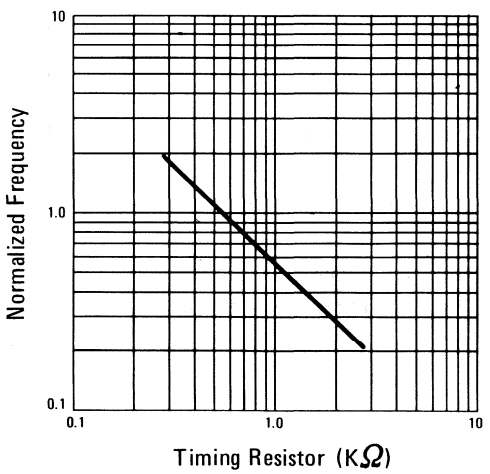
Unless otherwise specified: V+ = +6.0V; V- = -6.0V; $R_1 = R_3 = 10K\Omega$; $R_2 = 1K\Omega$; $R_4 = R_5 = 300\Omega$; $R_T = 540\Omega$; $C_1 = .015\mu f$; $C_2 = C_3 = C_4 = 0.1\mu f$; $C_T = 0.01\mu f$ ($f_o \approx 50kHz$); $V_{IN} = 100mV$ RMS; $T_A = +25^oC$

PERFORMANCE CURVES

CENTER FREQUENCY, f_o vs.
TIMING CAPACITOR, C_T ($R_T = 540\Omega$)

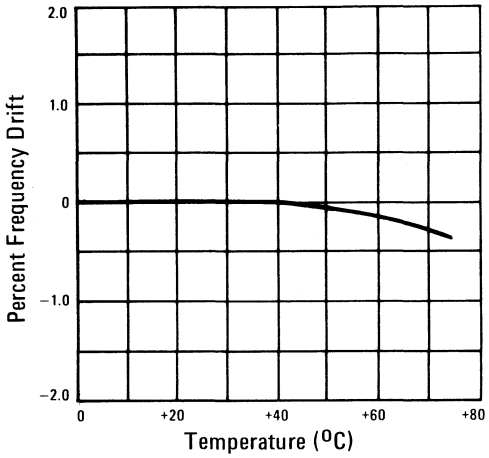


CENTER FREQUENCY, f_o vs.
TIMING RESISTOR, R_T ($C_T = .01\mu f$)

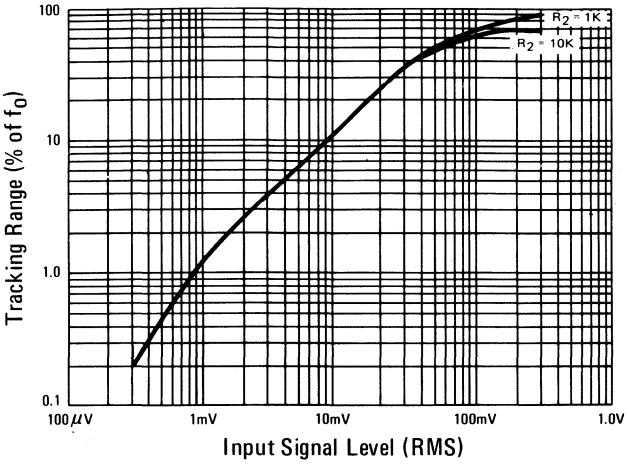


PERFORMANCE CURVES (continued)

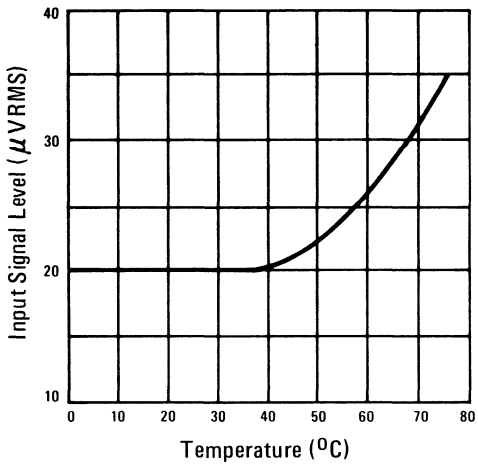
CENTER FREQUENCY DRIFT vs. TEMPERATURE



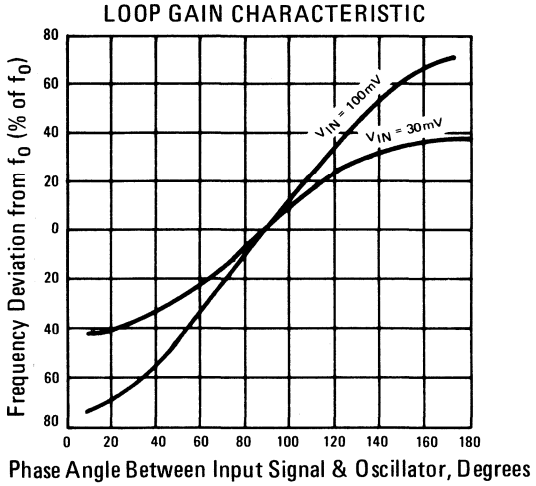
TRACKING RANGE vs. INPUT SIGNAL LEVEL



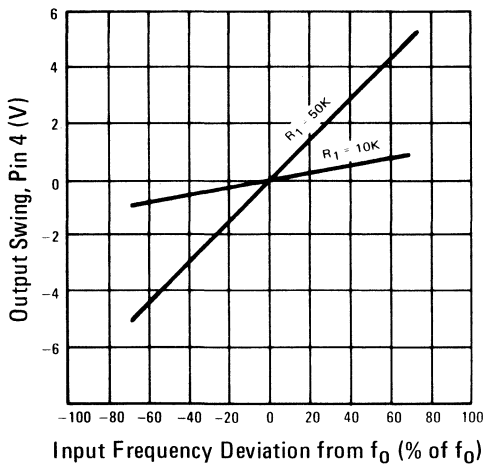
MINIMUM SIGNAL TO MAINTAIN LOCK



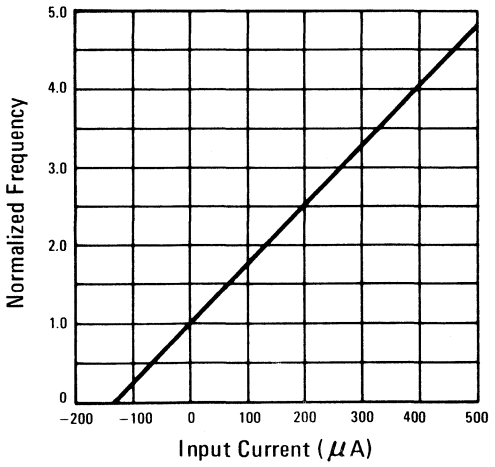
LOOP GAIN CHARACTERISTIC



DEMODULATED OUTPUT SWING



OSCILLATOR FREQUENCY vs. INPUT CURRENT, PIN 9 (f_0 = 50kHz)



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HI-0180/0185

8-Bit A to D Encoder

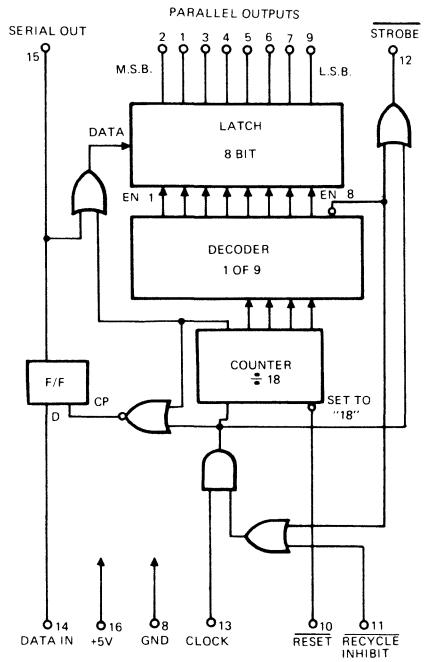
FEATURES

- REPLACES FOUR CONVENTIONAL M.S.I. PACKAGES
- SERIAL AND PARALLEL OUTPUTS
- STROBE OUTPUT INDICATES "DATA READY"
- CONTINUOUS OR "CONVERT ON EXTERNAL COMMAND" OPERATION
- ALSO FUNCTIONS AS SERIAL TO PARALLEL CONVERTER/DATA RECEIVER
- MEETS MIL-STD-883 REQUIREMENTS

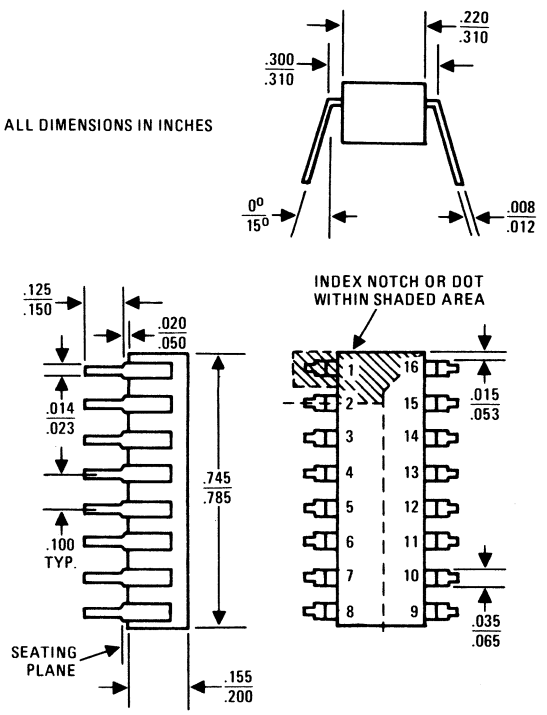
DESCRIPTION

This circuit contains all of the digital logic required to construct a high performance 8-bit successive approximation A/D converter, using an external D/A converter and comparator. When used with the Harris HA-1080/1085 D/A converter and the HA-2111/2311 comparator, a complete A/D is formed, capable of up to 40,000 conversions per second, with 1 L.S.B. absolute accuracy over the full operating temperature range Versatile control inputs allow a number of operating modes. The complete converter is ideal for point-of-measurement conversion in data aquisition systems; and for conversion of audio, instrumentation, and control signals in multiplexed data transmission systems.

FUNCTIONAL DIAGRAM



PACKAGE



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

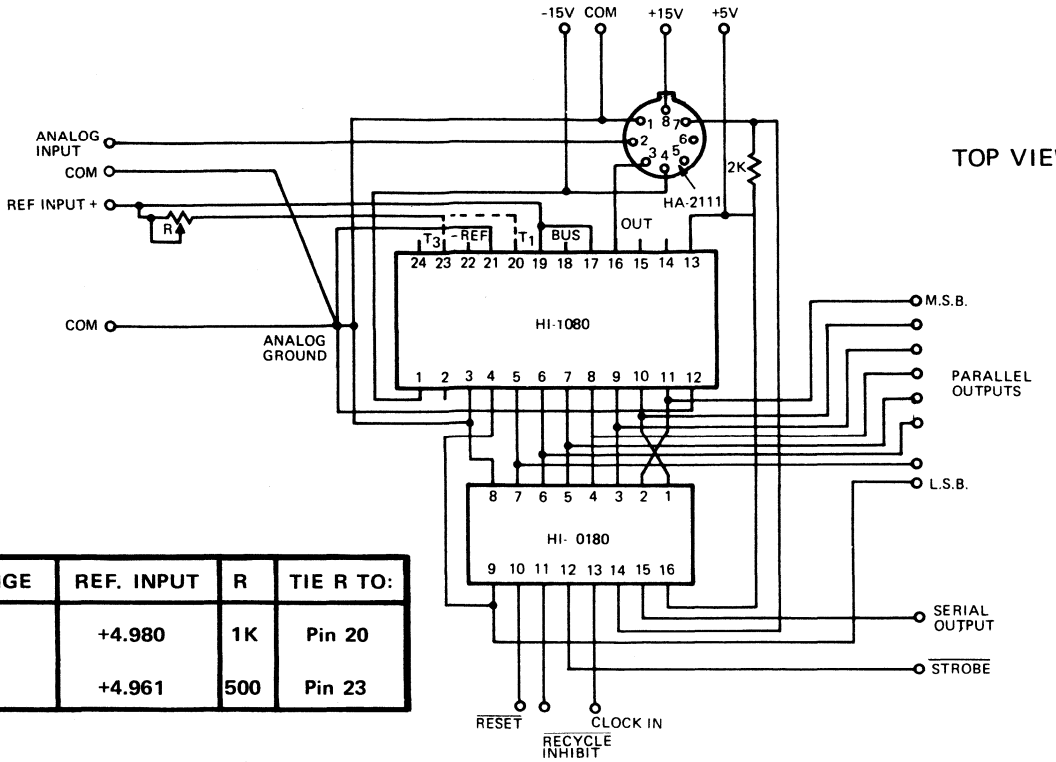
Guaranteed over operating range:

$+4.75V \leq V_{CC} \leq +5.25V$

HI-0180: $-55^{o}C \leq T_{CASE} \leq +125^{o}C$
HI-0185: $0^{o}C \leq T_A \leq +75^{o}C$

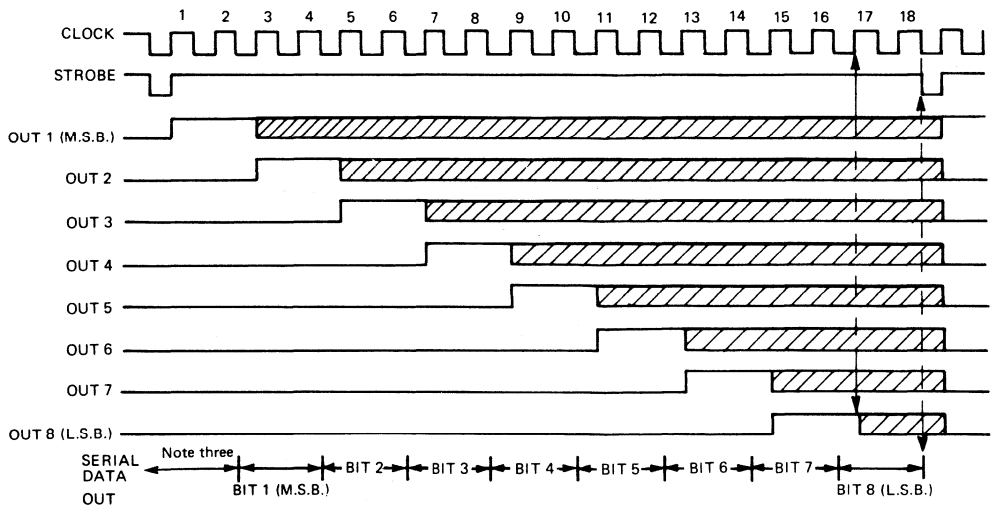
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS.
V_{IH}, High Level Input Voltage		2.0			Volts
V_{IL}, Low Level Input Voltage				0.8	Volts
V_{OH}, High Level Output Voltage	$I_{OH} = -200\mu A$	2.4			Volts
V_{OL}, Low Level Output Voltage	$I_{OL} = 8.0$ mA			0.4	Volts
I_{IH}, High Level Input Current	Clock, Data Inputs: V_I=+2.4V			200	μA
	Clock, Data Inputs: $V_I = V_{CC}$			2.0	mA
	Reset, Inhibit Inputs: V_I=+2.4V			100	μA
	Reset, Inhibit Inputs: $V_I = V_{CC}$			1.0	mA
I_{IL}, Low Level Input Current	Clock, Data Inputs: V_I=0.4V			1.0	mA
	Reset, Inhibit Inputs: V_I=0.4V			0.5	mA
I_{CC}, Power Supply Current			25	60	mA
f_{max}, Maximum Clock Frequency		2.0	4.0		MHz

8-BIT A TO D CONVERTER



INPUT RANGE	REF. INPUT	R	TIE R TO:
0 to +5V	+4.980	1K	Pin 20
-5 to +5V	+4.961	500	Pin 23

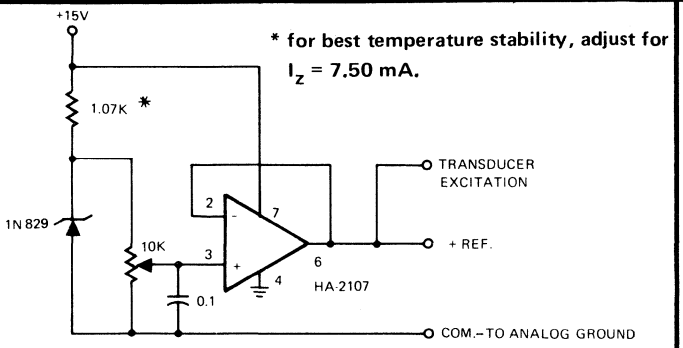
TIMING DIAGRAM



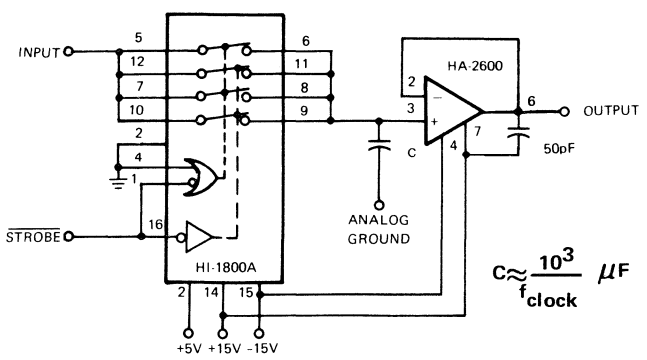
NOTES:

1. Note that 18 clock cycles are required for complete conversion cycle.
2. Shaded areas shown for parallel data outputs denote output states determined by Data Input state immediately prior to shaded area.
3. Serial data output states are determined by data input states immediately prior to each time slot. State of the first time slot is determined by the final data input state of the previous conversion (usually "high" for A/D converter with input within range.)
4. Recycle inhibit input: When "high", continuous conversion results as shown; when "low", conversion continues to final (strobe "low") state and stops -- to restart, apply momentary "high" to recycle inhibit input.
5. Reset input: When "high", normal conversion takes place; when "low", converter immediately sets to final (strobe "low") state. Clock signal will appear at strobe output while reset is held "low".

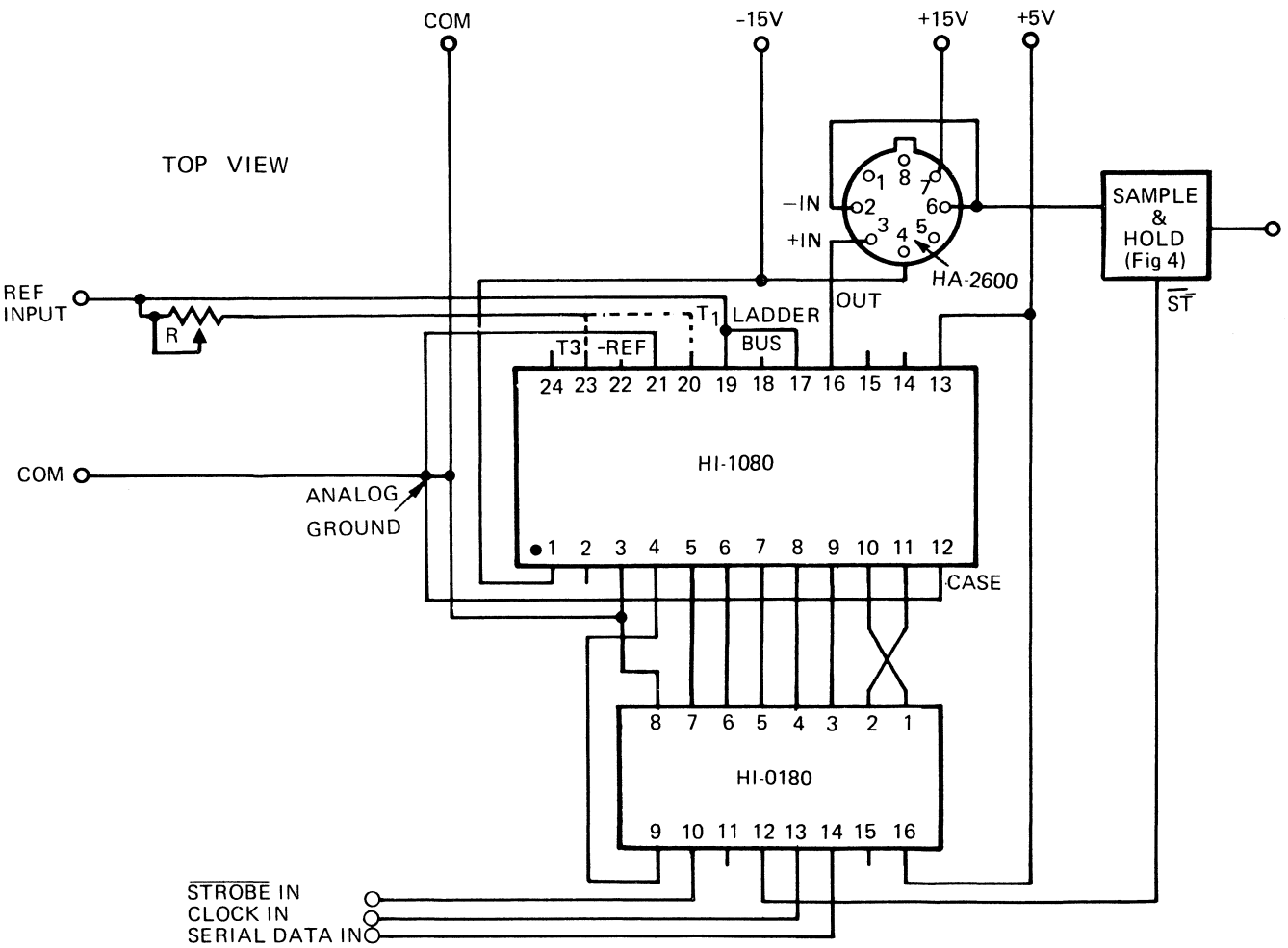
REFERENCE REGULATOR



SAMPLE AND HOLD



SERIAL INPUT DATA RECEIVER & D TO A CONVERTER



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HI-0910/1010

10-Bit D/A Ladder Network

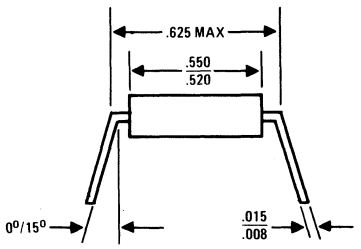
FEATURES

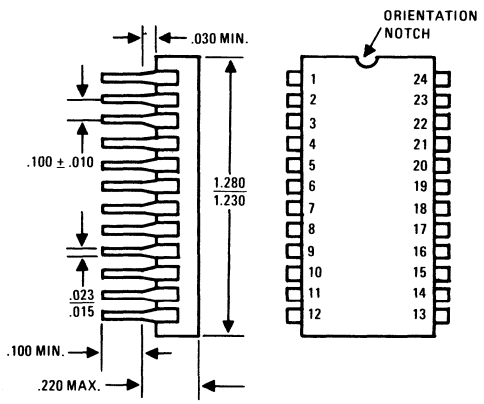
- AVAILABLE IN FULL -55°C TO +125°C TEMPERATURE RANGE PLUS LIMITED TEMPERATURE RANGES.
- COMPREHENSIVE ACCURACY GUARANTEE OVER TEMPERATURE RANGE.
- MONOLITHIC RELIABILITY MEETS MIL-STD-883.
- LOW COST

DESCRIPTION

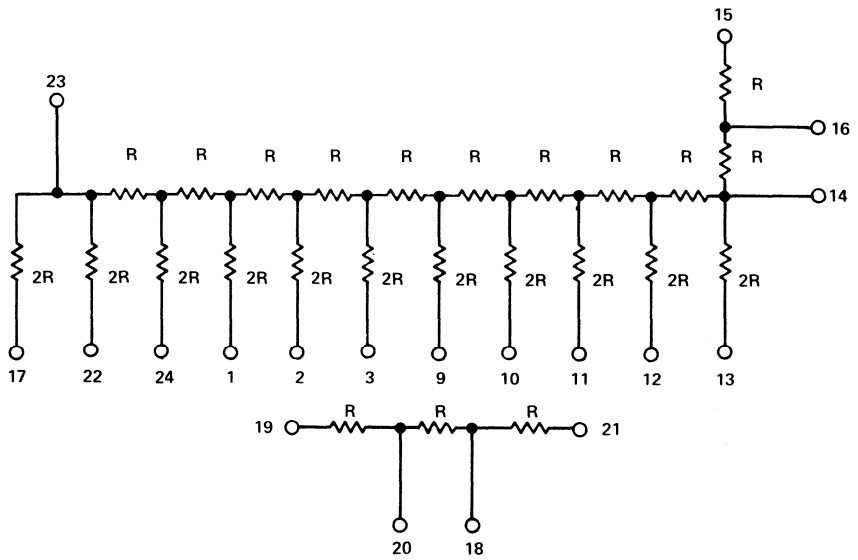
The Harris HI-0910 and HI-1010 are ten-bit, 5K ohm, R-2R ladder networks intended for use in voltage switching D to A and A to D converters. They are fabricated using proven processes involving passivated thin metallic films deposited on a single crystal silicon chip. This results in superior reliability, excellent match in resistance and temperature coefficient, together with the economy of batch processing. Extra resistors matched to the ladder are provided, which may be used as feedback or summing resistors in conjunction with external amplifiers or comparators. Two or more ladders may be cascaded for increased resolution.

PACKAGE





SCHEMATIC AND PIN BREAKOUT



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Applied: ±20.0V

Storage Temperature: -65°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions: Applied Voltage: +5.0V or Ground
T_{AMB} = +25°C
Unless otherwise specified.

PARAMETER		HI-1010-2	HI-0910-2	HI-1010-5	HI-0910-5	UNITS
Operating Temperature	MIN.	-55	-55	0	0	°C
	MAX.	+125	+125	+75	+75	°C
Resistor Value "R" Nom. ±20%		5K	5K	5K	5K	Ω
Accuracy (Note 1)	MAX.	½	1	½	1	L.S.B.
Settling Time (Note 2)	TYP.	500	500	500	500	ns

NOTES: 1. Accuracy is worst case deviation of output voltage from perfect value for any of the 1024 input combinations over the specified operating temperature temperature range.

2. Settling time is the total time measured from an input change until the output settles with ± ½ L.S.B. of its final value.

Test conditions: $R_L \geq 1$ megohm, $C_L \leq 5$pF.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HI-1080/HI-1085

8-Bit D to A Converter
High Speed Monolithic

FEATURES

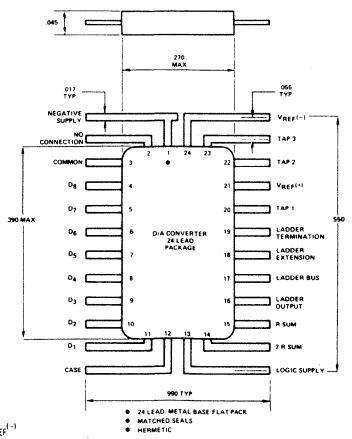
- ACCURACY — (HI-1080) } Guaranteed −55°C to +125°C
  (HI-1085) } or 0° to +75°C
- SPEED — 1.5 Microseconds settling to ½ L.S.B.
- VERSATILITY — Unipolar, Bipolar, Offset Operation
  Positive or Negative External Reference
  Taps Provided for Scale Factor Adjustment
  Provision for Cascading Converters
  Matched Amplifier Feedback Resistors
  Inputs DTL/TTL Compatible
- RELIABILITY — Monolithic Construction
  Meets Requirements of MIL-STD-883

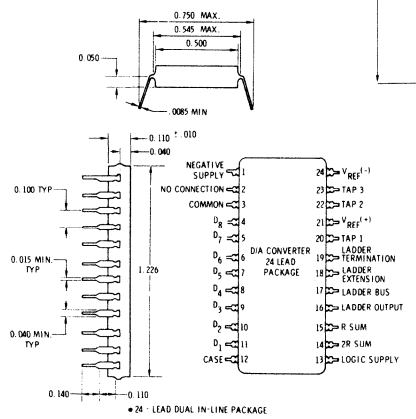
GENERAL DESCRIPTION

The HI-1080/1085 is a current switching converter complete with a precision thin film R-2R ladder resistor network on a single monolithic chip. It is ideal for general purpose high speed, moderate accuracy digital-analog interfaces. It is particularly suitable as part of a high speed successive approximation or up-down counter type A to D converter.

PACKAGES

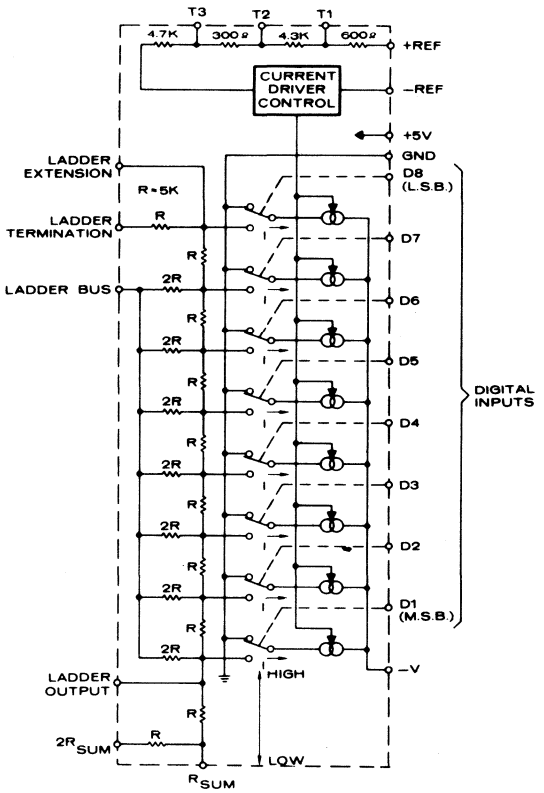
PACKAGE A1



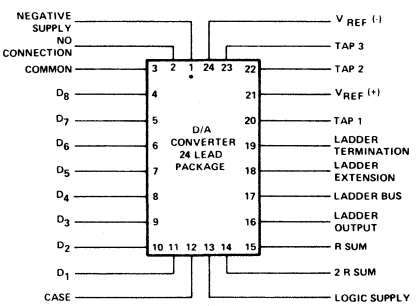


PACKAGE A2

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are limiting values above which permanent circuit damage may occur.

Voltage
V +: +8.0V
V - : -18.0V

Ladder Common:
±8.0V
I_{REF}: 1.6 mA

Storage Temp:
$-65^{o}C \leq TA \leq +150^{o}C$
Power Dissipation:
450 mW *

Digital Inputs: +5.5V

*Derate at 4mW/°C above 85°C ambient.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated all measurements taken at $V^+ = +5V$, $V^- = -15V$
$V_{REF} = +5V$, $V_{in}High = +2.4V$, $V_{in}Low = +0.4V$
Unipolar, zero reference connection (Figure 3)

	HI-1080 TEMP	LIMITS MIN	TYP	MAX	UNITS	HI-1085 TEMP	LIMITS MIN	TYP	MAX	UNITS
Resolution		8			Bits		8			Bits
Accuracy (Calibrated at 25°C) (Note 1)	+25°C -55°C to +125°C		1/4 1/2	1/2 1	L.S.B.	0°C to +75°C		1/2	1	L.S.B.
$V_{Full\ Scale}$ (Note 2) (Uncalibrated)	+25°C	-4.5	-4.98	-5.5	Volts	+25°C	-4.5	-4.98	-5.5	Volts
Power Supply Rejection (Note 3)	-55°C to +125°C	.05	.001		L.S.B. per Volt	0°C to +75°C	.05	.001		L.S.B. per Volt
Settling Time (Note 4)	+25°C		1.5	3.0	μs	+25°C		1.5		μs
Digital Inputs: High Threshold Low Threshold (Note 5) $I_{in}High$ $I_{in}Low$ (Note 6)	 -55°C to +125°C	 0.8 	 .01 -0.7	 2.0 1 -1.0	 Volts Volts μA mA	 0°C to +75°C	 0.8 	 .01 -0.7	 2.0 1 -1.0	 Volts Volts μA mA
Supply Current: I^+ I^- I_{REF} (Note 7)	-55°C to +125°C		8 8 0.5	10 10 0.6	mA mA mA	0°C to +75°C		8 8 0.5	10 10 0.6	mA mA mA

NOTES: Test Conditions –

1. Any Input Combination
2. Inputs all low
3. $\Delta V_{OUT}/\Delta V_{SUPPLY}$
   $V^+ = +5 \pm 0.5V$
   $V^- = -15 \pm 3V$
4. To ±0.2% of full scale after full scale input step
   $R_L > 10\ M\Omega$
   $C_L < 5pF$
5. $V^+ = 4.5V$
6. $V_{in} = 2.4$ Volts
   $V^+ = 5.5V$
   $V_{in} = 0.4$ Volts
   $V^+ = 5.5V$
7. $V^+ = +5.0V$
   $V^- = -15.0V$
   $V_{REF} = +5.0V$
   Inputs all low

PERFORMANCE CURVES

TYPICAL OUTPUT ACCURACY VS. TEMPERATURE

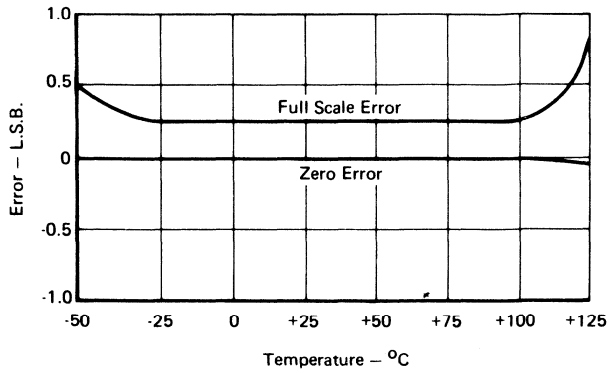


Figure 1

TYPICAL SETTLING TIME

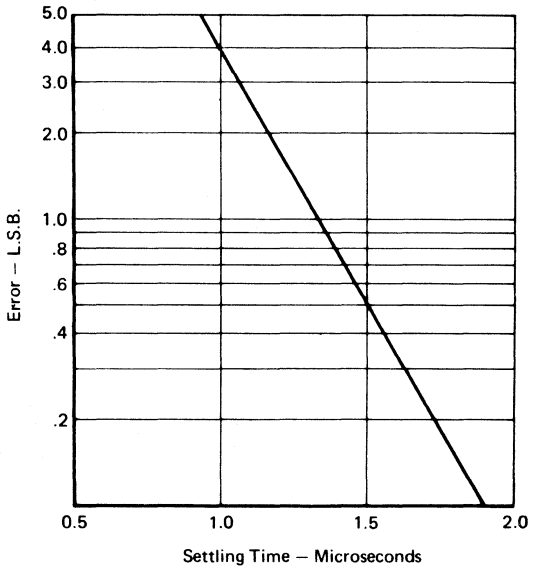
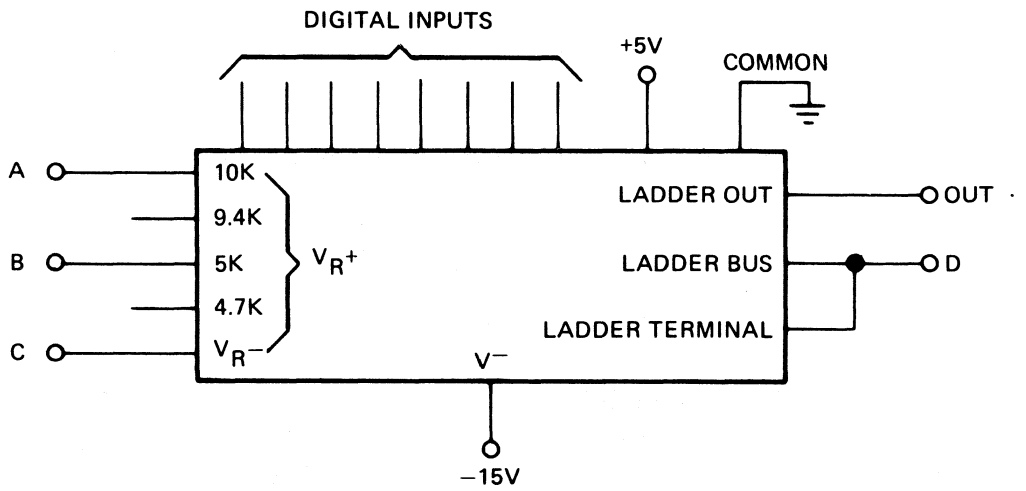


Figure 2

OPERATION MODES

D/A CONVERTER OPERATION MODES



MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALL LOW	CONNECTIONS			
		A	B	C	D
UNIPOLAR ZERO REFERENCE	0 TO – V_R+ – 1 L.S.B.	V_R+	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+ / V_R+/ TO 0 + 1 L.S.B.	V_R+	N.C.	GND	V_R
BIPOLAR	/V_R+/ TO –V_R + 1 L.S.B.	N.C.	V_R+	GND	V_R+

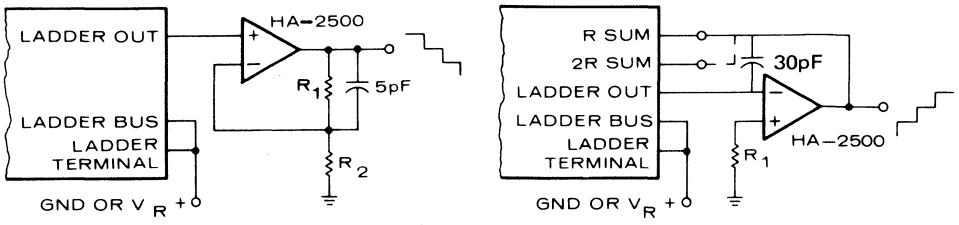
OPERATING MODES

Figure 3

* Tap 1 or Tap 3 with selected external series resistor may be substituted for points A or B, respectively, for fine adjustment of output range.

TYPICAL APPLICATIONS

BUFFER AMPLIFIER CONNECTION



NON-INVERTING OUTPUT
(MORE NEGATIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

OUTPUT RANGE: SAME AS SHOWN ON 'CHART 'OPERATING MODE' CHART

MULTIPLIED BY $\frac{R\,2}{R_1 + R_2}$

INVERTING OUTPUT
(MORE POSITIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO	R_1
+4.98V	SUM	2.5K
+9.96V	2R SUM	3.3K

Figure 4

CASCADED UNITS FOR 12 BIT RESOLUTION

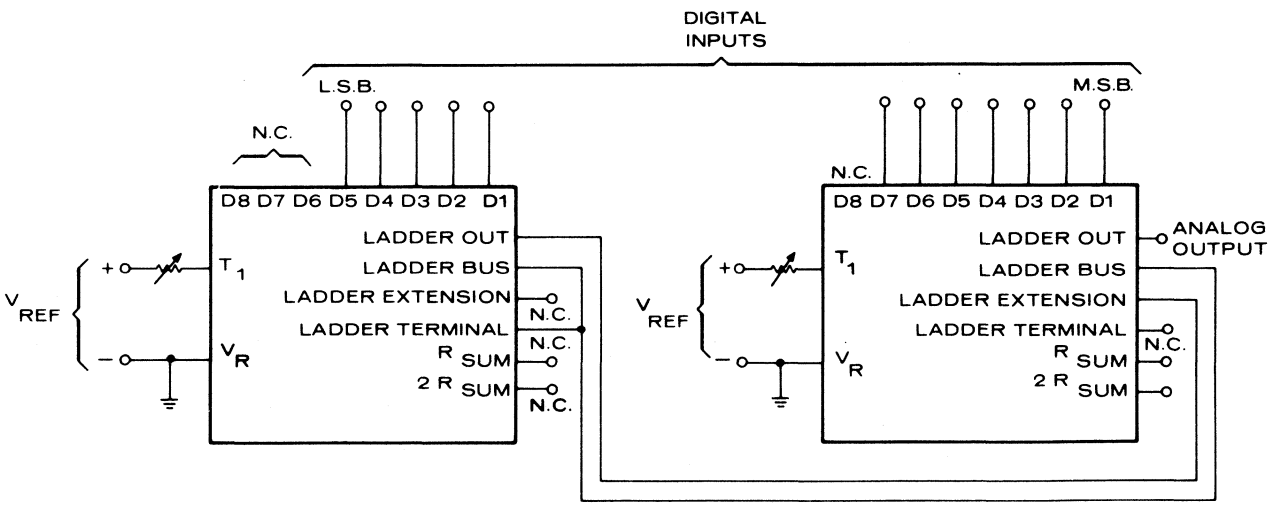


Figure 5

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HI-1800/HI-1800A

Analog Switch Four-Channel

DESCRIPTION

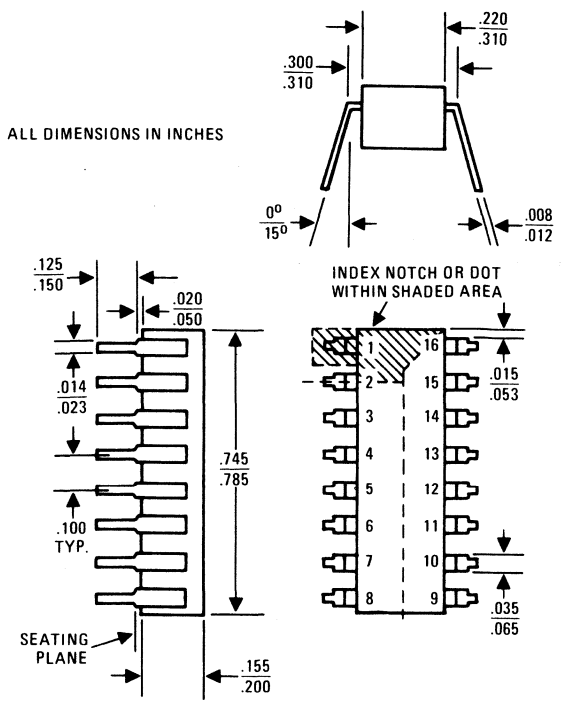
The HI-1800 is a general purpose analog switch which may be used as a signal selector, multiplexer, chopper, or crosspoint switch for signals from D.C. to R.F. The configuration is two independent DPST switches with versatile TTL compatible addressing logic which allows connection as two SPDT, or a single DPDT, SPDT, or SPST switch by connection of external jumpers. ON resistance decreases correspondingly when switching elements are connected in parallel. The HI-1800 is fabricated on a single dielectrically isolated chip using complimentary N and P channel MOS devices. This unique process produces exceptionally low leakage currents (even at +125°C), constant ON resistance, low power dissipation, and fast switching. The HI-1800 is available in a hermetic 16 pin dual-in-line package.

TRUTH TABLE

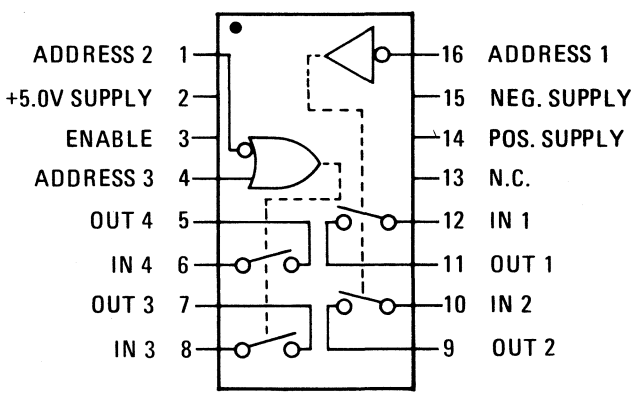
INPUT ADDRESS				SWITCH CHANNELS			
1	2	3	$\overline{EN}$	1	2	3	4
L	X	X	L	ON	ON		
H	X	X	L	OFF	OFF		
X	L	X	L			ON	ON
X	X	H	L			ON	ON
X	H	L	L			OFF	OFF
X	X	X	H	OFF	OFF	OFF	OFF

H ≥ +4.0V L ≤ +0.4V

PACKAGE



PIN FUNCTIONS



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	−8.0V to +8.0V
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	200mW
Analog Input Voltage	$\pm V_{Supply}$	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Supplies = +12.0V, −12.0V, +5.0V

PARAMETER	TEMP.	HI-1800-2/HI-1800A-2 −55°C to +125°C MIN.	TYP.	MAX.	HI-1800-5/HI-1800A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_{IN}, Analog Signal Range (HI-1800)	Full	-5.0		+5.0	-5.0		+5.0	V
V_{IN}, Analog Signal Range (HI-1800A)	Full	-10.0		+10.0	-10.0		+10.0	V
R_{ON}, ON Resistance (Note 2)	+25°C		125	200		125	250	Ω
	Full			250			300	Ω
I_{LI}, Input Leakage Current	+25°C		.01			.01		nA
	Full			20			60	nA
I_{LO}, Output Leakage Current	+25°C		.01			.01		nA
	Full			20			60	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 3)	Full	4.0			4.0			V
I_{IN}, Input Leakage Current	Full		.01	10		.01	10	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 4)	+25°C		250			250		ns
C_{IN}, Channel Input Capacitance	+25°C		5			5		pF
C_{OUT}, Channel Output Capacitance	+25°C		5			5		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5	20		5	20	mW
P_{DS}, Standby Power (Note 5)	Full		2.5	10		2.5	10	mW
I_+, Current Pin 14	Full			0.5			0.5	mA
I_-, Current Pin 15	Full			1			1	mA
I_L, Current Pin 2	Full			1			1	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges.
2. $V_{OUT} = \pm 5.0V$, $I_{OUT} = -100\mu A$.
3. To drive from DTL/TTL circuits, 1K pullup resistors to +5.0V supply are recommended.
4. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0V to +4.0V.
5. Voltage at Pin 3, $\overline{ENABLE} \geq +4.0V$.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HI-1818/1828/ 1818A/1828A

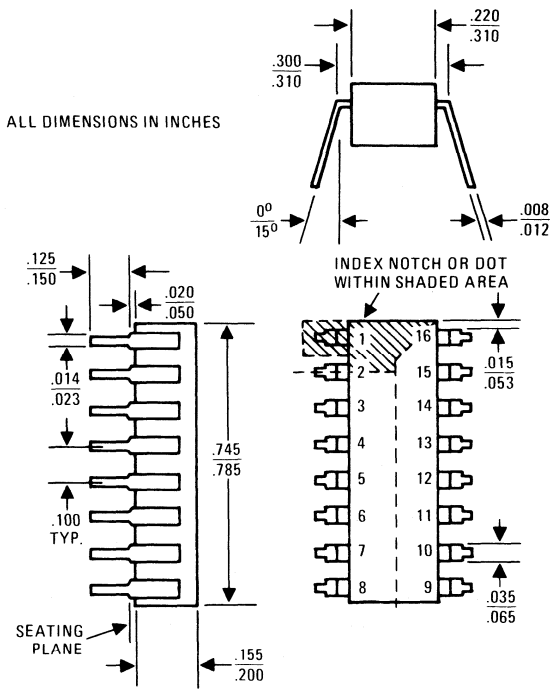
8 Channel Analog Multiplexers

LINEAR DATA

FEATURES

- SIGNAL RANGE ±5.0V, ±10.0V
- "ON" RESISTANCE 250 Ω TYP.
- LEAKAGE AT +125°C 1nA TYP.
- ACCESS TIME 250ns TYP.
- POWER CONSUMPTION 5mW TYP.
- DTL/TTL COMPATIBLE ADDRESS
- -55°C TO +125°C OPERATION

PACKAGE

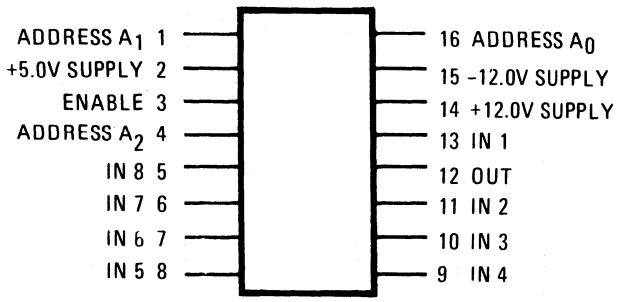


GENERAL DESCRIPTION

The Harris Hi-1818 and HI-1828 Analog Multiplexers represent a significant breakthrough in analog switch performance. Vastly superior characteristics are obtained through the unique process of forming complementary MOS transistors in a dielectrically isolated substrate. These devices are useful as multiplexers, signal selectors, and choppers over a wide range of signal levels and switching frequencies. The HI-1818 is a single 8 channel multiplexer while the HI-1828 is a dual 4 channel version. The devices are packaged in a standard 16 pin dual in-line hermetic case and are available in the full military or commercial temperature ranges.

PIN OUT/TRUTH TABLE

HI-1818/1818A

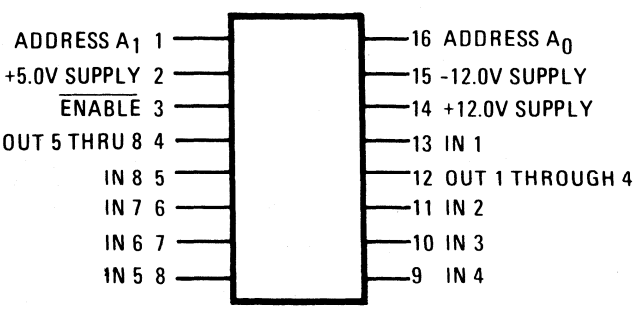


ADDRESS A_2	A_1	A_0	EN	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	X	NONE

PIN OUT/TRUTH TABLE

HI-1828/1828A

ADDRESS A_1	A_0	EN	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	-8.0V to +8.0V
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	200mW
Analog Input Voltage	$\pm V_{Supply}$	Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

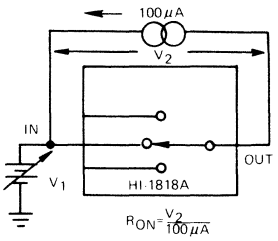
Supplies = +12.0V, -12.0V,+5.0V (Note 5)

PARAMETER	TEMP.	HI-1818-2/1818A-2 HI-1828-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818-5/1818A-5 HI-1828-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_{IN}, Analog Signal Range (HI-1818/1828)	Full	-5.0		+5.0	-5.0		+5.0	V
(HI-1818A/1828A)	Full	-10.0		+10.0	-10.0		+10.0	V
R_{ON}, ON Resistance (Note 2)	+25°C		250	400		250	500	Ω
	Full			500			600	Ω
I_{LI}, Input Leakage Current	+25°C		.01			.01		nA
	Full			10			30	nA
I_{LO}, Output Leakage Current	+25°C		0.1			0.1		nA
	Full			50			100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 3)	Full	4.0			4.0			V
I_{IN}, Input Leakage Current	Full		.01	1		.01	1	µA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 4)	+25°C		250			250		ns
O_{IN}, Channel Input Capacitance	+25°C		3			3		pF
C_{OUT}, Channel Output Capacitance	+25°C		10			10		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 5)	Full		5	20		5		mW
P_{DS}, Standby Power (Note 6)	Full		2.5	10		2.5		mW
I_+, Current Pin 14	Full		0.1	0.5		0.1		mA
I_-, Current Pin 15	Full		0.3	1		0.3		mA
I_L, Current Pin 2	Full		0.3	1		0.3		mA

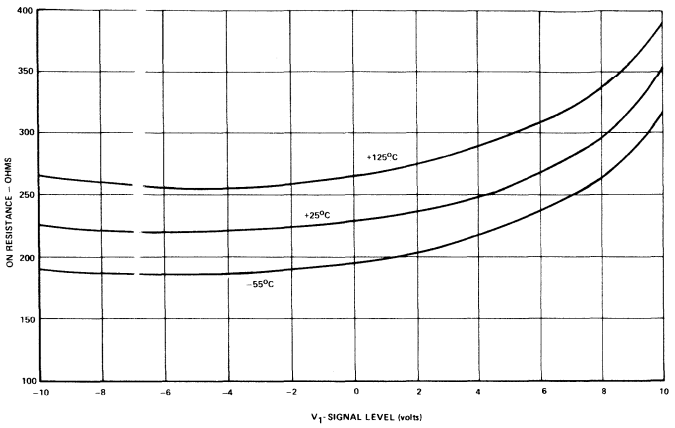
NOTES:
1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges. All pins should be shorted together during handling and installation.
2. V_{OUT} = ±5.0V, I_{OUT} = -100 µA
3. To drive from DTL/TTL circuits, 1KΩ pullup resistors to +5.0V supply are recommended.
4. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0V to +4.0V.
5. HI-1818A/1828A may be operated with +15V supplies with degraded leakage currents and power dissipation.
6. Voltage at Pin 3, $\overline{ENABLE}$ +4.0V.

PERFORMANCE CHARACTERISTICS

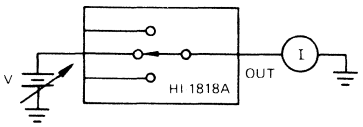
ON RESISTANCE vs ANALOG SIGNAL LEVEL



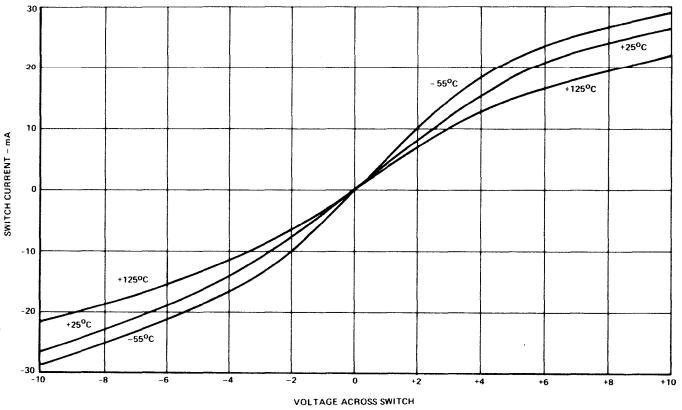
Test Circuit



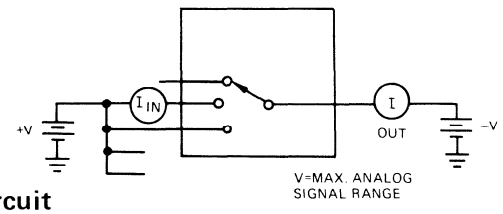
ON CHANNEL CURRENT vs VOLTAGE



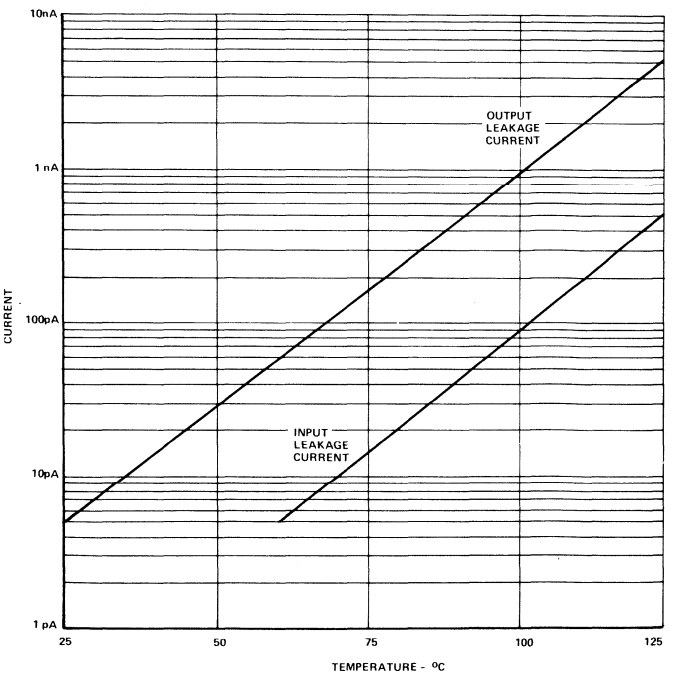
Test Circuit



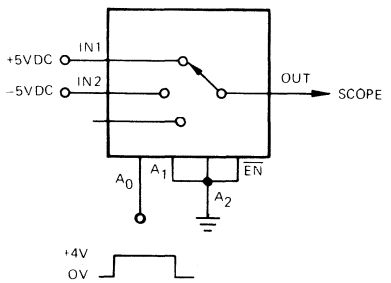
LEAKAGE CURRENT vs TEMPERATURE



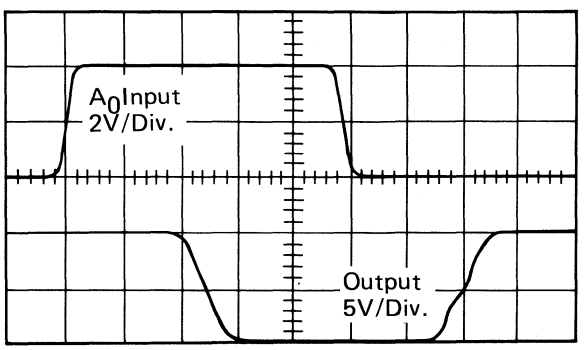
Test Circuit



ACCESS TIME



Test Circuit

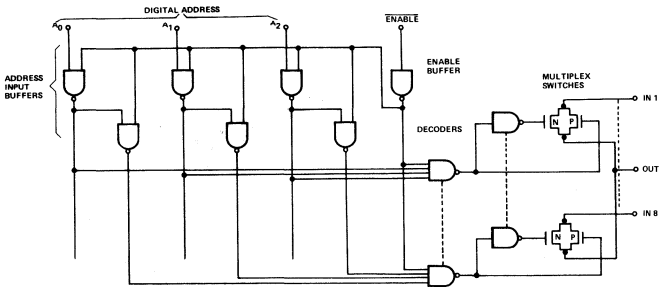


100ns/Div.

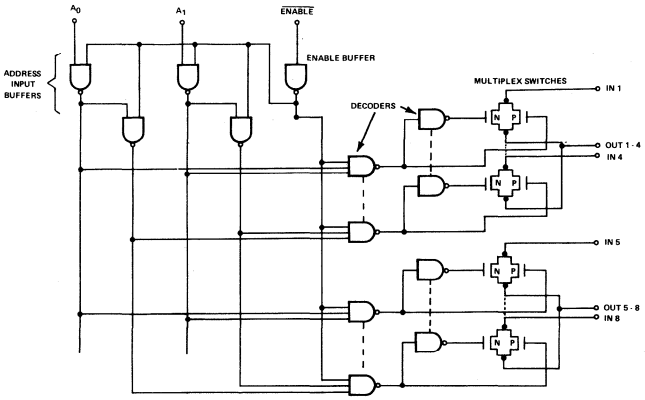
Note: Make-before-break overlap is approximately 100ns.

SCHEMATIC DIAGRAM

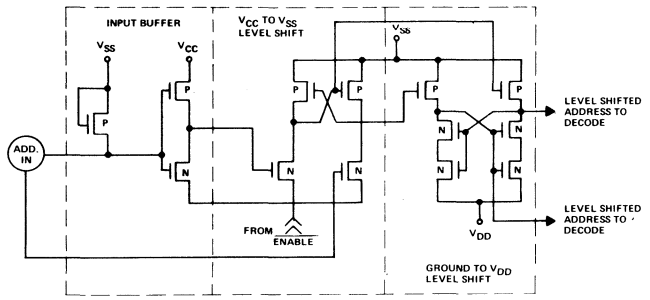
BLOCK DIAGRAM HI-1818



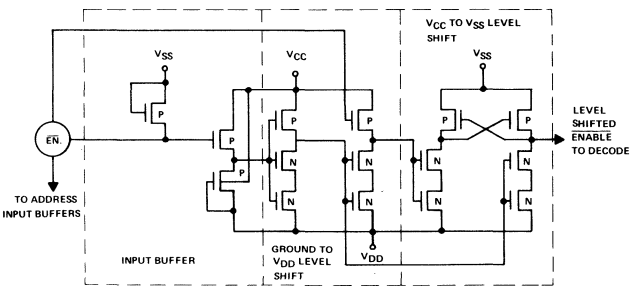
BLOCK DIAGRAM HI-1828



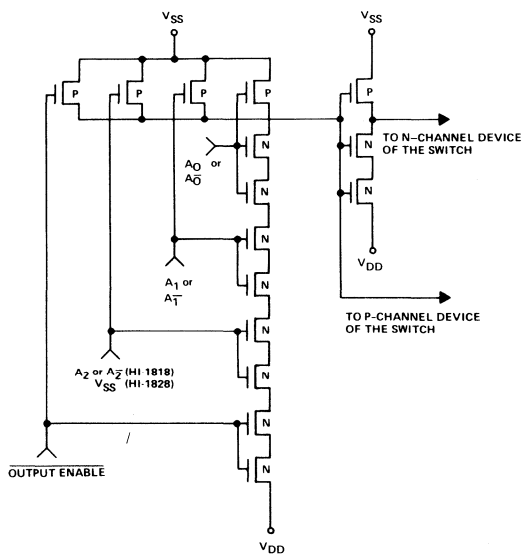
ADDRESS INPUT BUFFER



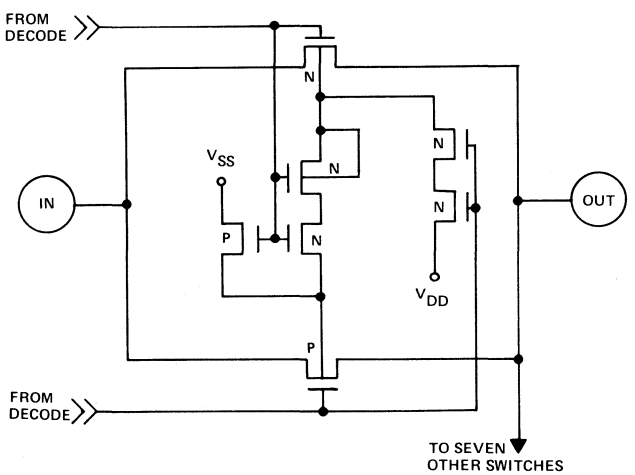
ENABLE INPUT BUFFER



DECODER GATE



MULTIPLEX SWITCH



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HS-1000

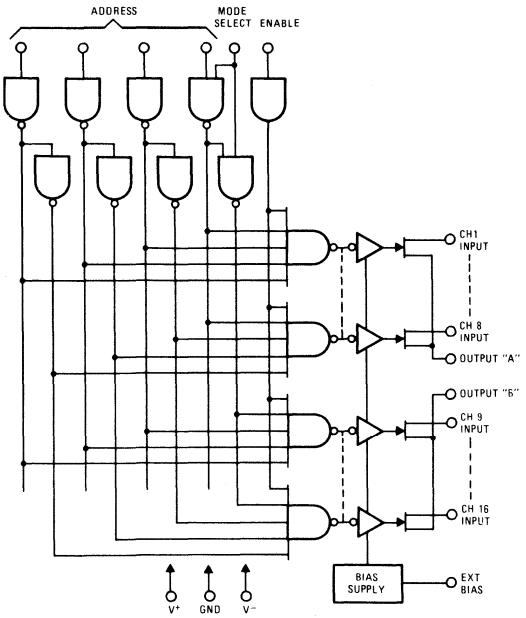
16 Channel Analog Multiplexer

LINEAR DATA

PRODUCT DESCRIPTION

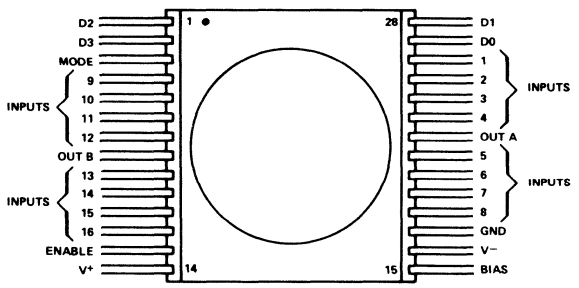
The HS-1000 16 Channel Multiplexer is an analog signal commutator combining the excellent switching properties of Junction Field Effect Devices with bipolar logic gating circuitry in a single monolithic circuit. The circuit commutates a bipolar signal range in excess of ±10V in a 1-of-16 or 2-of-16 configuration, allowing dual 8-channel, differential 8-channel or 16-channel operating modes. The HS-1000 features extremely low OFF current, fast random access channel selection and full channel blanking control for address expansion. The unit operates over the full military temperature range from −55°C to +125°C and meets or exceeds the requirements of MIL-STD-883.

DIAGRAM

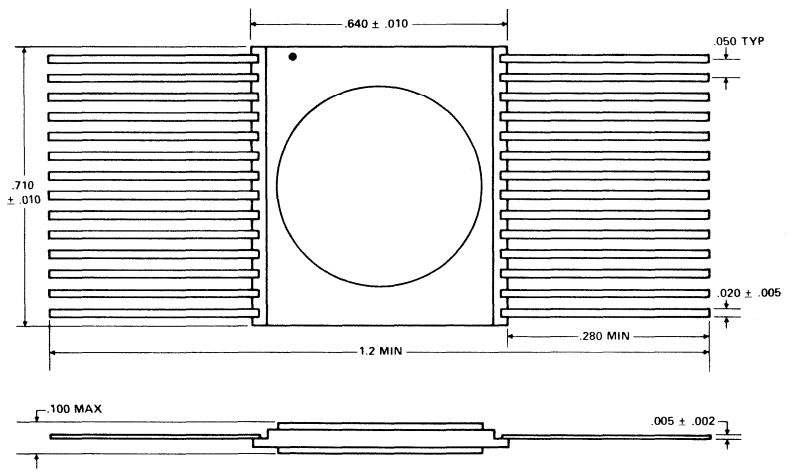


16 Channel Multiplexer Functional Diagram

PACKAGE



28-Lead Flat Package



ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V, V_{EE} = −15.0V, T = +25°C unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS
On Resistance (V_{IN} = ±8.0V		500	1200	Ohms
Off Input Current (V_{IN} = +10.0V) (V_{OUT} = +10.0V)		30	250	pA
Analog Input Voltage Range V_{EE} = −15.0	−8.0		+12.0	V
V_{EE} = −18.0	−10.0		+10.0	V
Input Capacitance (Address Enable = GND) (V_{IN} = −10.0V)			4	pF
Output Capacitance (Address Enable = GND) (V_{OUT} = −10.0V)			40	pF
Access Time (V_O = +10.0V)		0.5	2.0	µs
Power Dissipation		200		mW
Address Logic Levels V_{IN} (0)			.5	V
V_{IN} (1)	2.0			V
Address Logic Input Current I_{IN} (0) (V_{IN} = GND)		250		µA
Address Enable Input Current I_{IN} (0) (V_{IN} = GND)		800		µA
Cross Talk (V_{IN} = 20 VP/P) 100kHz		−80		dB

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DIELECTRICALLY ISOLATED NPN MATCHED PAIRS

2N4044 2N4045 2N4100 2N4878 2N4879 2N4800

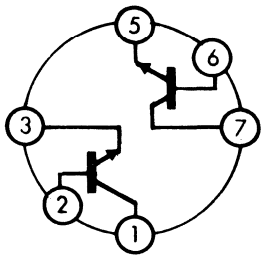
Dual • Monolithic • NPN • Silicon Transistors

LINEAR DATA

FEATURES

- HIGH GAIN AT LOW CURRENT $h_{FE} \geq 200 @ 10\mu A$
- LOW OUTPUT CAPACITANCE $C_{obo} \leq 0.8pF$
- h_{FE} MATCH $h_{FE1}/h_{FE2} \leq 10\%$
- TIGHT V_{BE} TRACKING $\Delta(V_{BE1} - V_{BE2}) \leq 3\mu V/^{o}C$ $-55^{o}C$ TO $+125^{o}C$

CONNECTION

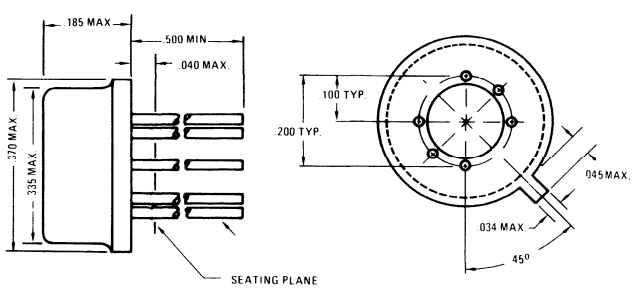


ABSOLUTE MAXIMUM RATINGS

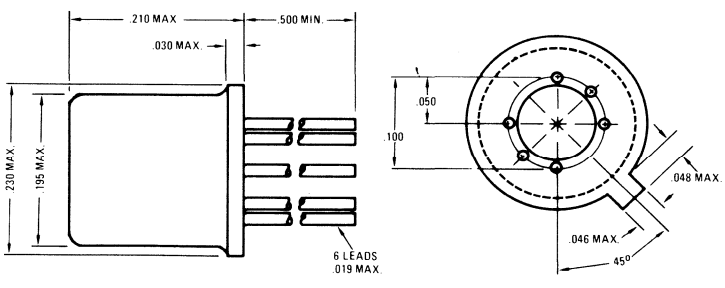
	SYM.	2N4878	2N4879	2N4880	2N4044	2N4100	2N4045	UNITS
Dissipation at 25°C Case Temperature								
Each Side (Note 1)	P_D	0.3	0.3	0.3	0.4	0.4	0.4	Watt
Both Sides	P_D	0.5	0.5	0.5	0.75	0.75	0.75	Watt
Derating Factor								
Each Side		1.7	1.7	1.7	2.3	2.3	2.3	mW/°C
Both Sides		2.9	2.9	2.9	4.3	4.3	4.3	mW/°C
Voltage								
Collector to Base	V_{CBO}	60	55	45	60	55	45	V
Collector to Emitter	V_{CBO}	60	55	45	60	55	45	V
Emitter to Base (Note 2)	V_{EBO}	7.0	7.0	7.0	7.0	7.0	7.0	V
Collector to Collector	V_{CCO}	100	100	100	100	100	100	V
Collector Current	I_C	10	10	10	10	10	10	mA
Storage Temperature	T_S	-65 to +200	-65 to +200	-65 to +200	-65 to +200	-65 to +200	-65 to +200	°C

PACKAGES

TO–78
2N4044 / 2N4045 / 2N4100



TO–71
2N4878 / 2N4879 / 2N4800



NOTES: 1. All leads gold plated KOVAR.
2. All dimensions in inches

ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	2N4044/2N4878 MIN.	2N4044/2N4878 MAX.	2N4100/2N4879 MIN.	2N4100/2N4879 MAX.	2N4045/2N4880 MIN.	2N4045/2N4880 MAX.	UNITS	CONDITIONS
DC Current Gain	h_{FE}	200	600	150	600	80			$I_C = 10\mu A, V_{CE} = 5.0V$
DC Current Gain	h_{FE}	225		175		100			$I_C = 1.0mA, V_{CE} = 5.0V$
DC Current Gain	h_{FE} (−55°C)	75		50		30			$I_C = 10\mu A, V_{CE} = 5.0V$
Emitter - Base On Voltage	V_{BE} (on)		0.7		0.7		0.7	V	$I_C = 10\mu A, V_{CE} = 5.0V$
Collector Saturation Voltage	V_{CE} (sat)		0.35		0.35		0.35	V	$I_C = 1.0mA, I_B = 0.1mA$
Collector Cutoff Current	I_{CBO}		0.1		0.1		0.1	nA	$I_E = 0, V_{CB} = 45.0V, 30.0V$
Collector Cutoff Current	I_{CBO} (+150°C)		0.1		0.1		0.1	A	$I_E = 0, V_{CB} = 45.0V, 30.0V$
Emitter Cutoff Current	I_{EBO}		0.1		0.1		0.1	nA	$I_C = 0, V_{EB} = 5.0V$
Output Capacitance	C_{obo}		0.8		0.8		0.8	pF	$I_E = 0, V_{CB} = 5.0V$
Emitter Transition Capacitance	C_{TE}		1		1		1	pF	$I_C = 0, V_{EB} = 0.5V$
Collector to Collector Capacitance	$C_{C1,C2}$		0.8		0.8		0.8	pF	$V_{CC} = 0$
Collector to Collector Leakage Current	$I_{C1,C2}$		5		5		5	pA	$V_{CC} = \pm 100.0V$
Collector to Emitter Sustaining Voltage	V_{CEO} (sustaining)	60.0		55.0		45.0		V	$I_C = 1mA, I_B = 0$
Current Gain Bandwidth Product	f_T	200		150		150		mHz	$I_C = 1mA, V_{CE} = 10.0V$
Current Gain Bandwidth Product	f_T	20		15		15		mHz	$I_C = 10\mu A, V_{CE} = 10.0V$
Narrow Band Noise Figure	NF		2		3		3	dB	$I_C = 10\mu A, V_{CE} = 5.0V$ f = 1kHz, $R_G = 10k\Omega$, BW = 200Hz
Collector Base Breakdown Voltage	BV_{CBO}	60.0		55.0		45.0		V	$I_C = 10\mu A, I_E = 0$
Emitter Base Breakdown Voltage	BV_{EBO}	7.0		7.0		7.0		V	$I_E = 10\mu A, I_C = 0$

MATCHING CHARACTERISTICS

PARAMETER	SYM.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS	CONDITIONS
DC Current Gain Ratio (Note 3)	h_{FE1}/h_{FE2}	0.9	1	0.85	1	0.8	1		$I_C = 10\mu A$ to 1mA $V_{CE} = 5.0V$
Base Emitter Voltage Differential	$\lvert V_{BE1} - V_{BE2} \rvert$		3		5		5	mV	$I_C = 10\mu A$, $V_{CE} = 5.0V$
Base Current Differential	$\lvert I_{B1} - I_{B2} \rvert$		5		10		25	nA	$I_C = 10\mu A$, $V_{CE} = 5.0V$
Base-Emitter Voltage Differential Change with Temperature	$\lvert \Delta(V_{BE1} - V_{BE2}) \rvert / ^\circ C$		3		5		10	V/°C	$T_A = -55^\circ C$ to +125°C $I_C = 10\mu A, V_{CE} = 5.0V$
Base-Current Differential Change with Temperature	$\lvert \Delta(I_{B1} - I_{B2}) \rvert / ^\circ C$		0.3		0.5		1	nA/°C	$T_A = -55^\circ C$ to +125°C, $I_C = 10\mu A$, $V_{CE} = 5.0V$

SMALL SIGNAL CHARACTERISTICS

PARAMETER	SYM.	TYPICAL VALUE	UNITS	CONDITIONS
Input Resistance	h_{ib}	28	Ohms	$I_C = 1mA, V_{CB} = 5.0V$
Voltage Feedback Ratio	h_{rb}	4.3	$X 10^{-4}$	$I_C = 1mA, V_{CB} = 5.0V$
Small Signal Current Gain	h_{fe}	250		$I_C = 1mA, V_{CE} = 5.0V$
Output Conductance	h_{ob}	0.6	$X 10^{-7}$ mhos	$I_C = 1mA, V_{CB} = 5.0V$
Input Resistance	h_{ie}	9.6	kΩ	$I_C = 1mA, V_{CE} = 5.0V$
Voltage Feedback Ratio	h_{re}	4.2	$X 10^{-4}$	$I_C = 1mA, V_{CE} = 5.0V$
Output Conductance	h_{oe}	12	mhos	$I_C = 1mA, V_{CE} = 5.0V$

NOTES: 1. Maximum ratings are limiting values above which devices may be damaged. These ratings give a maximum junction temperature of 200°C.

2. The reverse base-to-emitter voltage must never exceed 7.0V and the reverse base-to-emitter current must never exceed 10 amperes.
3. Lower of two h_{FE} readings is defined as h_{FE1}.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS INTERTYPE CORPORATION

DIELECTRICALLY ISOLATED PNP MATCHED PAIRS 2N5117 2N5118 2N5119

Dual•Monolithic•PNP•Silicon Transistors

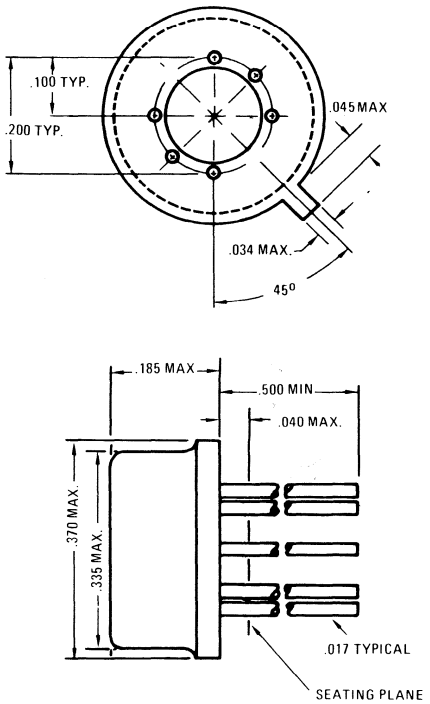
FEATURES

- HIGH GAIN AT LOW CURRENT $h_{FE} \geq 100 @ 10\mu A$
- LOW OUTPUT CAPACITANCE $C_{obo} \leq 0.8pF$
- h_{FE} MATCH $h_{FE1}/h_{FE2} \leq 10\%$
- TIGHT V_{BE} TRACKING $\Delta(V_{BE1} - V_{BE2}) \leq 3\mu V/^{o}C$ $-55^{o}C$ TO $+125^{o}C$

ABSOLUTE MAXIMUM RATINGS

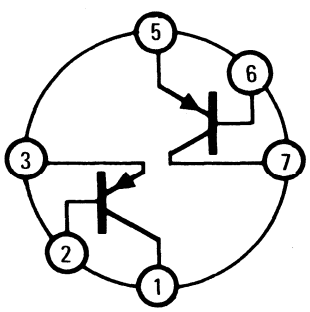
	SYM.	2N5117 2N5118 2N5119	UNITS
Dissipation at 25°C			
Case Temperature			
Each Side (Note 1)	P_D	0.4	Watt
Both Sides	P_D	0.75	Watt
Derating Factor			
Each Side		2.3	mW/°C
Both Sides		4.3	mW/°C
Voltage			
Collector to Base	V_{CBO}	45.0	V
Collector to Emitter	V_{CBO}	45.0	V
Emitter to Base (Note 2)	V_{EBO}	7.0	V
Collector to Collector	V_{CCO}	100.0	V
Collector Current	I_C	10	mA
Storage Temperature	T_S	-65 to +200	°C
Lead Temperature for 10 seconds		+300	°C

PACKAGE



NOTES: 1. All leads gold plated KOVAR
2. All dimensions in inches

CONNECTION



ELECTRICAL CHARACTERISTICS

	SYMBOL	2N5117 2N5118 MIN.	2N5117 2N5118 MAX.	2N5119 MIN.	2N5119 MAX.	UNITS	CONDITIONS
DC Current Gain	h_{FE}	100	300	50			I_C = 10μA, V_{CE} = 5.0V
DC Current Gain	h_{FE}	100		50			I_C = 500μA, V_{CE} = 5.0V
DC Current Gain (−55°C)	h_{FE}	30		20			I_C = 10μA, V_{CE} = 5.0V
Collector Cutoff Current	I_{CBO}		0.1		0.1	nA	I_E = 0, V_{CB} = 30.0V
Collector Cutoff Current (150°C)	I_{CBO}		0.1		0.1	μA	I_E = 0, V_{CB} = 30.0V
Emitter Cutoff Current	I_{EBO}		0.1		0.1	nA	I_C = 0, V_{EB} = 5.0V
Collector-Collector Leakage	$I_{C1, C2}$		5.0		5.0	pA	V_{CC} = 100V
Current Gain Bandwidth Product	f_T	100		100		MHz	I_C = 500μA, V_{CE} = 10.0V
Output Capacitance	C_{ob}		0.8		0.8	pF	I_E = 0, V_{CB} = 5.0V
Emitter Transition Capacitance	C_{TE}		1.0		1.0	pF	I_C = 0, V_{EB} = 0.5V
Collector-Collector Capacitance	$C_{C1, C2}$		0.8		0.8	pF	V_{CC} = 0
Collector-Emitter Sustaining Voltage	V_{CEO} (sustaining)	45.0		45.0		V	I_C = 1.0mA, I_E = 0
Narrow Band Noise Figure	NF		4.0		4.0	dB	I_C = 10μA, V_{CE} = 5.0V, f = 1kHz R_G = 10KΩ, BW = 200cps
Collector Base Breakdown Voltage	$V_{(BE)\ CBO}$	45.0		45.0		V	I_C = 10μA, I_E = 0
Emitter Base Breakdown Voltage	$V_{(BE)\ CBO}$	7.0		7.0		V	I_E = 10μA, E_C = 0

MATCHING CHARACTERISTICS

	SYM.	2N5117 MIN.	2N5117 MAX.	2N5118 MIN.	2N5118 MAX.	2N5119 MIN.	2N5119 MAX.	UNITS	CONDITIONS
DC Current Gain Ratio (Note 3)	h_{FE1}/h_{FE2}	0.9	1.0	0.85	1.0	0.8	1.0		I_C = 10μA to 500μA, V_{CE} = 5.0V, I_C = 10μA, V_{CE} = 5.0V
Base-Emitter Voltage Differential	$V_{BE1} - V_{VE2}$		3.0		5.0		5.0	mV	I_C = 10μA to 500μA, V_{CE} = 5.0V, I_C = 10μA, V_{CE} = 5.0V
Base Current Differential	$I_{B1} - I_{B2}$		10.0		15		40	nA	I_C = 10μA, V_{CE} = 5.0V
Base Voltage Differential Change with Temperature	$\Delta(V_{BE1} - V_{BE2})$		3.0		5.0		10	μV/°C	T_A = −55°C to +125°C I_C = 10μA, V_{CE} = 5.0V
Base-Current Differential Change with Temperature	$\Delta(I_{B1} - I_{B2})$		0.3		0.5		1.0	nA/°C	T_A = −55°C to +125°C I_C = 10μA, V_{CE} = 5.0V

NOTES:
1. Maximum ratings are limiting values above which devices may be damaged. These ratings give a maximum junction temperature of 200°C.
2. The reverse base-to-emitter voltage must never exceed 7.0V and the reverse base-to-emitter current must never exceed 10μA.
3. Lower of two h_{FE} readings is defined as h_{FE1}.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 501

HA-909 OPERATIONAL AMPLIFIER

SERVO PREAMPLIFIER

Harris's HA-909 Operational Amplifier offers a new dimension in the design of monolithic DC servo preamplifiers. It simplifies design, provides unconditional stability without external compensation, and allows accurate determination of lag and lead frequencies. Only Radiation's RA-909 Amplifier offers the characteristics needed for such an application.

Feedback components are selected to optimize overall preamplifier parameters without regard to the active element in this configuration.

Transfer characteristics are:

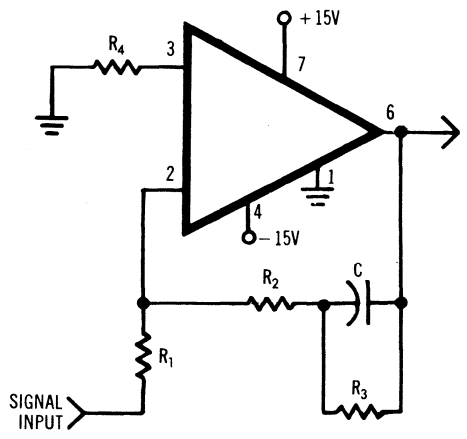
$$\frac{E_{out}}{E_{in}} = -\left[\frac{R_2 + R_3}{R_1}\right]\left[\frac{1 + j\,\omega\tau_1}{1 + j\,\omega\tau_2}\right]$$

Where: $\tau_1 = \frac{R_2R_3}{R_2 + R_3}$ and $\tau_2 = R_3C$

Frequency of lag and lead are defined by:

$$f_{lag} = \frac{1}{2\pi\tau_2};\ f_{lead} = \frac{1}{2\pi\tau_1}$$

For a gain of 100, the preamplifier roll-off will be 70 kHz. Undistorted output voltage is 26.0 $V_{p\text{-}p}$.



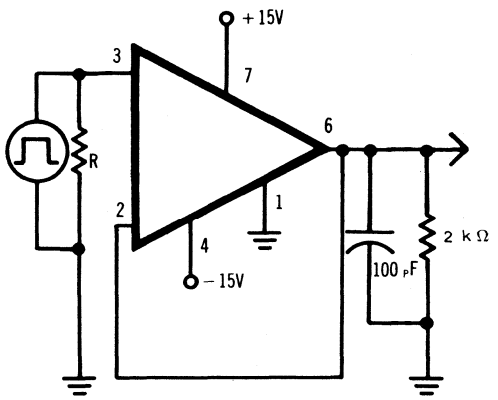
UNITY GAIN BREADBOARD

OPERATIONAL AMPLIFIER

This application of the HA-909 Operational Amplifier, illustrates the outstanding performance characteristics of this unique circuit. It provides the 6 db/octave high-frequency roll-off required for unconditional stability in operational feedback connections without use of external compensation . . . even for the critical unity gain configuration.

Performance Characteristics:

$V_{in} = V_{out}$:	200 mV
Rise time:	40 ns
Overshoot:	15%
Slew rate:	5 V/μs
Bandwidth:	7 MHz
Phase Margin:	60°



HIGH-Q BANDPASS FILTER

Harris's Dielectric Isolation, in conjunction with a virtually ideal circuit, permits design of high Q active filters with high initial attenuation. The HA-909 Amplifier has an extremely high internal feedback impedance, and allows wide flexibility in the choice of external filter components without regard to the active element of the circuit.

The filter shown features a Q of 100 at a center frequency of 10 kHz.

The filter transfer function is:

$$\frac{E_{out}}{E_{in}} = \frac{jxy}{1 + y(1 - x^2) + jx}\ ;\ \text{where}$$

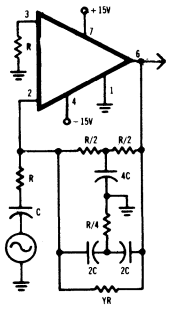
$$x = \frac{f}{f_l} \cdot f_l = \frac{1}{2\pi RC} \cdot f_o = f_l\left[\frac{1+y}{y}\right]^{1/2}$$

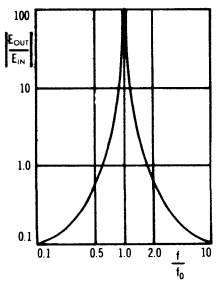
$$Q = y\left[\frac{1+y}{y}\right]^{1/2}$$

f_o = center frequency
f_l = lower 3 dB frequency

Typical response curve shows exceptionally high Q obtainable with RA-909 in this application. Q = 100, f_o = 10 kHz, E_{out} = ±13.0V.

Initial attenuation as determined by y is approximately 40 dB per decade. Final attenuation is approximately 20 dB per decade below unity gain.





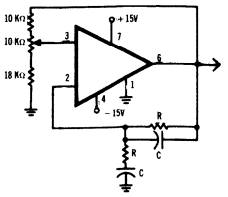
WIEN BRIDGE OSCILLATOR

The flexibility of the HA-909 Operational Amplifier is indicated by this application. Here, the Amplifier is used in the design of a highly stable, uncompensated Wien Bridge Oscillator which is virtually unaffected by temperature variations.

Using the HA-909 you may select a wide range of RC combinations without regard to the active element of the circuit. Frequency of oscillation (up to 500 kHz) is defined by:

$$f_o = \frac{1}{2\pi RC}$$

In this application, the amplifier offers the following typical performance characteristics: @ f_o = 10 kHz; Undistorted E_{out} = 26.0 V_{p-p} with R_L = 2kΩ
@ f_o = 150 kHz; Undistorted E_{out} = 11.2 V_{p-p} with R_L = 2kΩ



PHASE-DELAY FILTERS

The HA-909 Operational Amplifier provides greater flexibility in the design of monolithic Phase-Delay Filters. It's unique design produces unconditional stability without external compensation, and allows accurate determination of phase shift.

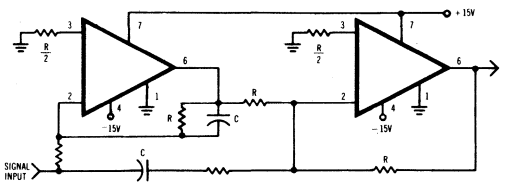
Feedback components are selected to determine the 90° phase shift frequency, without regard to the active elements in this configuration.

The transfer characteristic is:

$$\frac{E_{out}}{E_{in}} = \frac{1 - jx}{1 + jx} \text{ where } x = \frac{f}{f_o}.$$

90° phase-shift frequency is: $f_o = \frac{1}{2\pi RC}$

X is the normalized frequency ratio referenced to the 90° phase-shift frequency. For $f_o \leq 70$kHz, output voltage is 26.0V_{p-p}.



HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 502

HA-909 OPERATIONAL AMPLIFIERS PERFORMANCE TAILORING

BY DON JONES

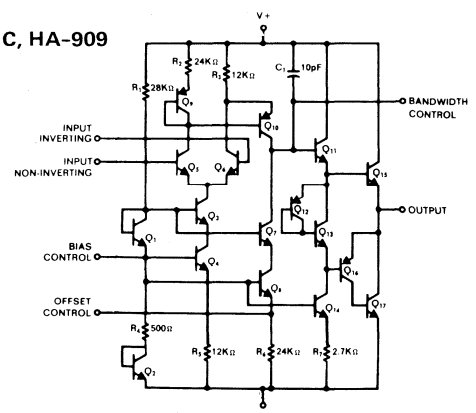
INTRODUCTION

In most applications, the HA-909 operational amplifier family will approach the theoretical "ideal" op amp requiring only connections to the power supplies and to feedback components determined from classical analog computer theory. This results from the exceptionally wide bandwidth of the HA-909 combined with internally compensated 6 dB per octave frequency rolloff and high impedance, low drift, low noise input characteristics.

Nevertheless, in the unlimited number of possible operational amplifier applications, there are those in which certain performance factors may need to be optimized. These performance factors include offset, power dissipation, bandwidth, large signal bandwidth, slew rate, transient response, and stability with reactive loads. The Harris HA-909 combines a design which minimizes the necessity for added external components with the availability of internal circuit points which allow the altering of performance characteristics.

The schematic of the HA-909 family is shown in Figure 1. The circuit nodes connected to the device pins on the HA-909 for performance tailoring are the Offset Control, the Bandwidth Control, and the Bias Control. The HA2-909, an 8-lead metal can version, has only the Bandwidth Control available.

FIGURE 1.
SCHEMATIC, HA-909



OFFSET ADJUSTMENT

In many applications, the guaranteed offset voltage of the HA-909 family is sufficiently small that no connection to the offset control pin is required. In some high precision or high gain DC amplifier applications, it may be desired to set the room temperature offset voltage to zero. Figure 2 shows the proper connection of a single 200K ohm potentiometer to accomplish this. Selected fixed resistors in a voltage divider circuit could also be used; the upper leg between the bias control pin and the offset control pin could be a fixed value of about 120K ohms and the lower leg between the offset control pin and -V could be a value usually between 50K and 100K ohms selected to yield zero offset.

Figure 3 shows offset voltage change with temperature for one unit with and without room temperature offset zeroing. These curves should not be regarded as "typical" since offset can be of either polarity and the temperature slope can be in either direction. In general, room temperature zeroing of offset voltage results in lower temperature coefficients of offset voltage.

FIGURE 2.
OFFSET ADJUSTMENT, HA-909

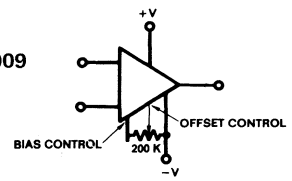
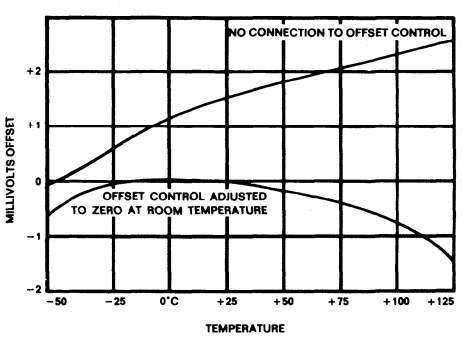


FIGURE 3.
OFFSET VOLTAGE vs. TEMPERATURE



BANDWIDTH ADJUSTMENT

A unique feature of the HA-909 family of operational amplifiers is wide bandwidth (typically 7 MHz) combined with internal compensation for 6 dB per octave rolloff. This assures stable operation at any gain with resistive loads, plus superior transient response and full power bandwidth.

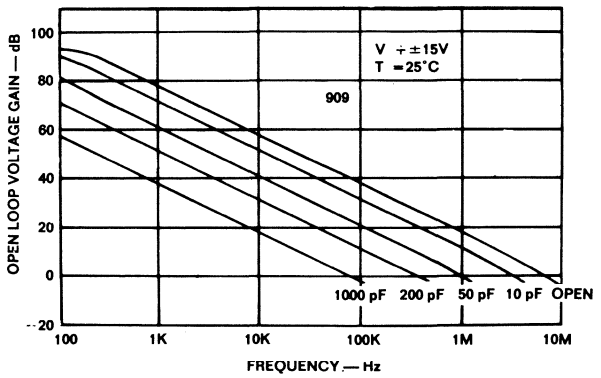
In certain instances, such as when driving reactive loads or when the amplifier is part of a servo loop, it may be desirable for stability to reduce the bandwidth while maintaining the 6 dB per octave rolloff characteristic. Also, in certain systems, it may be desirable to attenuate frequencies above a certain value or to limit transient response.

Connection of a capacitor from the bandwidth control pin to ground will move the first break point on the open loop frequency response curve to a lower frequency while retaining the 6 dB per octave rolloff (Figure 4).

The effective built in capacitance is about 10 pF, so the new bandwidth with external capacitance connected is approximately $Bw = Bwo \times \frac{10}{C+10}$; where Bwo is the bandwidth without external capacitance and C is the external capacitance in pF. Slew rate and full power bandwidth will be reduced by the same factor as the bandwidth.

The Bandwidth Control pin may also be used to limit the output swing by connecting diodes at this point to reference voltages. This pin is a high impedance point which carries the same voltage swing as the output pin offset by about +1.5 volts.

FIGURE 4.
OPEN LOOP FREQUENCY RESPONSE



FREQUENCY RESPONSE VS. CAPACITANCE FROM BANDWIDTH CONTROL PIN TO GROUND.

BIAS CONTROL ADJUSTMENT

Bias Control refers to control of internal device quiescent currents and should not be confused with the Input Bias Current parameter.

Referring to the HA-909 schematic in Figure 1, the current in all stages of the amplifier is determined by the resistor-diode string consisting of R1, Q1, R4, and Q2. The impedance at the collector of Q10 which drives the rolloff capacitor, C1, is directly proportional to the current through R4 and Q2. This current is approximately 1.0 mA at supply voltage of ±15 volts; 0.65 mA at ±10 volts; or 1.35 mA at ±20 volts. As a result, the bandwidth and slew rate measured with supplies of ±20 volts are nearly double the values measured at ±10 volts. It is possible to control bandwidth, slew rate, and to some extent open loop gain by adding or subtracting current through R4 and Q2 by connecting a resistor from the supply voltage to the Bias Control pin.

Adding bias control current by connecting a resistor between the positive supply and the Bias Control pin may be desirable to achieve maximum bandwidth or slew rate, particularly when supply voltages less than ±15 volts must be utilized. Reducing bias control current by connecting a resistor between the negative supply and the bias control pin has much the same effect as adding capacitance to the Bandwidth Control pin but may be desirable to minimize power supply current.

Figure 5 shows the change in D. C. open loop gain with supply voltage and external bias control current normalized to the gain measured at ±15 volt supplies and the Bias Control pin open.

FIGURE 5.
OPEN LOOP GAIN WITH BIAS CURRENT

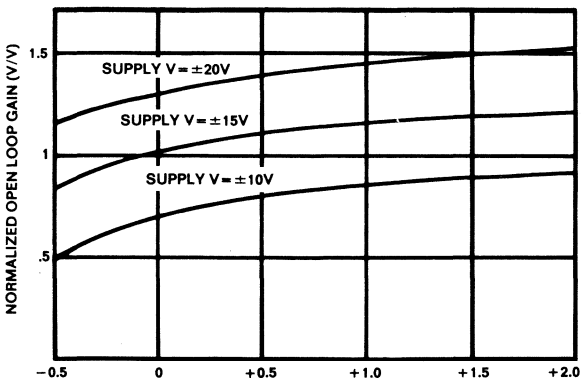


FIGURE 6.
OTHER PARAMETER CHANGES WITH BIAS CURRENT

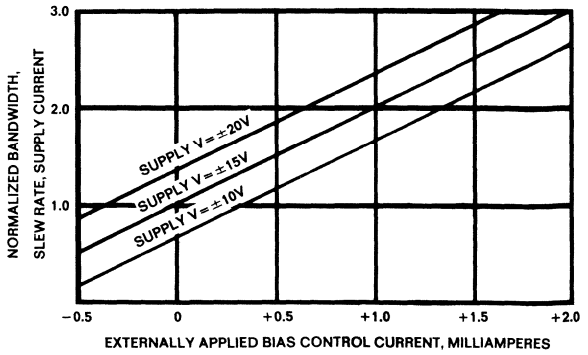
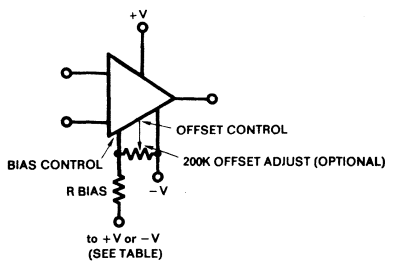


Figure 6 refers to changes in slew rate, bandwidth, large signal bandwidth for a fixed output level, and power supply current with respect to changes in supply voltage and external bias control current. These curves are normalized with respect to the parameters measured at ±15 volt supplies and the Bias Control pin open. It can be seen that these parameters can be increased to those normal at a higher supply voltage by adding bias control current; 0.35 mA added at ±10 volts brings the performance up to the normal 15 volt level and 0.35 mA added at ±15 volts brings the performance up to the normal 20 volt level.

Obviously the maximum output voltage swing cannot be increased by adding bias control current, but actually tends to decrease by about 1 volt at 2 mA bias control current. Bias control currents from 2 to 5 mA increase the parameters even more but instability at unity gain may result from reduced phase margin.

Figure 7 shows the typical external resistance required for various bias control currents at different supply voltage levels.

FIGURE 7.



BIAS RESISTOR SELECTION

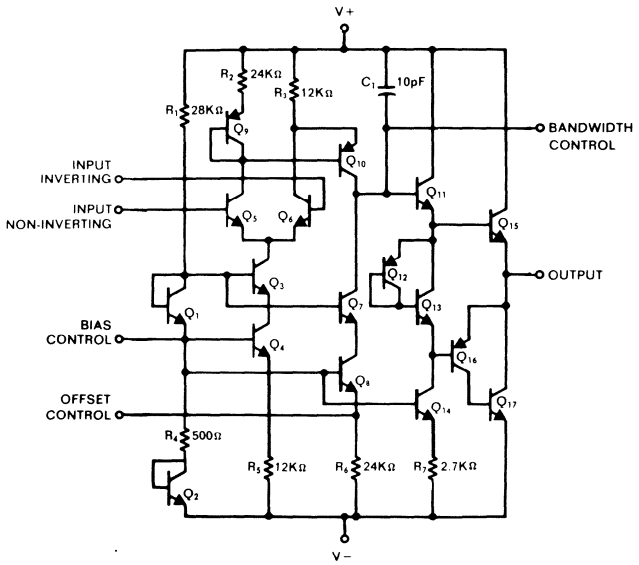
External Bias Current mA	Connect R Bias to:	R Bias In Ohms At Supply Voltage:		
		±10V	±15V	±20V
−0.5	−V	1.7K	2K	2.4K
+0.5	+V	39K	57K	77K
+1.0	+V	18K	28K	38K
+1.5	+V	12K	21K	27K
+2.0	+V	9K	14K	19K

CONCLUSION

For most applications, no connections are required at the Offset, Bandwidth, or Bias Control pins; they are simply terminated at an isolated solder pad on the PC Card.

The versatility provided by these control points allows the HA-909 to be used in many special applications so that a single op amp type can be used for virtually all op amp requirements in a system.

HA-909 SCHEMATIC



HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 504

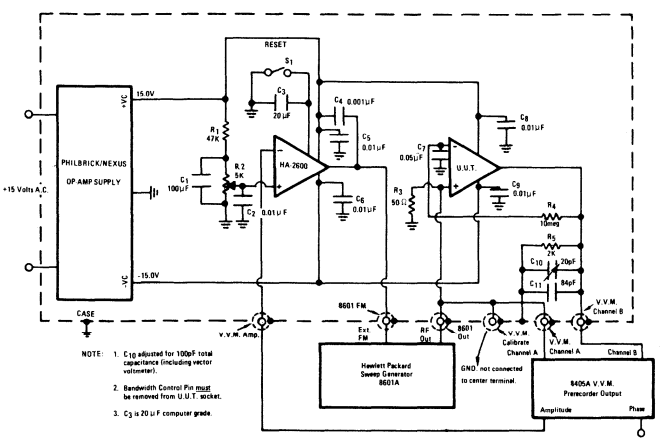
AUTOMATIC PHASE MARGIN TESTING

BY G. G. MILER

APP. NOTES

In order to test a large number of operational amplifiers for characterization of new products, an automatic testing system is needed to measure the phase margin and the unity gain bandwidth. This test system should be fast and easy to operate.

The phase margin is normally measured by adjusting the frequency of a signal generator until the open loop voltage gain of the operational amplifier is unity. The phase shift can be measured with a vector voltmeter such as the Hewlett Packard Model 8405A. This procedure, however, is slow because of the time required to adjust the oscillator to the unity gain frequency. Also, a skilled operator is needed to make the necessary adjustments for this measurement.



The test can be automated by driving a voltage controlled oscillator to the unity gain frequency using a HA-2600 as a comparator as shown below. The inverting input is connected to the recorder output of the 8405A vector voltmeter. The non-inverting input of the HA-2600 is connected to reference voltage which is adjustable between zero and one volt. The output of the HA-2600 is connected to the external FM input of the sweep generator. The output of the HA-2600 drives the sweep generator until the output voltage of the vector voltmeter is equal to the voltage at the non-inverting input, which is set by R_2. R_2 should be adjusted so that the signal on Channel B is the same level as Channel A. The sweep rate of the sweep generator must be limited so that the phase locked oscillator of the vector voltmeter can maintain proper lock. The sweep rate can be limited by greatly reducing the slew rate of the HA-2600. This reduction can be accomplished by connecting a 20 µF computer grade capacitor between the bandwidth control pin and ground.

The RF signal level must be kept small to prevent the results from being affected by the slew rate (power bandwidth) of the unit under test (U.U.T.). The signal level should be between five and ten millivolts for the HA-909 and HA-2600. The unity gain frequency can be determined by using a frequency counter or it can be calculated by using

the sweep generator setting and the output voltage of the HA-2600 comparator.

The center frequency of the sweep generator and the frequency range of the vector voltmeter should be set for the typical unity gain frequency of the unit under test. The sweep should be disabled on the sweep generator, while adjusting the equipment. The output level of the sweep generator should be set to 707 millivolts. The Channel B probe is connected to the V.V.M. calibrate jack. Channel A and B amplitudes can be checked and the phase meter can be zeroed. Channel B probe is then connected to the output of the unit under test. If phase lock is lost when a unit is inserted in the socket, it can be restored by depressing the reset button. Depressing the reset button drives the sweep generator to the center frequency. It may be necessary to reset the sweep generator center frequency and the vector voltmeter range if the unity gain frequency is more than five MHz from the typical unity gain frequency. The signal generator level and R_2 can be set to measure the phase shift at any predetermined gain if desired.

R_4 provides D.C. feedback to reduce the effects of offset voltage. C_7 removes the high frequency components from the feedback. Therefore, the U.U.T. is operating open loop at high frequency. The lead dress is very critical when the phase margin is being measured on wideband operational amplifiers. All of the vector voltmeter leads should be the same length and they should be as short as possible. The signal generator should be terminated with a 50 Ω resistor at the test socket.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 505

A HIGH IMPEDANCE HYSTERSIS CIRCUIT

BY G. G. MILER

APP. NOTES

A hysteresis amplifier is often needed for Schmitt triggers, analog simulation, differential comparators, and for servomechanisms. Frequently the hysteresis amplifiers used in these circuits are required to have a high input impedance and a low input current to avoid disturbing the input signal. The threshold voltages should be independent of the signal source impedances.

The input current introduces an error in the thresholds, which is equal to the product of the input current and the source resistance. The hysteresis circuit uses positive feedback from the output to the noninverting input of the operational amplifier. Coupling between the output and the source through the input resistance of the operational amplifier can cause multiple triggering unless the differential input resistance of the operational amplifier is large compared with the source resistance. An input impedance of 100 megohms and a bias current of two nanoamperes is obtainable with modern high impedance operational amplifiers.

It is frequently necessary to limit the output swing to some convenient levels, such as standard logic levels. The output voltage of current limited devices can be clamped; however, this will create an unnecessary amount of power dissipation.

The output voltage of the circuit can also be limited by using a series resistor between the operational amplifier and a clamp. In this case, the output of the operational amplifier is allowed to swing through its full range. However, this will limit the available output current and will require additional switching time for the output to slew through its full range. On the HA-2520 or HA-2620 the output voltage can be limited by placing a clamp at the bandwidth control point. The bandwidth control point is a high impedance point, which is at the same voltage as the output.

Figure 1 shows a simple hysteresis circuit in which the output voltage is clamped at the bandwidth control point. Let the thresholds, E_T, be defined by:

$$E_T = E_{10} \pm \frac{\Delta E_1}{2} \qquad (1)$$

Where E_{10} is the input threshold offset voltage. The output voltage limits are E_0, defined by:

$$E_O = E_{00} \pm \frac{\Delta E_0}{2} \qquad (2)$$

Where E_{00} is the output offset. The total threshold offset, E_{TO} is defined as:

$$E_{TO} = E_{00} - E_{10} \qquad (3)$$

The voltage at the noninverting input, E_1, is given by:

$$E_+ = \frac{R_1}{R_1 + R_2} E_0 \qquad (4)$$

The threshold of the hysteresis circuit occurs when E_- is equal to E_+. It can be shown that:

$$\Delta E_+ = \frac{R_1}{R_1 + R_2} \Delta E_0 \qquad (5)$$

Since ΔE_I is equal to ΔE_+ it is obvious that R_1 can be found by:

$$R_1 = \frac{\Delta E_I}{\Delta E_0} (R_1 + R_2) \qquad (6)$$

$R_1 + R_2$ is chosen to be some convenient resistance.

The next step is to calculate the reference voltage, E_R. R_1 and R_2 form a voltage divider between E_R and E_0. Therefore, the reference voltage can be calculated by:

$$E_R = E_{00} - E_{TO} \left(\frac{R_1 + R_2}{R_2}\right) \qquad (7)$$

As an example, let the output swing between -0.5 and 5.5 volts. The output is diode clamped to these levels as shown in Figure 2. Let the threshold be at ±1.5 volts and let $R_1 + R_2$ be 4.4K.

$$R_1 = \frac{\Delta E_I}{\Delta E_O} (R_1 + R_2) =$$

$$\frac{3.0}{6.0} \times 4.4K = 2.2K \qquad (8)$$

Therefore:

$$R_2 = (R_1 + R_2) - R_1 =$$

$$4.4K - 2.2K = 2.2K \qquad (9)$$

The output offset is 2.5 volts and the input offset is zero. Therefore, the total offset voltage is 2.5 volts.

$$E_R = E_{OO} - E_{TO} \left(\frac{R_1 + R_2}{R_2}\right) =$$

$$2.5 - 2.5 \left(\frac{4.4K}{2.2K}\right) = 2.5 \text{ volts.} \qquad (10)$$

An HA-2620 is used because it has an extremely high input impedance. An HA-2520 could also be used if faster switching times are desired.

The hysteresis circuit triggers approximately 70 millivolts early because the output voltage begins to drop when the input is within 75 millivolts of the threshold. The maximum current through the diode clamps is only several hundred microamps and remains constant if the differential input voltage is greater than 100 millivolts. Therefore, output voltage remains constant within a few millivolts unless the input is near the threshold. The threshold voltages and the output voltages vary by only a few millivolts from one device to the next. The circuit functions properly with a variation in the threshold voltage of less than ten millivolts when the source resistance is 10 megohms.

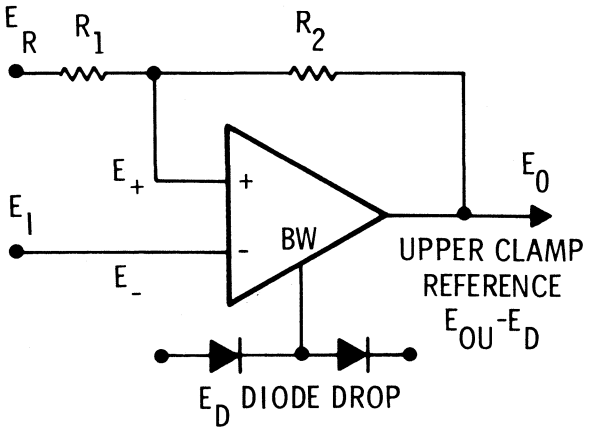


Figure 1

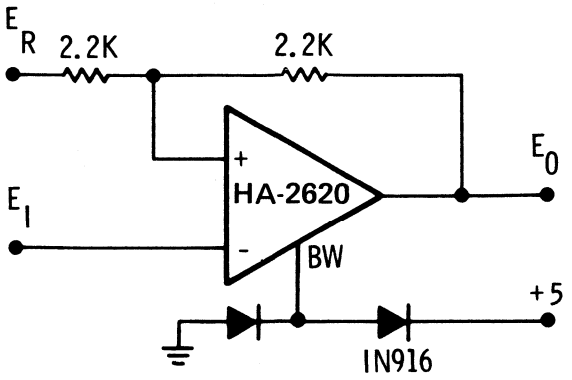


Figure 2

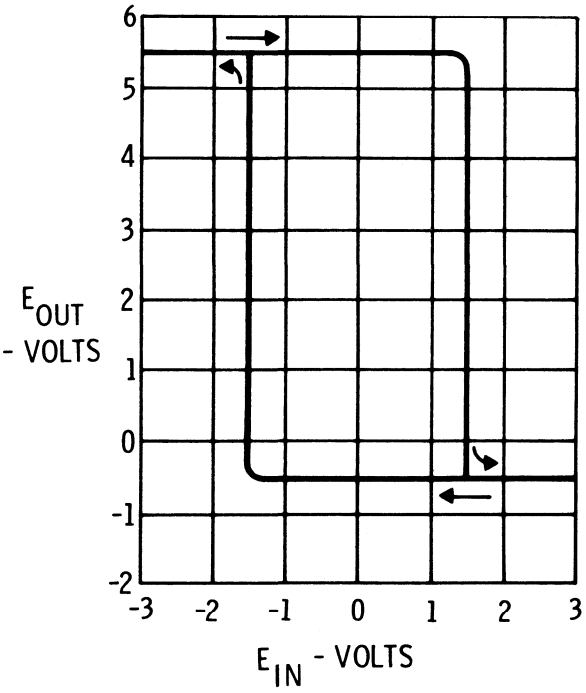


Figure 3. Output Voltage vs. Input Voltage for HA-2620 Hysteresis Amplifier

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 506

EQUIVALENT INPUT NOISE MEASUREMENTS ON HIGH GAIN MONOLITHIC OPERATIONAL AMPLIFIERS

BY G. G. MILER

Signal-to-noise ratio is very important in the design of communications and control systems. The resolution and accuracy of these systems is greatly dependent upon the signal-to-noise ratio.

The R.M.S. noise power of a broad band noise source is proportional to the square root of the bandwidth. Therefore, the signal-to-noise ratio can be improved if the bandwidth can be reduced. It is also desirable to keep all resistances to a minimum because the broad band noise of a resistor is proportional to the square root of the resistance.

The input stage is the prime noise contributor within the device if the first stage gain is large. The noise of the later stages is small compared to the amplified noise of a high gain first stage. In addition to the noise generated within the device, there is a noise current between the inputs. This noise current will generate a voltage across the source resistance.

There are two types of noise generated within operational amplifiers. One is the thermal, which is a broad band white noise; the other is a noise which is inversely proportional to the frequency ($\frac{1}{f}$ noise). The $\frac{1}{f}$ noise is generally negligible above 10kHz.

Figures 1, 2, 3, and 4 show the Broad Band Noise vs. Bandwidth for four popular Harris Semiconductor operational amplifiers. The noise is measured with a true R.M.S. voltmeter, which has a low frequency three dB point of ten Hertz. The operational amplifiers are connected to have various 3dB bandwidths ranging from 100Hz to 10MHz. The bandwidth of the HA-709R is controlled by using various combinations of compensation networks and closed loop gains. The bandwidths of the other Harris Semiconductor operational amplifiers are easily controlled by using various closed loop gains and capacitors on the bandwidth control point.

The noise bandwidth is the bandwidth of a filter which has a rectangular frequency response. This is not easily achieved in practice. The effective bandwidth of an amplifier can be determined by integrating the area under the frequency response curve. If the amplifier has a rolloff of 20dB per decade, the effective bandwidth is 1.57 times the 3dB bandwidth. The noise bandwidth shown is the 3dB bandwidth, since this will probably be more useful. The effective bandwidth can be found by multiplying the bandwidth shown by 1.57 since the rolloff is 20dB per decade.

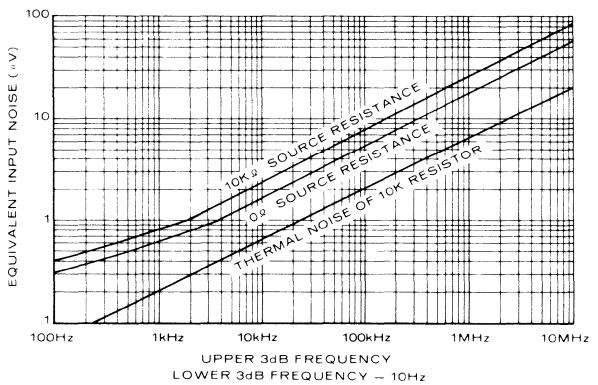


Figure 1. Equivalent Input Noise vs. Bandwidth for HA-2600

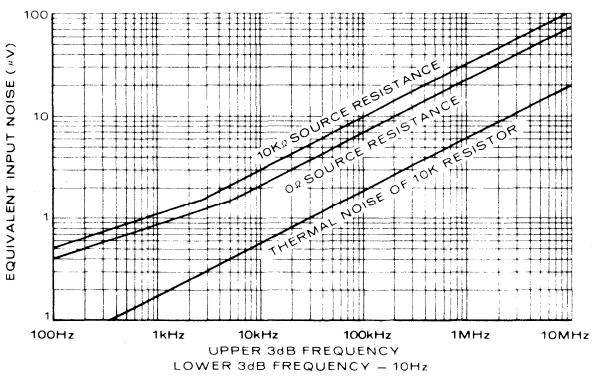


Figure 2. Equivalent Input Noise vs. Bandwidth for HA-2520

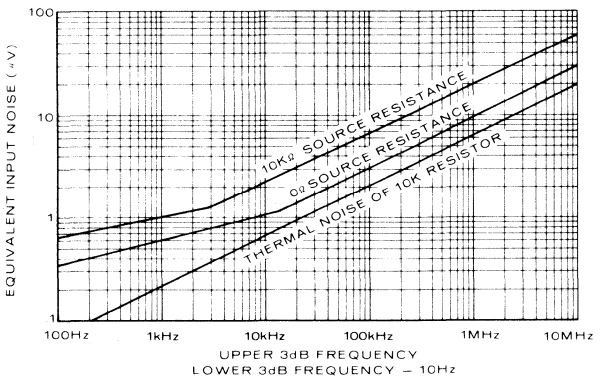


Figure 3. Equivalent Input Noise vs. Bandwidth for HA-909

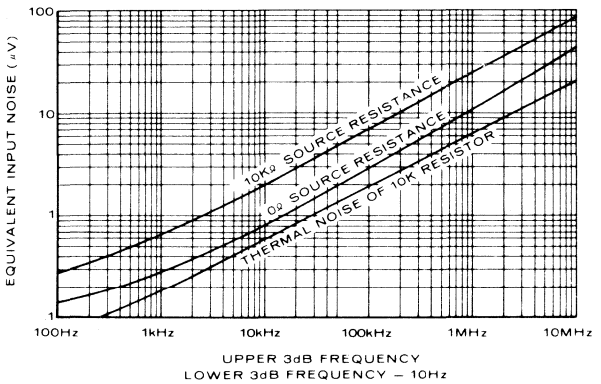


Figure 4. Equivalent Input Noise vs. Bandwidth for HA-709R

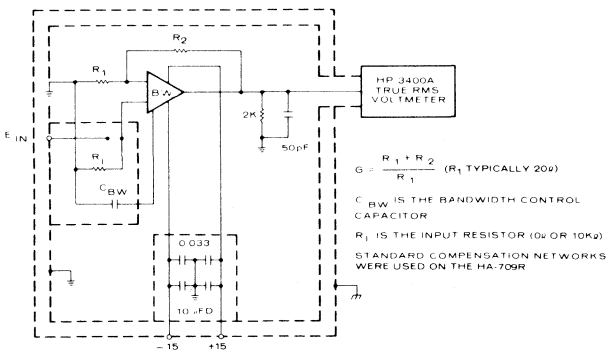


Figure 5.

Figure 5 shows the typical circuit used to measure the noise. The circuit is built in a double shielded box to reduce external noise. The power supply leads are filtered in a shielded compartment. The noise voltage is measured with a Hewlett-Packard 3400A True R.M.S. Voltmeter. The three dB bandwidth is measured by applying a signal to the input and determining the 3dB point with the True R.M.S. Voltmeter.

The zero source resistance curves show the equivalent input noise generated within the operational amplifier. The 10K Ω source resistance curve contains the sum of the internal equivalent noise, the thermal noise of a 10K Ω resistor and the noise voltage developed across the 10K Ω resistor due to the noise current. The thermal noise calculated for a 10K Ω resistor at 25°C is shown for comparison. This noise is calculated by $V_n = \sqrt{4KTRB}$, where K is the Boltzmann Constant (1.38×10^{-23} joules /°C), T is the temperature in degrees Kelvin, R is the resistance in ohms, and B is the effective bandwidth in Hertz.

The predominate noise at 100 Hertz is the $\frac{1}{f}$ noise. Generally, between one and ten kHz, the thermal noise becomes more important.

Figure 4 shows the typical broad band noise for the HA-709R. The HA-709R is a radiation hardened version of the standard 709 operational amplifier. It is apparent from Figure 4 that the $\frac{1}{f}$ noise of the HA-709R is very low.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 507

A SIMPLE FUNCTION GENERATOR USING OPERATIONAL AMPLIFIERS

BY G. G. MILER

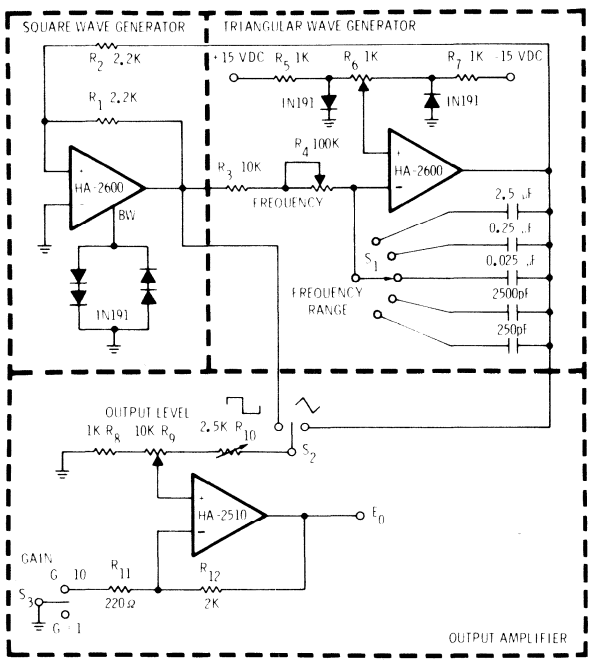


Figure 1

A function generator which produces square and triangular waveforms is frequently needed. Such a generator, using discrete components, is a relatively complex circuit. Figure 1 shows a very simple function generator which uses only three operational amplifiers. The amplitude of the square and triangular waveforms is variable from 0.2 to 20 volts peak-to-peak. The frequency range is from 1Hz to 100kHz. The rise time of the square wave is less than 450 nanoseconds. Rise times of less than 200 nanoseconds are obtainable at reduced amplitude. The slope of the triangular waveform is very linear. Very little change in frequency, amplitude, or waveform is observed with changes in supply voltages between ±10 and ±20 volts.

The square wave generator consists of a simple hysteresis circuit which is triggered by the triangular wave generator. The output voltage of the square wave generator is clamped to the desired level by diodes connected to the bandwidth control point. The four diodes shown give an output of two volts peak-to-peak. Two diodes will give one volt peak-to-peak output and a faster rise time. The ratio of the amplitude of the square wave to the triangular wave is equal to the ratio of R_1 to R_2. The rise time is generally limited by the slew rate of the operational amplifier. The best waveform is obtained by using an HA-2600 but much better rise times are obtainable using an HA-2620, HA-2510 or HA-2520 because of their higher slew rates.

The triangular wave generator consists of an integrator which integrates the output of the square wave generator. The frequency of the function generator is controlled by the ramp rate of the triangular wave. S_1 selects the integrating capacitor which changes the frequency range in decade steps. R_4 is the variable frequency control. The frequency of the function generator, f, is given by:

$$f = \frac{1}{4(R_3 + R_4)\ C} \left(\frac{R_1}{R_2}\right)$$

The symmetry of the waveform is adjusted by R_6, which controls the reference voltage of the integrator. The frequency will change if the symmetry is changed by more than approximately ten percent. The noninverting input of the op-amp can be grounded if it is not necessary to change the symmetry of the waveform. The resulting symmetry is very good. The HA-2600 is chosen because it produces the most accurate integration, having a typical input bias current of 3nA. The HA-2510 is preferable if it is necessary to operate the function generator at frequencies as high as 1MHz.

The output amplifier consists of a simple non-inverting amplifier using an HA-2510. The HA-2510 is chosen for its high slew rate of 50 volts per microsecond. S_3 selects a gain of one or ten. The variable output attenuator, R_9, sets the input level to the amplifier. R_{10} serves as an output level calibration control. The maximum output current should be limited to 20mA. The load impedance should not be less than 600Ω for a gain of ten and 50Ω for unity gain.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 508

TEST PROCEDURES FOR OPERATIONAL AMPLIFIERS

BY G. G. MILER

APP. NOTES

The offset voltage of the amplifier under test (A.U.T.) is measured as follows:

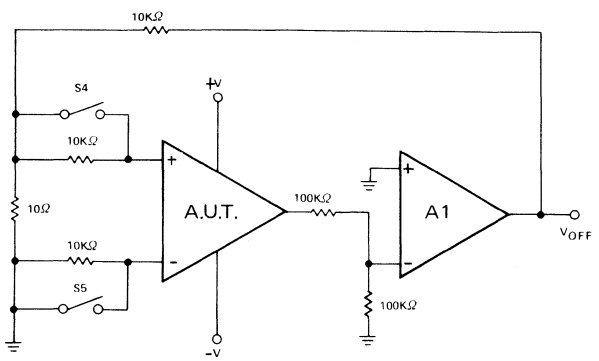
1. Set + and -V to the desired supply voltage and close S4 and S5.
2. Measure the voltage at V_{OFF}.

The offset voltage is equal to (V_{OFF}) (10^{-3}). The feedback amplifier, A1, drives the input of the A.U.T. so that the output is at ground reference, V_{OFF} is driven to 1000 times the voltage necessary to compensate for the offset voltage.

The bias current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and measure V_{OFF2}.
3. The plus input current is equal to $(V_{OFF2} - V_{OFF1}) \times 10^{-7}$.
4. Close S4 and open S5 and measure V_{OFF4}.
5. The minus input current is equal to $(V_{OFF4} - V_{OFF1}) \times 10^{-7}$.

TEST CIRCUIT FOR MEASUREMENT OF OFFSET VOLTAGE, BIAS CURRENT, AND OFFSET CURRENT 10KΩ

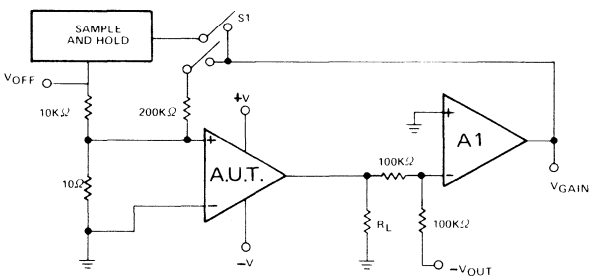


The bias current is equal to the average of the plus and minus input currents.

The input offset current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and S5 and measure V_{OFF2}.
3. The offset current is equal to $(V_{OFF2} - V_{OFF1}) \times 10^{-7}$.

TEST CIRCUIT FOR MEASURING OPEN LOOP VOLTAGE GAIN



The open loop voltage gain is measured as follows:

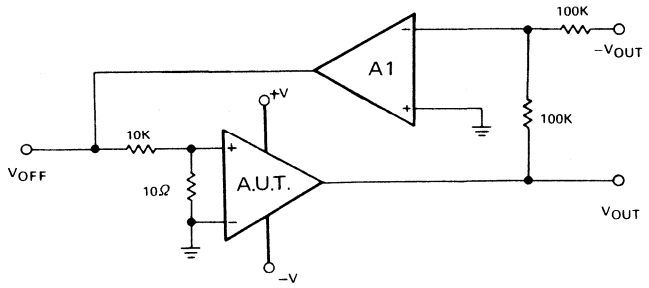
1. Set the +V and -V supply voltages to the desired value and set $-V_{OUT}$ to ground.
2. Close S1 so that the sample and hold will null the offset voltage.
3. S1 can be opened when the circuit stabilizes. The sample and hold will maintain the voltage which nulls the offset voltage.
4. Set $-V_{OUT}$ to the desired output voltage, $-V_4$ and measure V_{GAIN4}.
5. Set $-V_{OUT}$ to another output voltage, $-V5$ and measure V_{GAIN5}.

6. The gain is equal to

$$\left[\frac{V4 - V5}{V_{GAIN4} - V_{GAIN5}}\right] \times 20{,}000.$$

$-V_{OUT}$ can be first set to zero and then to −10 volts. This gives the gain in the plus direction. The gain in the minus direction can be determined by using zero and +10 volts. The average gain can be determined by using output voltages of −10 and +10 volts.

TEST CIRCUITS FOR MEASUREMENT OF COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO



Common Mode Rejection Ratio:

1. Set +V to +20 VDC, -V to -10 VDC, V_{OUT} +5 VDC by applying -5 VDC to $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC, -V to -20 VDC, V_{OUT} to -5 VDC by applying +5 VDC to $-V_{OUT}$.
4. Measure $| V_{OFF2} - V_{OFF4} |$ <1.0 VDC.

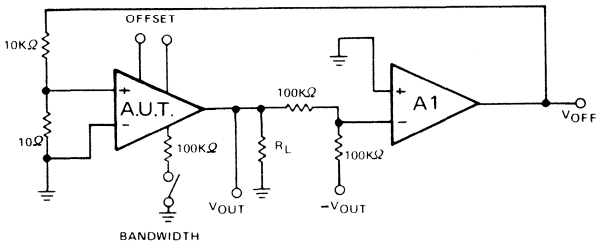
The +1.0 volt limit corresponds to a rejection ratio of 80 dB.

Power Supply Rejection Ratio:

1. Set +V to +20 VDC, -V to 15 VDC, V_{OUT} to ground by grounding $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC.
4. Measure $| V_{OFF2} - V_{OFF4} |$ <1.0 VDC.
5. Set +V to +15 VDC, -V to -10 VDC.
6. Measure V_{OFF6}.
7. Set -V to -20 VDC.
8. Measure $| V_{OFF6} - V_{OFF8} |$ <1.0 VDC.

The ±1.0 volt limit corresponds to a rejection ratio of 80 dB.

TEST CIRCUITS FOR MEASURING OUTPUT VOLTAGE/CURRENT, POWER DISSIPATION, AND CONTINUITY CHECKS

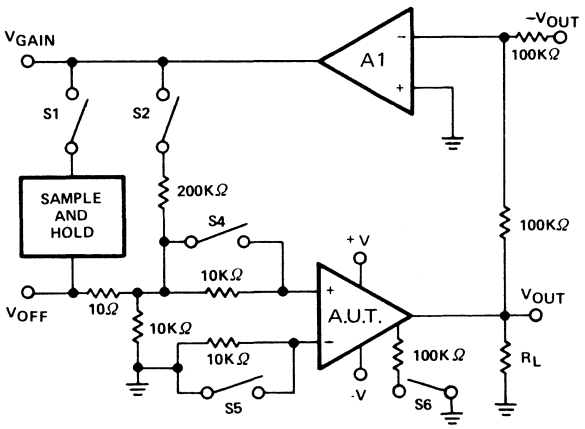


The output voltage/current is measured by connecting a load resistor, R_L, to the output of the A.U.T. The value of R_L is chosen to yield an output current which is the minimum acceptable output current at the desired output voltage. The amplifier under test is programed to a voltage greater than the desired output voltage by applying an equal but opposite polarity voltage to $=V_{OUT}$. The output voltage, V_{OUT}, is measured to see if it reaches the desired output voltage. This test is performed driving the output positive and driving the output negative.

The power dissipation is measured by driving the output voltage to zero by grounding $-V_{OUT}$ and measuring the current in one of the power supply leads.

The continuity of the bandwidth control point is checked by applying −5V to $-V_{OUT}$ and grounding the bandwidth control point through a 100K resistor. V_{OUT} should be less than one volt. There is a known relationship between the voltage at the bandwidth control point and the output voltage, V_{OUT}. This relationship depends on the device type. The continuity of the offset control points is determined by measuring the voltage at these points. These voltages will be slightly less than the positive supply voltage for the HA-2600 and the HA-2500.

SIMPLIFIED SCHEMATIC OF THE COMPLETE D.C. TEST CIRCUIT FOR OPERATIONAL AMPLIFIERS



HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 509

A SIMPLE COMPARATOR USING THE HA-2620

BY G. G. MILER

APP. NOTES

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

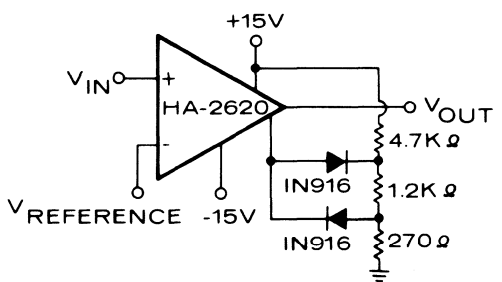


FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

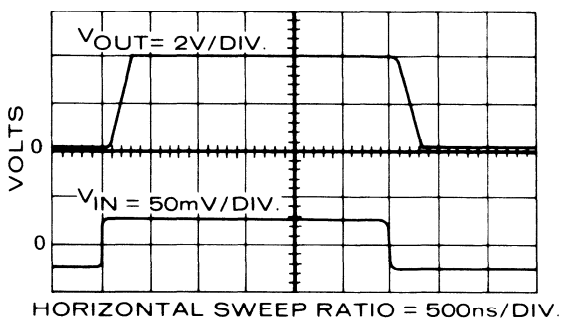


FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 510

A SIMPLE SQUARE-TRIANGLE WAVEFORM GENERATOR

BY G. G. MILER

APP. NOTES

Figure 1 shows a very simple function generator which uses only three operational amplifiers. The amplitude of the square and triangular waveforms is variable from 0.2 to 20 volts peak-to-peak. The frequency range is from 2.5 Hz to 250 kHz. The rise time of the square wave is less than 100 nanoseconds. The slope of the triangular waveform is very linear. Very little change in frequency, amplitude, or waveform is observed with changes in supply voltages between 10 and 20 volts.

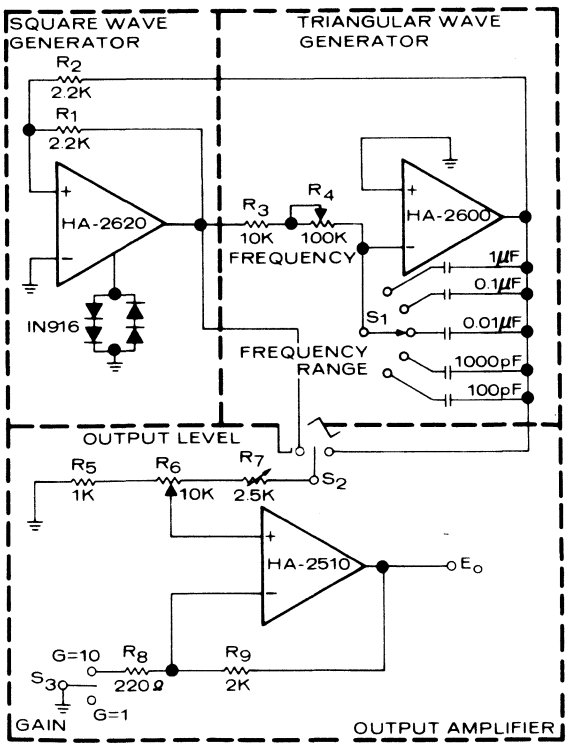


FIGURE 1

The square wave generator consists of a simple hysteresis circuit which is triggered by the triangular wave generator. The output voltage of the square wave generator is clamped to the desired level by diodes connected to the bandwidth control point. The circuit shown gives an output of two volts peak-to-peak. The ratio of the amplitude of the square wave to the triangular wave is equal to the ratio of R_1 to R_2. An HA-2620 is chosen for the comparator because it has very low input currents, high slew rate and wide bandwidth.

The triangular wave generator consists of an integrator which integrates the output of the square wave generator. The frequency of the function generator is controlled by the ramp rate of the triangular wave and the threshold levels of the hysteresis circuit. S_1 selects the integrating capacitor which changes the frequency range in decade steps. R_4 is the variable frequency control. The frequency of the function generator, f, is given by:

$$f = \frac{1}{4(R_3 + R_4)\,C}\left(\frac{R_1}{R_2}\right)$$

Better high frequency operation can be obtained by reducing the value of R_3 and R_4. Very long periods can be obtained by increasing the value of R_3, R_4 and the integrating capacitor. The HA-2600 is chosen because it produces the most accurate integration, having a typical input bias current of 1 nA. The HA-2620 can be used for the integrator. It may be necessary to add some external compensation to prevent ringing if an HA-2620 is used.

The output amplifier consists of a simple non-inverting amplifier using a HA-2510. The HA-2510 is chosen for its high slew rate of 50 volts per microsecond. S_3 selects a gain of one or ten. The variable output attenuator, R_6, sets the input level to the amplifier. R_7 serves as an output level calibration control. The maximum output current should be limited to 20mA. The load impedance should not be less than 600Ω for a gain of ten and 50Ω for unity gain.

HARRIS SEMICONDUCTOR

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APPLICATION NOTE 511

DIGITAL TO ANALOG CONVERTER APPLICATIONS

BY DON JONES

GENERAL USES

D to A converters are useful in any system where both digital and analog signals are present. Some of the more common applications include:

1. Data processing output interface; driver for displays, plotters, etc.
2. Programmable power supply or function generator in automatic test equipment.
3. Tool interface in numerical controlled machining.
4. Interface for automatic process control to control temperature, flow rates, etc.
5. Digital communications: digital to audio interface.
6. Feedback network in A to D converters.

TERMINOLOGY

A definition of some of the terms and parameters encountered in D to A conversion will be helpful to those being introduced to the field.

Resolution: An indication of the number of possible analog output levels, usually expressed as the number of input bits that the converter will handle. For example, an eight (8) bit binary weighted converter will have $2^8 = 256$ possible output levels (including zero). This should not be confused with accuracy, which is sometimes also expressed as a number of bits.

Accuracy: A measure of the deviation of the analog output level from its predicted value under any input combination. This can be expressed as a percentage of full scale, a number of bits (N bits accuracy = $\frac{1}{2}^N$ possible error,) or a fraction of the least significant bit (if a converter with M bits resolution has 1/2 L.S.B. accuracy the possible error is $\frac{1}{2} \times \frac{1}{2^M}$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. The importance of accuracy vs. resolution depends on the application. Possible errors in individual bit weights which may be cumulative with combinations of bits; errors in the summation of individual bit weights and changes in these due to temperature variations.

Least Significant Bit (L.S.B.): The digital input bit carrying the lowest numerical weight; or the analog level shift associated with this bit, which is the smallest possible analog step.

Most Significant Bit (M.S.B.): The digital input bit carrying the highest numerical weight; or the analog level shift associated with this bit. In a binary weighted converter the M.S.B. creates a half of full scale level shift.

Settling Time: The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. It should be noted that the transition from one level to another is not always smooth; spikes and ringing may occur.

THE HI-1080 MONOLITHIC D TO A CONVERTER

The Harris Semiconductor HI-1080 is the first monolithic integrated circuit D to A converter complete with the thin film resistor ladder network on the same chip as the switching devices. Along with the advantages of small size and monolithic reliability, this allows higher speed and faster settling. Also it has the advantage over separate switches and ladder networks in that overall performance is guaranteed and there is no need to add the possible errors of separate components.

The functional diagram of the HI-1080 is shown in Figure 1. An external reference supply, usually 5 volts, is connected between the +REF and the -REF pins. The output levels will be directly proportional to the differential reference voltage. Variations of the other +5 volt and the -15 volt power supplies have negligible effect on the analog output. Either the +REF or the -REF pin may be grounded, so reference supplies of either polarity may be accomodated. The smaller value resistors between +REF and T_1 or between T_2 and T_3 may be externally shorted out, or an external trimmer substituted, for fine adjustment of the full scale output level. The positive side of the reference supply may be connected to T_2 or T_3 for a 10 volt nominal output swing, which is useful in bipolar operation.

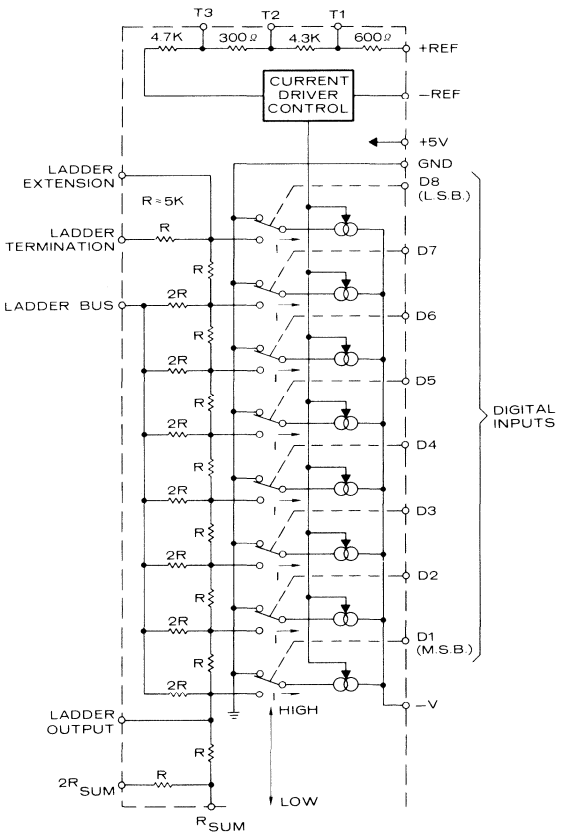


Figure 1. Functional Diagram HI-1080

The reference level is conditioned through the current driver control where the output current of each of the eight current drivers is determined.

The use of current sources to drive the ladder network has several advantages over voltage sources. Within the constant current range of the sources, the current, and hence the differential ladder output voltage, will remain constant regardless of variations in the negative supply voltage and the voltage of the ladder return bus. The ladder bus may be returned to a voltage other than ground if desired for offset or bipolar outputs without affecting its output. The digital and analog grounds can be effectively separated for noise free operation. Also switching of a current source rather than a voltage source generally is faster, creates less ringing at the output, and produces smaller power supply transients.

The digital inputs effectively switch the current source outputs either to the ladder network or to ground. The inputs are fully compatible with any standard 5 volt DTL or TTL logic circuits. A "high" input ($>$ +2 volts) switches the current source to ground; a "low" input ($<$+0.8 volts) switches the current source to the ladder, creating a more negative output voltage. This polarity convention should be kept in mind when designing with the HI-1080.

The ladder network is constructed from high stability metal film resistors deposited on the same silicon chip. Identical material is used for the resistors in the reference supply network and in the current source circuitry to achieve good temperature stability. The "R – 2R" ladder network is used rather than a weighted resistor network because identical resistors will match better in value and temperature coefficient. Extra resistors are provided at the R Sum and 2R Sum terminals which are very useful for feedback or summing with external amplifiers or comparators, since these resistors will track almost perfectly with the ladder source resistance. Provision is made at the other end of the ladder for cascading converters for higher resolution.

A block diagram is shown in Figure 2 and schematics of the block in Figures 3 – 5.

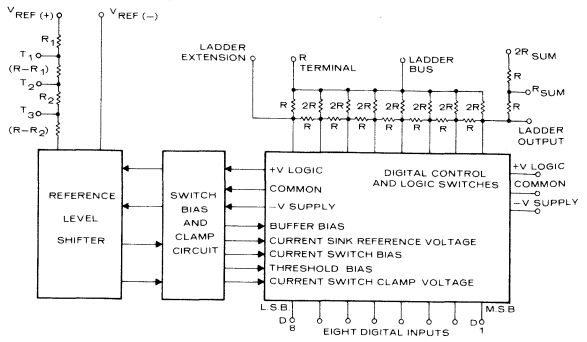


Figure 2. 8 Bit D/A Converter Block Diagram

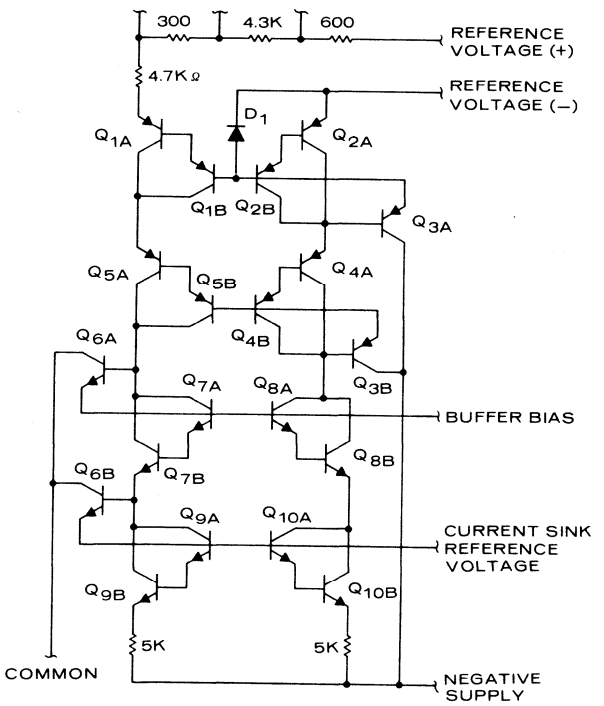


Figure 3. D/A Converter Reference Level Shifter

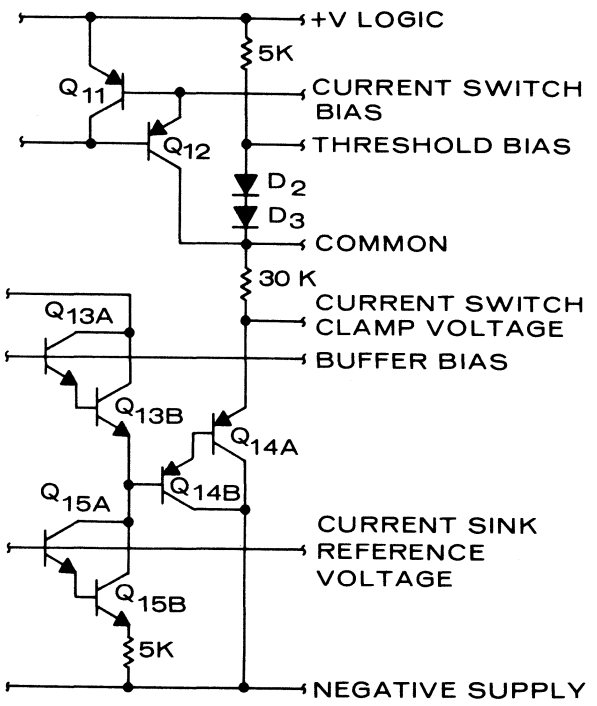


Figure 4. D/A Converter Current Switch Bias & Clamp Circuit

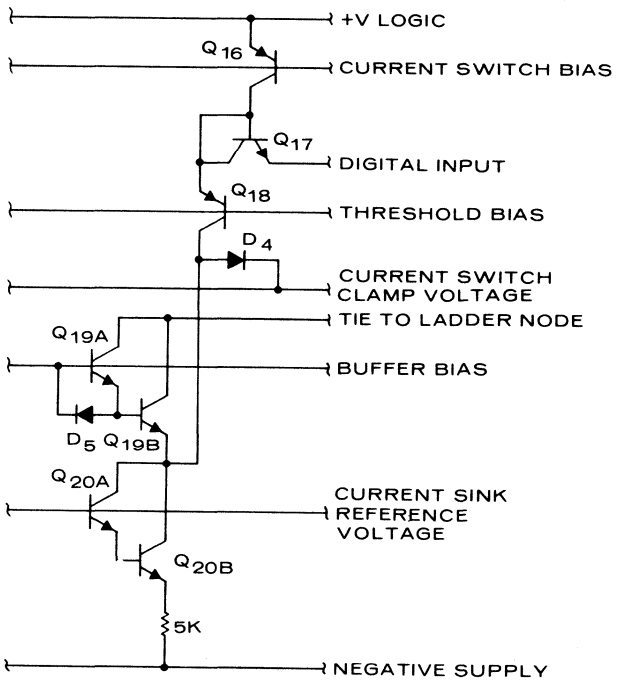
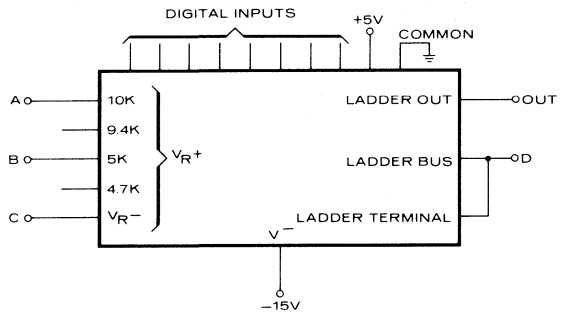


Figure 5. D/A Converter Ladder Current Switch

OPERATING MODES

Some of the possible operating modes of the HI-1080 are illustrated in Figure 6. Since both the reference supply terminals and the ladder bus terminal can be connected to any voltage within ±5 volts with respect to power supply ground, a number of output polarity modes can be achieved. In all cases the ladder output will become more negative with respect to the ladder bus as a digital input is changed from the high to the low state.



MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALL LOW	CONNECTIONS			
		A	B	C	D
UNIPOLAR ZERO REFERENCE	0 TO − [V_R+ − 1 L.S.B.]	V_R+	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+ / V_R+/ TO [0 + 1 L.S.B.]	V_R+	N.C.	GND	V_R+
BIPOLAR	/V_R+/ TO [−V_R+ 1 L.SB]	N.C.	V_R+	GND	V_R+

Figure 6. D/A Converter Operation Modes

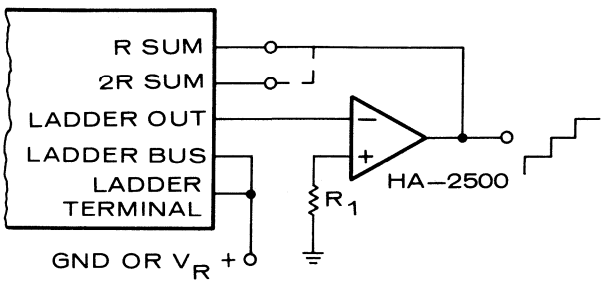
In the unipolar – zero reference mode, the ladder bus is grounded. Using negative logic convention (high = 0, low = 1), the output will increase in the negative direction with increasing input binary number. Either side of the reference supply may be grounded.

In the unipolar – zero full scale mode, the ladder bus is connected to the positive reference voltage, so the output will be always positive with respect to the reference ground. Now, using positive logic convention (low = 0, high = 1), the output will increase in the positive direction with increasing binary number. It may be necessary to connect V_R+ to a lower tap in series with a potentiometer to adjust the zero level.

The bipolar mode connection is similar to the previous mode except the V_R+ is connected to T_2 (or T_3 through a pot), so that the full scale excursion is now 10 volts. With all inputs low, the output will be most negative (about -4.96V). With only the M.S.B. high, the output will be zero volts. With all inputs high, the output will be at V_R+.

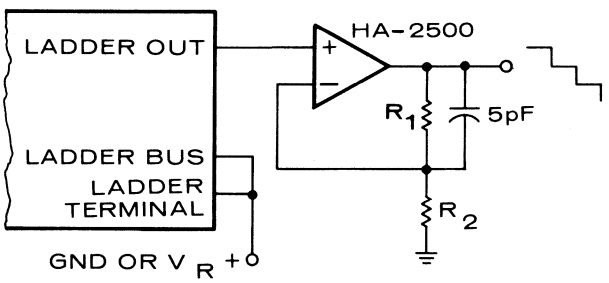
AMPLIFIER CONNECTIONS

Figure 7 illustrates connections from the converter to an operational amplifier. The inverting connection uses the summing registers provided on the chip for amplifier feedback. Since the ladder impedance is nominally 5K ohms, connection of the output to R Sum will result in a gain of -1. Connection to 2_R Sum will result in a gain of -2. Any of the operating modes discussed previously may be used.



FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO :	R_1
+4.98V	R_{SUM}	2.5K
+9.96V	$2R_{SUM}$	3.3K

INVERTING OUTPUT
(MORE POSITIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)



OUTPUT RANGE: SAME AS SHOWN ON 'OPERATING MODE' CHART

MULTIPLIED BY $\frac{R\,2}{R_1 + R_2}$

NON–INVERTING OUTPUT
(MORE NEGATIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

Figure 7. Buffer Amplifier Connection

For a noninverting output the operational amplifier is wired in the conventional manner. The R Sum or 2R Sum resistor could be used to sum an external analog signal of opposite polarity at the amplifier input.

The Harris Semiconductor HA-2500 operational amplifier is recommended for high speed applications since its slew rate of 25 volts per microsecond is sufficient to follow the converter output steps very closely. For more moderate speed applications, the Harris Semiconductor HA-2600 operational amplifier is recommended for better offset drift while retaining a minimum slew rate of 4 volts per microsecond. Booster stages may be added to the amplifier outputs to drive any required load.

CASCADED D TO A CONVERTERS

Two HI-1080 units may be cascaded to achieve resolutions from 9 to 15 bits, using the ladder extension terminals, as illustrated in Figure 8. Note that input D8 of the higher significant bit unit is not used. This is necessary in order to join the two ladders correctly.

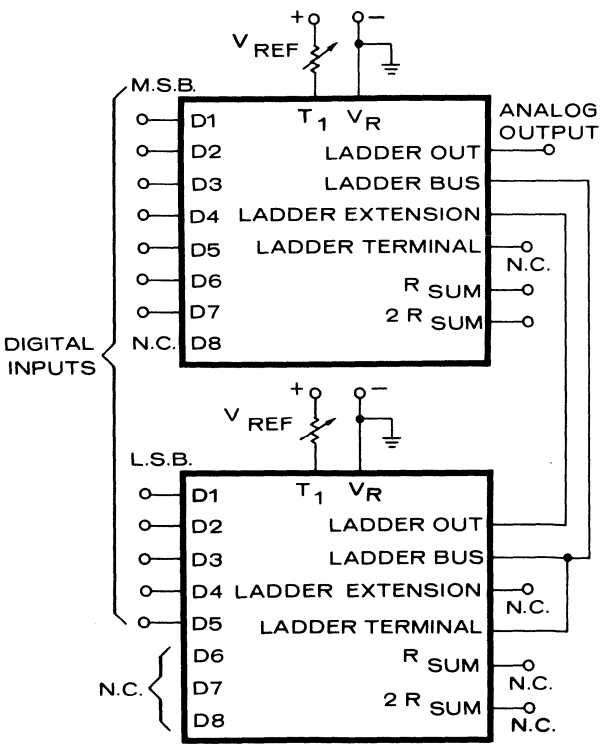


Figure 8. Cascaded Units for 12 Bit Resolution

A person might ask, "Why would anyone want a 12 bit converter with only 8-1/2 bit accuracy?" The answer is that most applications require accuracy expressed as a percentage of actual output rather than as a percentage of full scale output. One feature of the R – 2R ladder network is that errors in terms of millivolt deviation from the predicted output tend to become smaller as the lesser significant bits only are exercised. So for the 12 bit converter shown, with outputs between 1.25 and 5 volts the errors may be on the order of ±10 millivolts; but for outputs between 0 and 20 millivolts the errors will tend to be less than 0.7 millivolts.

A TO D CONVERTER; UP-DOWN COUNTER TYPE

A high speed D to A converter can be used as the heart of several very useful types of A to D converters. The up-down counter, or servo type converter is most efficient in monitoring one analog signal continuously, rather than monitoring multiplexed analog signals.

The converter works basically by balancing the input analog signal with the D to A output, adjusting the D to A by running a digital counter up or down as required to balance the signal. When the two analog signals balance, the counter state represents the digital equivalent of the input signal.

In the example shown in Figure 9, the two analog signals are fed differentially into an op-amp. For a positive input signal, the D to A could be run in the positive output mode, or in the negative output mode by summing the two signals at the inverting amplifier input. The amplifier gain should be set at 2 or greater to allow less critical thresholds for the comparators.

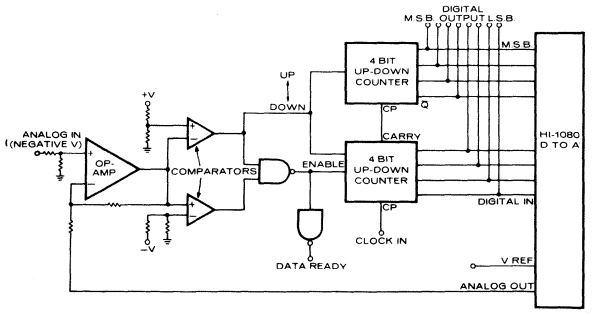


Figure 9. "Up-Down Counter" Type A to D Converter

The two comparator thresholds are set up by voltage dividers to correspond to unbalances of approximately ±1/2 L.S.B. When the analog signals are balanced within this range, the comparator outputs are both high, which stops the counters and gives a Data Ready signal to indicate that the digital outputs are correct.

If the analog signals are unbalanced by more than ±1/2 L.S.B., the counter is enabled and driven in the up or down direction depending on the polarity of the unbalance.

If the D to A converter is operated in the negative output mode, the digital outputs will follow negative logic convention.

If the analog input signal varies by less than 1 L.S.B. per clock period, the converter will continuously track the signal.

The Data Ready signal could be useful in adaptive systems for most efficient data transfer, since that signal changes state only when there is a significant change in the analog input. When monitoring a slowly varying input, it would be necessary to read-out the digital output only after a change has taken place. The Data Ready signal could trigger a flip-flop to flag this condition and the flip-flop would be reset after read-out.

The main disadvantage of the up-down counter converter is the time required to initially acquire a signal, which in an 8 bit system, could be up to 256 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking rate of the converter.

A TO D CONVERTER, SUCCESSIVE APPROXIMATION TYPE

Suppose you were asked to guess a secret number between 0 and 15 by asking the least number of questions answerable by yes or no. One of the most efficient ways might work as follows:

"Is it 8 or greater?"

"Yes"

"Is it 12 or greater?"

"No"

"Is it 10 or greater?"

"Yes"

"Is it 11?"

"No"

If you had jotted down a "1" for each "yes" and a "0" for each "no", you would have 1010, which of course is the binary notation for ten. So it is possible to find one number out of 16 with 4 questions. Likewise 8 questions would be required to find a number between 0 and 255. Obviously this technique is usually much quicker than saying, "Is it zero?", "Is it one?", etc., or guessing numbers at random.

The successive approximation converter shown in Figure 10 uses the same technique to find which proportional number between 0 and 255 best approximates the input analog voltage.

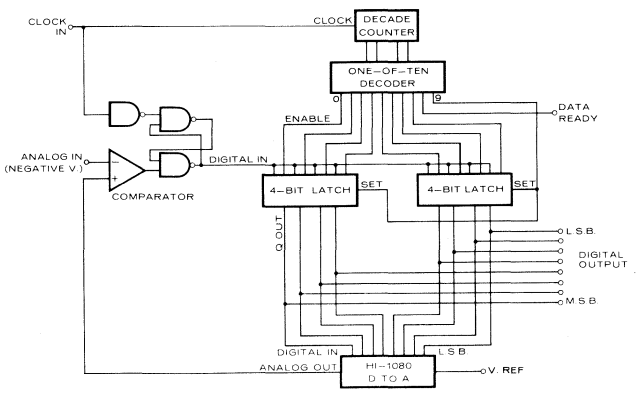


Figure 10. Successive Approximation Type A to D Converter

This is accomplished in 8 clock cycles – two additional cycles are used in this design to hold the data and to clear the registers, but this could be done during the eighth cycle, if necessary. The measurement starts with all zeros programmed into the D to A and the decade counter set to zero. The decoder enables the first of eight latches and the clock pulse sets a flip-flop composed of two cross-coupled gates setting a "1" in the first latch, so the D to A has a 10,000,000 input. The D to A consequently produces a half-scale output which goes to one side of the comparator. The comparator now effectly asks the question "Is the input greater than half-scale?". If the answer is "yes", the comparator output is high and the flip-flop remains set. If the answer is "no" the comparator resets the flip-flop during the second half cycle of the clock, resetting the first latch to zero.

On the second clock cycle the decoder enables the second latch while the last state of the first latch remains stored in it and remains as the D to A, M.S.B. input. In a similar manner, the state of the second M.S.B. is decided and the decoder moves on to the third. After the eighth clock cycle the conversion is complete, which is signaled by the Data Ready line on the ninth cycle. At the tenth cycle all latches are reset to be ready for the next conversion.

In practice, the delay of the clock pulse through the counter and decoder should be less than the delay through the three gates for proper timing.

Polarities shown are correct for the D to A connected in the negative output mode, and the digital output will be correct in negative logic. A positive analog input can be handled by summing with the D to A output at one comparator input, or by operating the D to A in the positive output mode and shifting the digital polarities as necessary.

It is necessary in any successive approximation converter for the analog input to remain constant during the conversion.

In multiplexed systems this is usually accomplished with a sample-and-hold circuit in the analog line.

It can be seen that the successive approximation type will give the correct output in eight clock cycles while the up-down counter type could take up to 255 cycles to acquire a signal. Once acquired, the up-down counter can indicate a change in a slowly varying signal within one clock cycle, while the successive approximation type must step through another eight cycles. The choice really depends on the type of signals to be monitored.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 512

COUNTER TYPE A TO D CONVERTER

BY DON JONES

INTRODUCTION

This paper describes circuit details for a full temperature range eight-bit A to D converter employing a unidirectional digital counter and a D to A converter. As shown in the simplified diagram in Figure 1, circuit operation is quite simple. A multiple stage counter circuit is driven from a clock and the counter output drives a D to A converter producing a staircase voltage ramp. When the D to A output voltage equals the analog input voltage, the comparator changes state, and at that instant, the counter state represents the digital equivalent of the analog input.

The heart of this circuit is the HI-1080 Eight-Bit D to A Converter, which is a monolithic integrated circuit containing both the current switches and the R-2R ladder network. This features good speed and accuracy over $-55^{o}C$ to $+125^{o}C$ temperature range. The HI-1080 D to A converter is also very effective in up-down counter and successive approximation type A to D converters, which are described in other application notes.

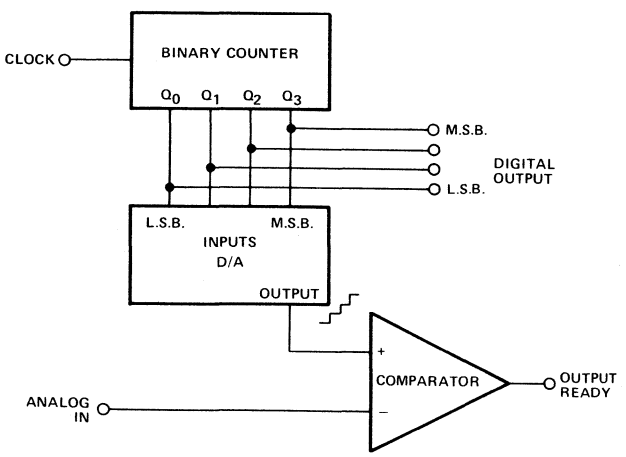


Figure 1. Simplified Diagram, Counter Type A/D

COUNTER vs. SUCCESSIVE APPROXIMATION TYPE CONVERTERS

The most popular A to D converter employing a D to A circuit is the successive approximation type. This type is useful for high speed conversion, since it requires only N clock cycles for an N-bit conversion, while the counter type requires up to 2^N cycles. One disadvantage, where many conversions per second are not needed, is that a sample-and-hold circuit is nearly always required in the analog signal path. The sample-and-hold circuit is an additional error source which is difficult to control over a wide temperature range. The counter type converter does not require a sample-and-hold circuit, since its output is a parallel digital number taken at the instant that the D to A and input signals are equal, although filtering of the input signal may be desirable in some applications. The counter type converter illustrated here can perform 1,000 conversions per second, which is adequate for many applications.

CIRCUIT DETAILS

The complete circuit schematic is shown in Figure 2 and typical waveforms are illustrated in Figure 3. The digital circuits shown are 9300 types, but comparable circuits from other TTL families will work equally well if any functional differences are taken into account.

Since the D to A converter normally has a negative output level, a positive input signal is compared by resistive summation at one comparator input, using the summing resistor internal to the D to A which closely matches the D to A equivalent output resistance.

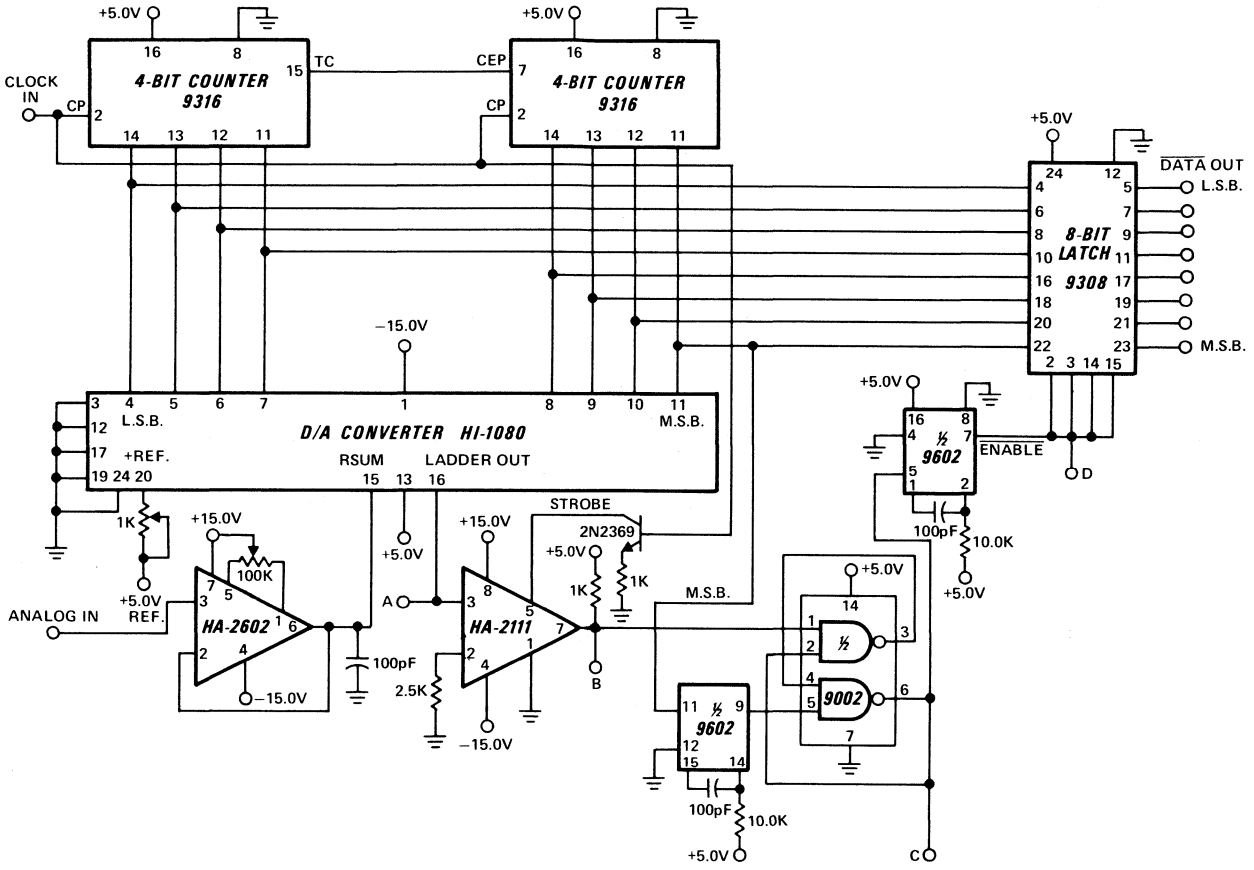


Figure 2. Complete A/D Schematic

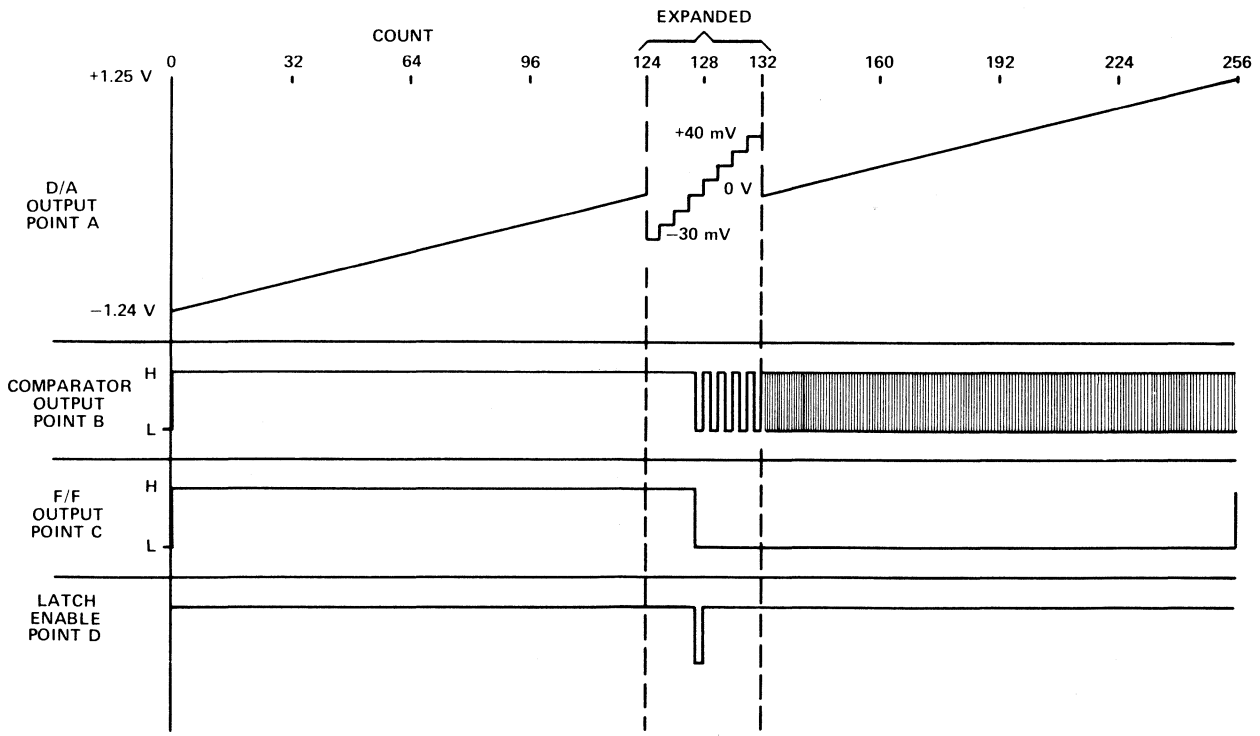


Figure 3. Waveforms with +2.50 Volts Analog Input

The comparator is strobed with the clock to prevent any D to A switching spikes from prematurely triggering the comparator. The strobing necessitates the use of the set-reset flip-flop formed by the cross-coupled gates so that the latch receives only one enable pulse per conversion cycle.

Note that the data output from the latch is the complement of the digital value, due to the polarity conventions of the D to A.

CIRCUIT ADJUSTMENT

For 0 to +5 volt input range the input op-amp is first zeroed in the conventional manner. Then +2.500 volts is applied to the input, and the pot between the reference supply and the D to A is adjusted so that the M.S.B. just trips in at this level. The full scale input will then be 1 L.S.B. below +5.000 volts which is +4.980 volts.

For 0 to +10 volts input range, connect the op-amp output to the 2R sum terminal on the D to A.

For 0 to −5 volt range, connect the op-amp output to the negative input of the comparator through a 5K ohm resistor.

For −5 volt to +5 volt bipolar operation, connect the ladder bus terminal on the D to A to the +5 volt reference, and connect the reference through the potentiometer to the T3 terminal of the D to A.

Virtually any other input range is possible by changing the op-amp gain or polarity, or adjusting the reference potentiometer. Zero shift may be accomplished by offsetting the ladder bus, or summing voltages at the op-amp or comparator inputs.

CIRCUIT PERFORMANCE

Accuracy is affected primarily by the D to A accuracy, and to a lesser degree by offsets in the input op-amp and the comparator. This circuit proved to be accurate within +½ L.S.B. at room temperature, and ±1 L.S.B. from −55°C to +125°C. This accuracy was maintained at clock rates up to 330 KHz. Clock rates up to 1 MHz could be used with about 1 additional L.S.B. of inaccuracy.

CIRCUIT VARIATIONS

Using the illustrated circuit as a starting point, many modifications to the digital circuitry are possible to suit the application.

For convert-on-command operation, the circuitry beyond the comparator, including the latch could be eliminated and the comparator output used to gate off the clock signal. The counters will hold their value until a command to convert again is issued by resetting the counters to zero.

For continuous conversion, a reduction in average (but not maximum) conversion time can be made by resetting the counters immediately after data is entered in the latches.

Another possible improvement in conversion time can be acheived by running the clock at a variable rate - fast while the D to A output is far from the input level and slower when the comparator is about ready to trip. One possibility is to use a VCO as the clock, controlled in frequency by an op-amp with inputs wired across the comparator inputs. Another possibility would be to use a fixed 5 MHz clock and insert a ÷16 counter in series with the clock line when the D to A and input voltages are nearly equal. This could be controlled by a second comparator with the trip point offset from that of the main comparator.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 514

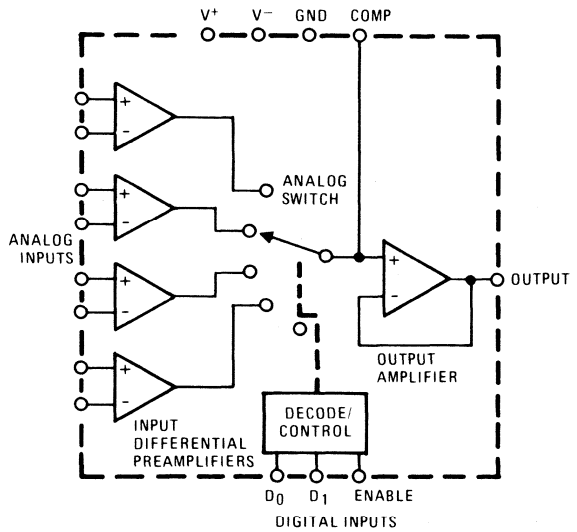
THE HA-2400 PRAM™ FOUR CHANNEL OPERATIONAL AMPLIFIER

BY DON JONES

APP. NOTES

INTRODUCTION

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

CIRCUIT CONNECTIONS

These inputs control the selection of the amplifier input channels in accordance with the truth table below:

D_0	D_1	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
H	L	H	OFF	ON	OFF	OFF
L	H	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \leq L \leq +0.8V$ $\quad +2.0V \geq H \geq +5.0V$

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

COMPENSATION

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A.C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

GAIN, VOLTS/VOLT		C_{COMP}	BANDWIDTH (TYPICAL)	SLEW RATE (TYPICAL)
NON-INVERTING	INVERTING	pF	(-3dB), MHz	VOLTS/μs
1	-	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40÷GAIN	50

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater

phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

APPLICATIONS

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

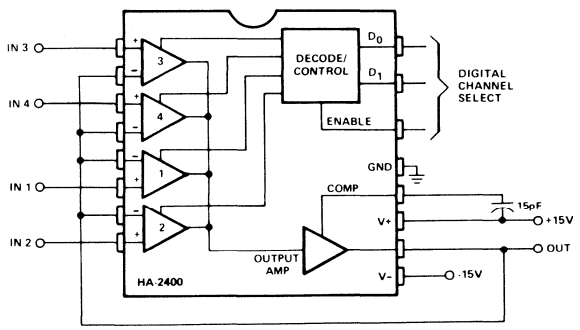
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs may be left floating, or grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

APPLICATION NO. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (—) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

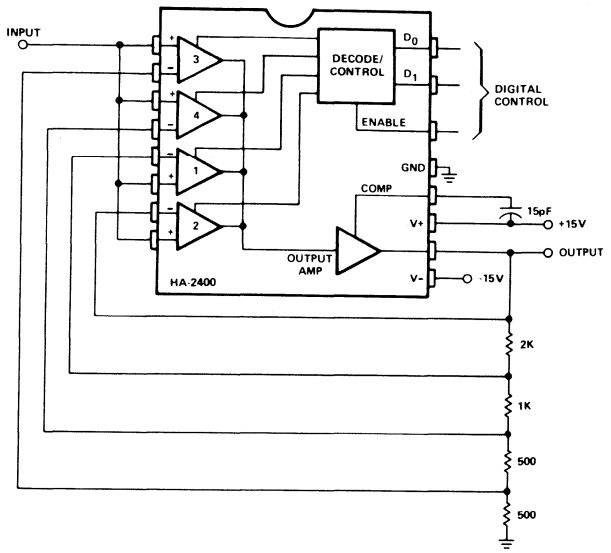
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

APPLICATION NO. 2



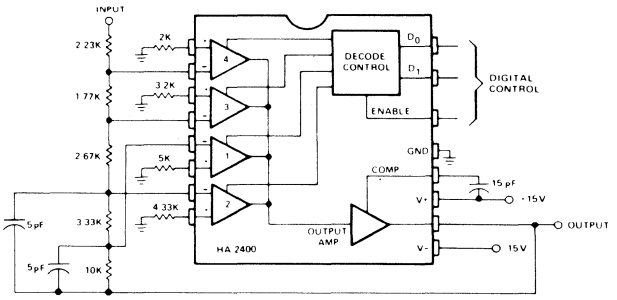
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

APPLICATION NO. 3

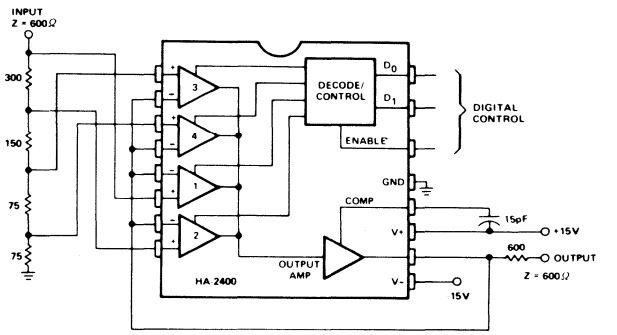


AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, −1, −2, −4 or −8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

APPLICATION NO. 4

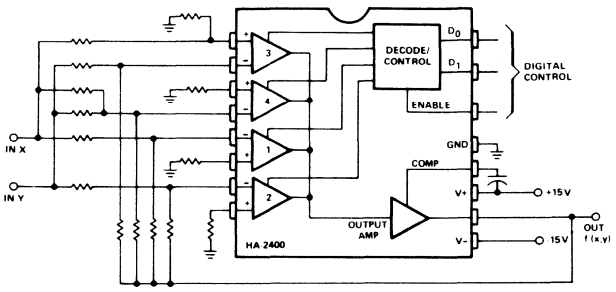


ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

APPLICATION NO. 5

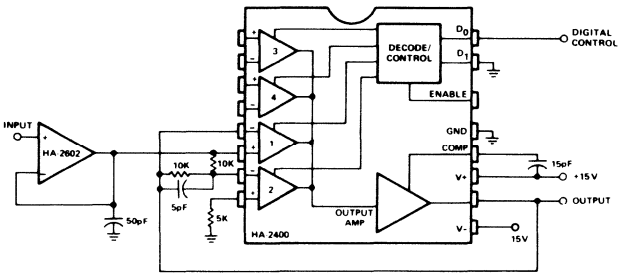


ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

APPLICATION NO. 6

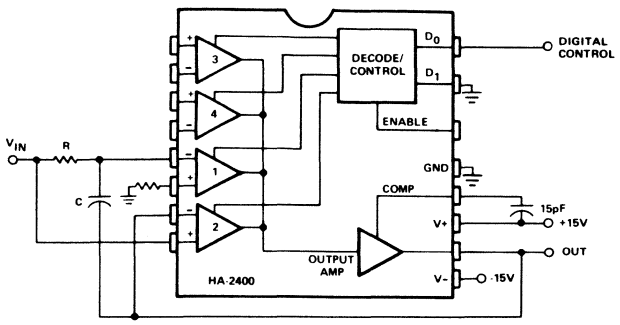


PHASE SELECTOR/PHASE DETECTOR/ SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D.C. output being proportional to the phase difference, with zero volts at $\pm 90^{o}$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

APPLICATION NO. 7

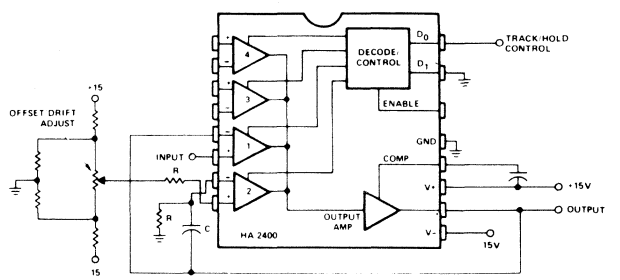


INTEGRATOR/RAMP GENERATOR WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D.C. input. Many variations are possible, such as programmable time constant integrators.

APPLICATION NO. 8



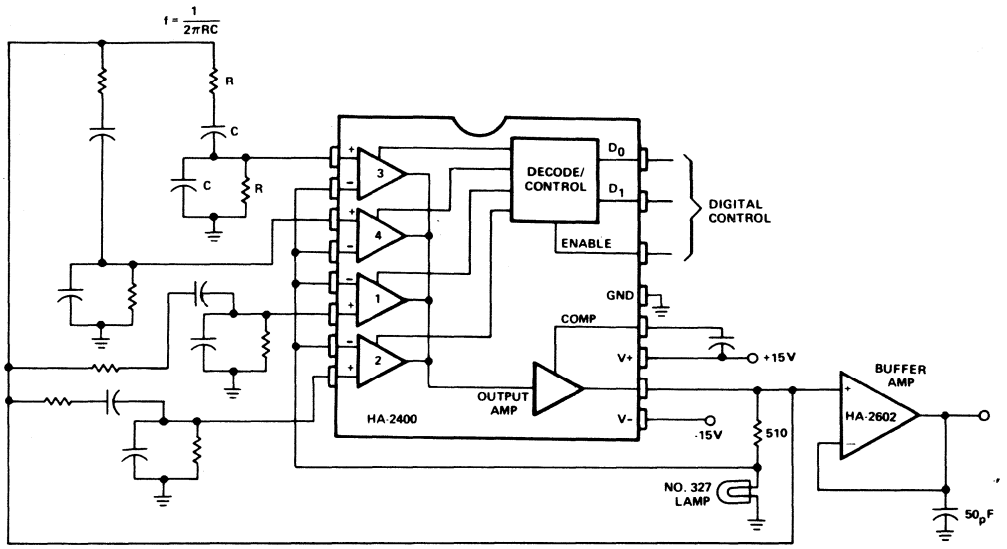
TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and

is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

APPLICATION NO. 9

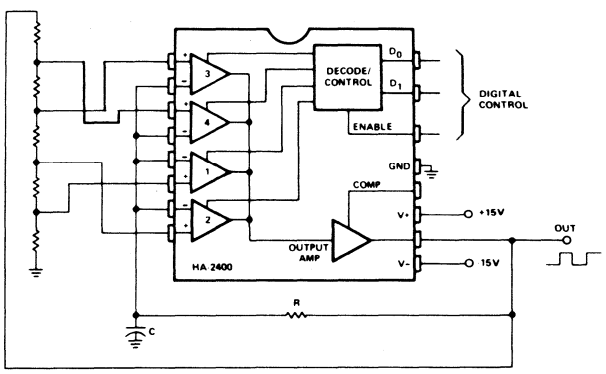


SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

APPLICATION NO. 10



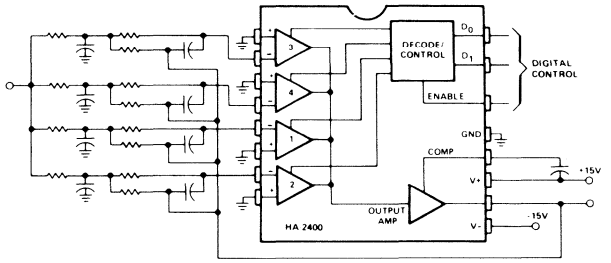
MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has

rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

APPLICATION NO. 11



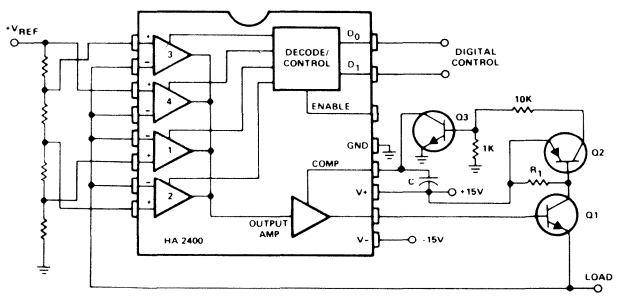
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

APPLICATION NO. 12

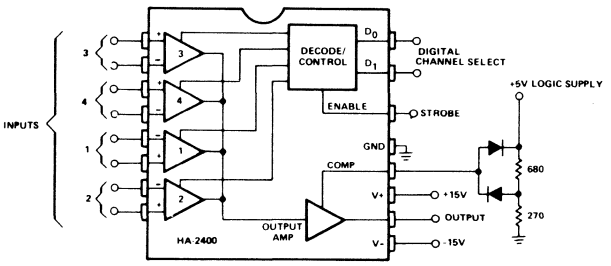


POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

APPLICATION NO. 13



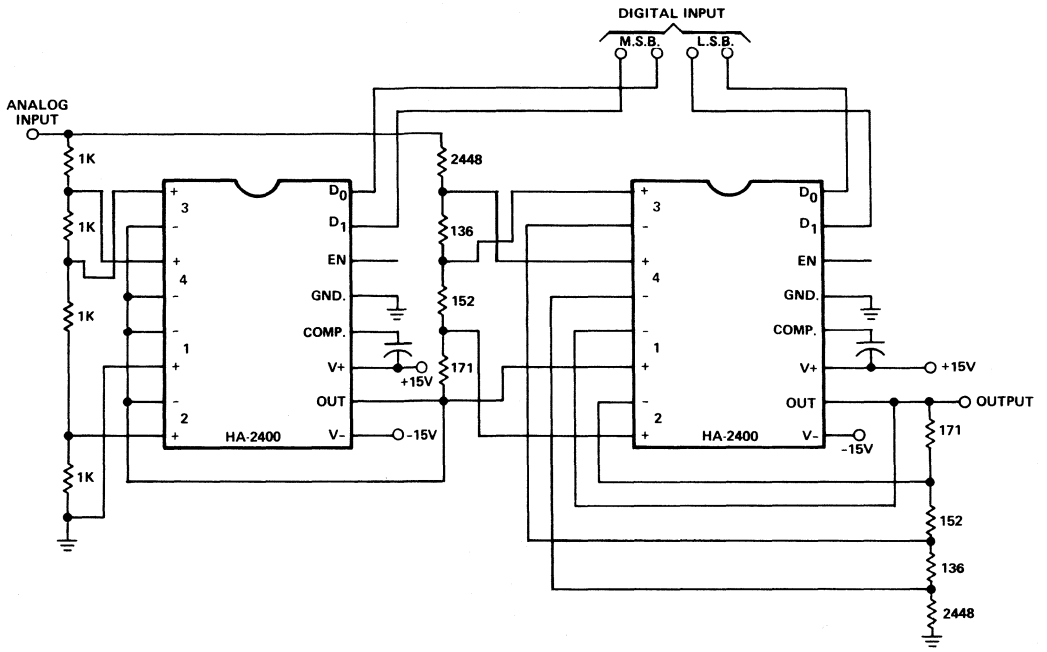
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

APPLICATION NO. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or – sign bit of the digital input.

MORE CHALLENGES

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

FEEDBACK

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

Give your questions and ideas to your local Harris Semiconductor sales engineer, or write to:

Harris Semiconductor
Linear Applications Engineering
P. O. Box 883
Melbourne, Florida 32901

HARRIS SEMICONDUCTOR

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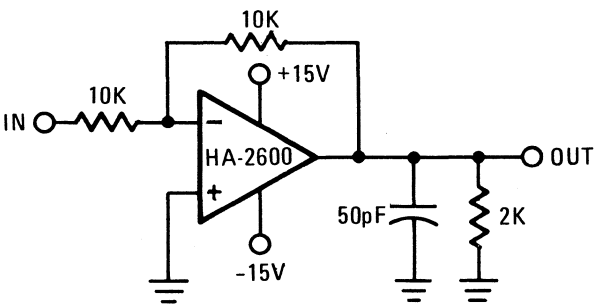
APPLICATION NOTE 515

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

BY DON JONES

This is the first in a series of notes dealing with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



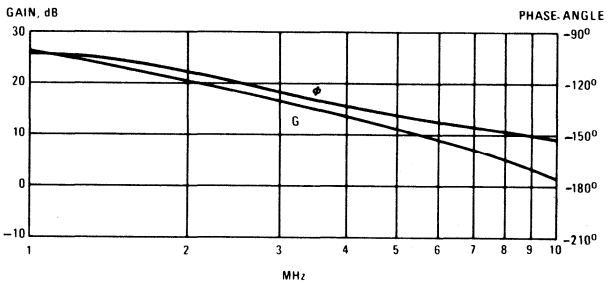
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5 MHz.

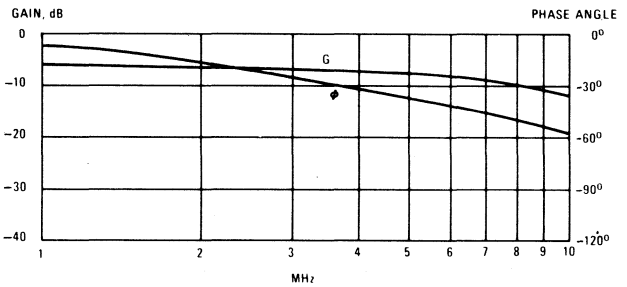
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6 dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3 pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6 pF. With only 5K effective resistance at this point, 5 to 10 pF seems pretty negligible, doesn't it? But let's find out.

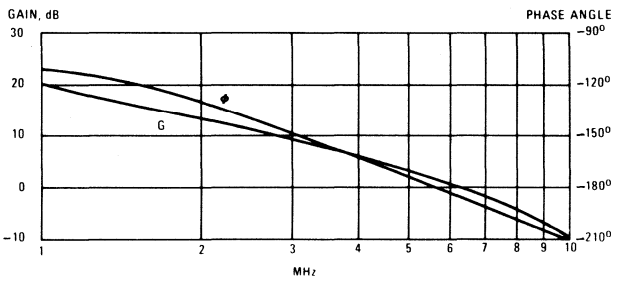
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10 MHz looks like this:



The characteristics of the feedback network alone with 5 pF capacitance to ground looks like this:

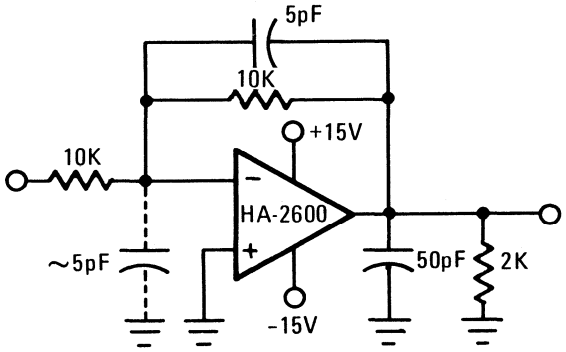


Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



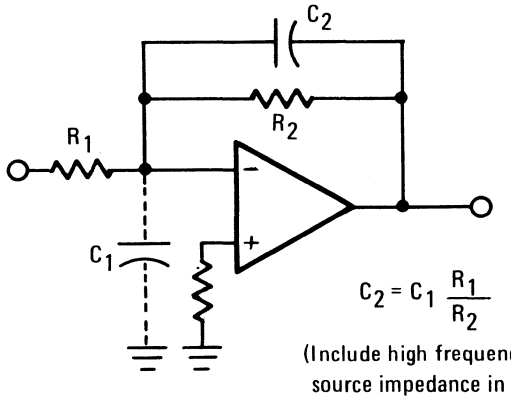
We can see that on the composite response curves, the phase shift crosses 180° at 5.5 MHz, and that there is still about +2 dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:

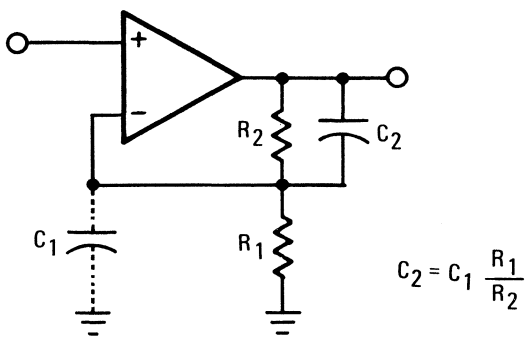


If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6 dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5 MHz and a positive phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

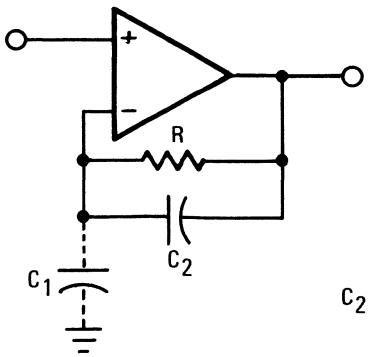
The general scheme for compensation of various circuit types is shown below:



INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 - for most layouts, about 5 to 10 pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2 pF, it isn't necessary to use C_2 - but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output - if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage - if the high frequency peaking is less than +6 dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

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APPLICATION NOTE 601

INTRODUCTION TO THE PHASE LOCKED LOOP

BY DON JONES

INTRODUCTION

In electronics, we are all concerned with the manipulation of information which is expressed as electrical quantities. This information can be expressed many ways - as a voltage, a current, a time period between two events, or as modulation information on an A.C. carrier - amplitude, frequency, or phase angle.

Of these, the time related expressions - time, frequency, and phase angle have several advantages. Information can be transferred between remote points with less loss of accuracy due to noise. Extremely accurate standards are available - crystal oscillators and atomic clocks.

One reason that frequency or phase modulation has not been used more universally as an information medium, is that hardware to manipulate these signals has been more complex than that for voltage and current signals. For voltage and current signals, inexpensive building blocks such as operational amplifiers and digital circuits have greatly simplified design of complex systems. Now, there is a versatile building block for signals in the frequency domain - the monolithic phase locked loop.

You've probably heard the term. "phase locked loop", a number of times since first starting in electronics; but unless you have already had the opportunity to work with one, the concept may not be clear. The general operation of this circuit is really not difficult to understand. You will find the phase locked loop to be a very useful tool wherever A.C. signals are encountered - from subaudio to microwave frequencies.

WHAT IS A LOOP?

First, let's review what is meant by "loop"; then later we can show where "phase lock" comes in.

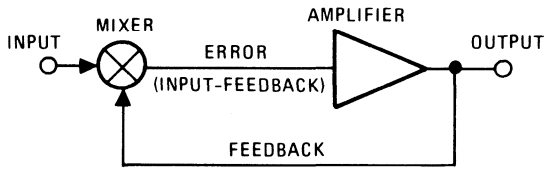


Figure 1

Figure 1 is a general diagram which fits many control systems - electronic, mechanical, or even the human body. The input signal is a function of the desired output. If the output is not presently at the desired point, an error signal is generated by the mixer- which is amplified and drives the output in a direction so as to minimize the error signal. In a moment, we will see how this negative feedback loop system applies to the phase locked loop.

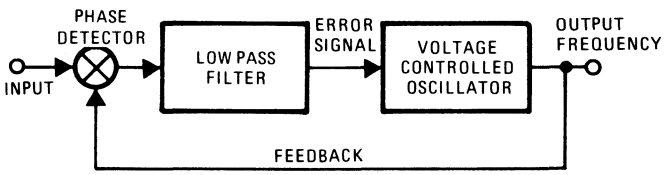


Figure 2

A simple diagram for a phase locked loop is shown in Figure 2. If we consider the phase detector and low pass filter to be a mixer, and the voltage controlled oscillator to be a type of amplifier, the diagram is identical to the negative feedback loop in Figure 1.

In many feedback control systems, the input and output information signals are expressed as voltages. In the phase locked loop, however, the input and output information signals are expressed as A.C. frequencies.

As in the general loop, the output is driven in the direction which will tend to minimize the error signal. In this case, the error signal is a frequency - so the loop tends to drive the error frequency towards zero frequency. To accomplish this, the feedback frequency must be made equal to the input frequency. Once the two frequencies are made equal, the error signal is a function of phase difference between the two signals, so that the phase difference is also controlled.

Before showing what we can do with the phase locked loop, let's examine its parts.

PHASE DETECTOR AND FILTER

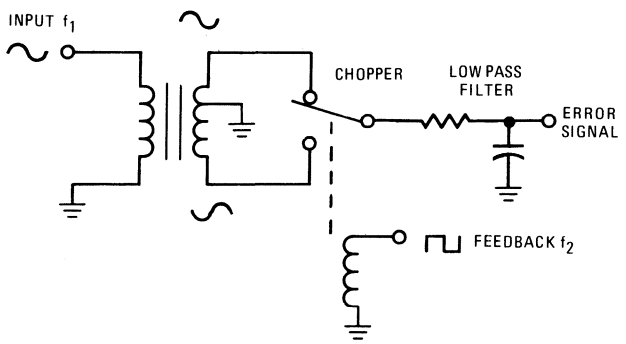


Figure 3

For simplicity, an electromechanical phase detector is illustrated in Figure 3. Of course, most systems use a solid state switching element, rather than a mechanical chopper.

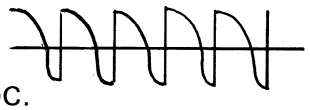
As the chopper armature is moved from one contact to the other, the input signal appears at the armature alternately at 0^o or 180^o phase. If the input and feedback frequencies, f_1 and f_2 are not equal, the circuit acts as a balanced modulator with sum and difference frequencies, $(f_1 + f_2)$ and $(f_1 - f_2)$ appearing at the chopper armature. The low pass filter will pass mainly the difference frequency with increasing amplitude as the two frequencies approach one another.

If the input and feedback frequencies are exactly equal, a D.C. component will appear at the filter output, with amplitude dependent on the phase difference between the two signals. This is illustrated in Figure 4.

a) f_1 & f_2 In Phase:

Chopper Armature:
Filter output is positive D.C.

b) f_1 & f_2 90^o Out of Phase



Chopper Armature:
Fitler output is OVDC.

c) f_1 & f_2 180^o Out of Phase:

Chopper Armature:
Filter output is negative D.C.

Figure 4

Figure 5 shows filter output D.C. voltage as a function of phase difference between f_1 and f_2.

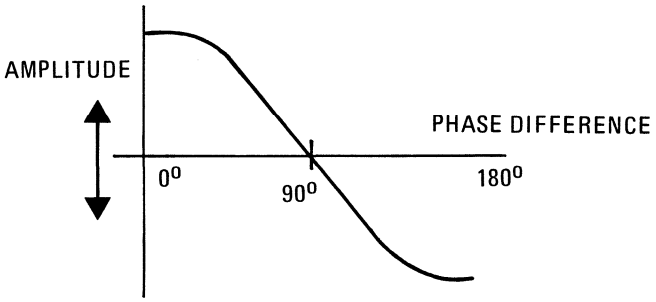


Figure 5

In this example, we can see that the output level is proportional to the input amplitude, as well as phase angle, and that zero output occurs at 90^o phase angle. This is also true of most solid state phase detectors, which actually multyply the two A.C. input signals together.

VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator (V.C.O.) is usually nothing more than a free running multivibrator with a D.C. input which can vary the frequency over a certain range.

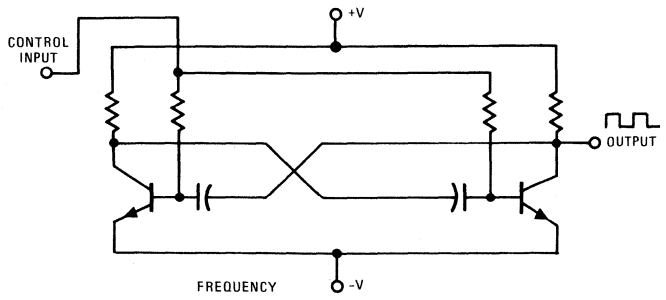


Figure 6

Figure 6 shows a simple V.C.O. If the control input were tied to +V, this would be a conventional fixed frequency multivibrator. As the control input D.C. voltage becomes more positive, the timing capacitors charge more rapidly, and the output frequency increases. Conversely, as the control input becomes less positive, the timing capacitors will charge more slowly and the output frequency will decrease. This relationship is shown in Figure 7.

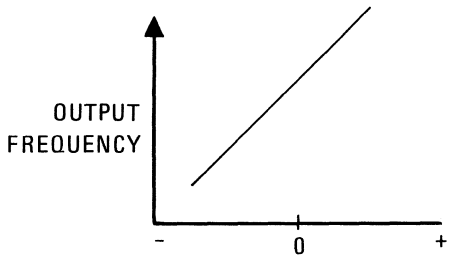


Figure 7

PHASE LOCKED LOOP OPERATION

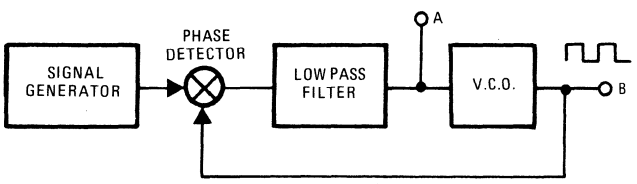


Figure 8

Suppose we connect a signal generator to the P.L.L. as shown above, and watch what happens as we vary the input frequency. First, we have chosen the timing components in the V.C.O. to produce the characteristic shown in Figure 9.

The V.C.O. can be constrained to run between 900 and 1,100 Hz by limiting the voltage swing at point A. Since the detector output characteristic (Figure 5) is bounded at both ends, the oscillator can only function between the limits determined by its input characteristic (Figure 7) and the detector output characteristic.

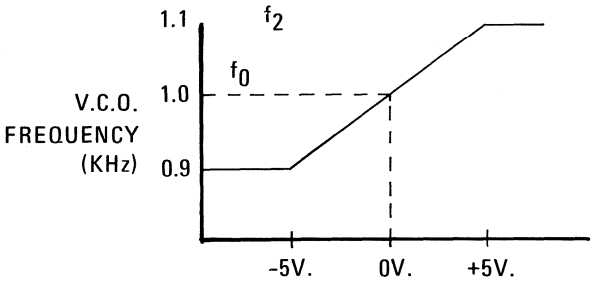


Figure 9

If the signal generator is disconnected, the V.C.O. will run at f_o, 1000 Hz, since the filter output is zero volts. If we then connect the signal generator with its frequency set to 700 Hz, the V.C.O. will still run at f_o, since the difference frequency is high and very little signal gets through the low pass filter.

Now, as we slowly increase the generator frequency, we will observe more and more "jitter" on the V.C.O. output, as the difference frequency becomes lower, and appears larger at the filter output, frequency modulating the V.C.O. about f_o.

Suddenly, say when the generator reaches about 920 Hz - the V.C.O. frequency abruptly jumps and holds steady exactly at the generator frequency. We find that the V.C.O. frequency is "locked" to the generator frequency as long as the generator remains between 900 and 1,100 Hz. If the generator frequency goes outside these limits, the V.C.O. will snap back to f_o. As the generator approaches f_o from either direction, we find that we have to go slightly closer to f_o to initially achieve "lock" than the 900 to 1,100 Hz limits required to hold the signal in "lock". These two sets of limits are known as Capture Range and Lock Range respectively, and can be independently adjusted by changing circuit constants in the PLL.

HOW DOES IT WORK?

Prior to lock, as the generator frequency approached f_o from either direction, the difference frequency from the phase detector becomes smaller and its amplitude passed though the filter becomes larger. This signal modulates the V.C.O. frequency about f_o

until the V.C.O. frequency sweeps past the input frequency - then "lock" takes place.

But why do the two signals "lock"? We can examine the stability of any closed loop system, by imagining what happens if the output takes a small random drift in either direction. Let's assume for the moment that the generato and V.C.O. frequencies are identical. The low pass filter output will be the D.C. level required to maintain the V.C.O. at that frequency in accordance with Figure 9. The phase difference between the V.C.O. and the generator will not necessarily be 90° - it will be whatever phase angle is necessary to produce the proper V.C.O. D.C. input through the phase detector and filter to hold the oscillator frequency identical with the input frequency. Now suppose that the V.C.O. frequency drifts upward from the generator frequency by a fraction of a cycle. The first indication of this is that the phase difference between the two signals will change - the V.C.O. phase will become more leading. If the phase detector is connected such that a leading V.C.O. phase will make its output less positive, then the filter output will tend to pull the V.C.O. back to its original frequency. Conversely, a tendency for the V.C.O. to drift downward will also be corrected. For the same reasons, any change in the generator frequency will be tracked by the V.C.O. frequency. Since the phase detector output level as a function of phase angle is a cosine curve (Figure 5), there will be two points in 360° where the detector output is at the proper level to drive the oscillator to the input frequency - but only one of these points has positive stability, so the loop will automatically settle on the stable side of the curve.

APPLICATIONS

There are several properties of the phase locked loop which make it quite useful in processing signals in the frequency domain.

First we will find that the PLL is able to lock on to low level C.W. signals, even in the presence of random noise of greater amplitude than the signal.

1. The PLL can perform as an amplifier and noise filter.

Also, we know that the PLL will respond only to frequencies in the range of the V.C.O. and phase detector, so:

2. The PLL functions as a band-pass filter.

Referring back to Figure 8, suppose we rock the signal generator frequency back and forth between 900 and 1,100 Hz while observing the filter output at point A with a D.C. voltmeter. We will find that as the generator (and V.C.O.) frequency increases, the voltage will increase by a proportional amount in accordance with Figure 9: since the V.C.O. input voltage must change to track a change in generator frequency. If the generator is frequency modulated by a low frequency sine wave, that sine wave will be reproduced at point A. We can conclude:

3. The PLL will domodulate F.M. signals.

Some of the areas where the PLL may be applied include:

1. F. M. Receivers
   A PLL connected to a receiver I.F. signal with its center frequency at the I.F. frequency will replace one or more I.F. stages and the discriminator stage, eliminating the cost, bulk, and lower reliability of I.F. and discriminator transformers. In broadcast receivers, PLL's can also be used to detect the stereo pilot signal and to demodulate SCA broadcasts. In T.V. receivers, PLL's can be used in the I.F., sound discriminator, synch separator, and color discriminator sections; in each case replacing L-C tuned circuits. With modifications, the PLL can also be used in A.M. or phase modulation discriminators.

2. Data Modems
   In transmitting digital data over telephone lines, the ones and zeros are often encoded as two different audio tone frequencies. This is know as frequency shift keying, or FSK.

   The PLL may be used to decode these tones, since its filter output level will be proportional to the input frequency. Other modem systems utilize phase modulation of a single audio frequency, which can also be detected by a PLL in terms of spikes at the filter output.

3. Data Synchronizers
   In exchanging data between different systems, it is often necessary that the different system clocks be synchronized together. The V.C.O. of a PLL connected to an

incoming data stream will recreate the clock signal of the sending system. This eliminates the need for a separate data channel to send the clock signal.

4. Motor Speed Control
Many electromechanical systems, such as magnetic tape drives, require precise speed control, particularly during start and stop operations. Figure 10 shows the incorporation of a motor control within a phase locked loop.

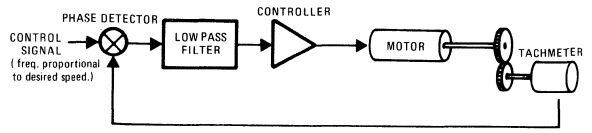


Figure 10

5. Frequency Synthesizers
A frequency synthesizer is a programmable frequency source with high stability, used in test equipment and in transmitters. It is often desirable to derive any of the programmed frequencies from a single stable reference frequency, as illustrated in Figure 11.

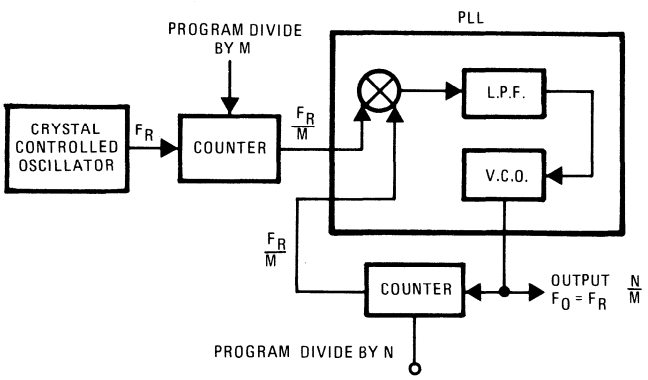


Figure 11

The counters shown may be standard digital integrated circuits which perform a programmed frequency division. The reference frequency, F_R, is first divided by an integer, M, and applied to the PLL input. In order for the loop to be locked, the identical frequency must be present at the other phase detector input. Since another counter (divide by N) is in series with the V.C.O. feedback line, the V.C.O. must be running at N times the PLL input frequency to satisfy conditions for lock. Therefore, the V.C.O. frequency is F_R times the ratio, $\frac{M}{N}$. Therefore, by programming M and N, we can produce any of a large number of frequencies, each with the stability of the single reference frequency.

HA-2800/HA-2820 PLL

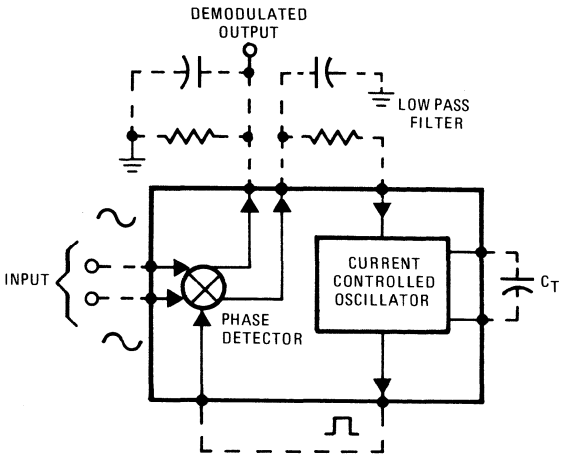


Figure 12

Harris Semiconductor has developed two monolithic PLL integrated circuits with a number of improvements over other similar circuits. The HA-2800 operates at frequencies from 1kHz to 25MHz, while the HA-2820 is designed for frequencies from 0.01Hz to 3MHz.

Functions common to both devices are shown in Figure 12. Significant features include:

1. No Internal Connections Between Detector and Oscillator

   This greatly enhances the device versatility. The low pass filter can be a critical element in some applications. With the loop broken at this point, complex passive or active filters may be inserted, several filters of different characteristics may be switched into the loop to aid in signal acquisition and tracking, or sweep circuits may be switched into the oscillator to scan a frequency band and acquire a signal.

   Also, with the loop broken, amplifiers may be inserted in the loop to control loop gain. This technique will be discussed in a later section.

2. Two Isolated Phase Detector Outputs
   For F.M. demodulation, the demodulated output is generally the filtered error signal

from the phase detector. However, a separate output from the phase detector has several advantages. The demodulated output gain can then be adjusted independent of the loop gain, and different filter characteristics may be chosen for the loop filter and the demodulated output filter. Separate filters are necessary to demodulate phase modulated signals - a low frequency cutoff filter in the loop so that the oscillator phase is constant and is determined by the average input phase; and a higher cutoff filter at the demodulated output to distinguish phase shifts between the input signal and oscillator.

3. Current Controlled Oscillator
   Operation of these devices is identical with those described previously containing a voltage controlled oscillator, except that error signal from the phase detector is a current, rather than a voltage. The phase detector outputs are high impedance current sources, so that the demodulated output voltage swing may be adjusted by selection of a load resistor. The oscillator input is a low impedance current sink with a fixed negative input voltage level. The impedance levels allow construction of accurate, temperature stable filters, since filter characteristics will be relatively independent of the device internal impedance characteristics.

LOOP GAIN ADJUSTMENT

In certain applications it may be desirable to increase loop gain by the addition of an amplifier in the error signal path. This has the effect of:

1. Increasing tracking range. The tracking range will then be limited only by the oscillator input range, rather than by the detector output range. Tracking ranges of greater than 3:1 are practical.

2. Tighter characteristics for small input frequency ranges. With an amplified error signal, the phase relationship between the input signal and oscillator output will stay closer to 90° over a given frequency range. The demodulated output swing will be smaller, but more linear.

A simple connection for insertion of an operational amplifier is shown in Figure 13.

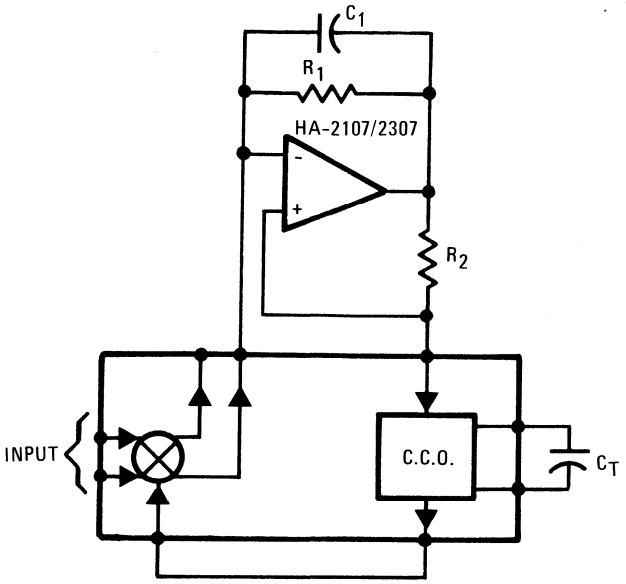


Figure 13

The current gain of the circuit is:

$$-\frac{R_1}{R_2}$$

The inversion of the error signal does not affect loop stability, since the phase detector characteristic is symmetrical about 0° and lock will occur at -90° rather than +90°. The low pass filter is formed by R_1 and C_1. The connection of the amplifier (+) input to the C.C.O. input sets the amplifier output voltage swing about the C.C.O. input voltage - very little signal feedback to the (+) input occurs because of the low impedance of the C.C.O. input.

TRACKING RANGE LIMITER

This circuit is internal to the HA-2800/2805 and may be added externally to the HA-2820/2825.

Tracking range in a PLL is normally limited by the output signal range of the phase detector. In some applications, such as where response to a limited frequency band is desired, tighter control of the tracking range is necessary. This can be accomplished by limiting the excursions of the error signal.

The circuit in Figure 14 shows one method of limiting tracking range. The operational amplifier simply produces an isolated output voltage equal to the oscillator input voltage.

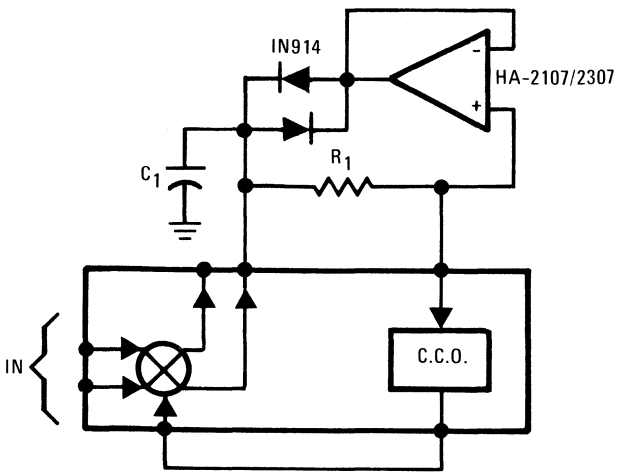


Figure 14

The voltage swing at the amplifier output is limited to approximately ±0.7 volts about the C.C.O. input voltage by the forward diode characteristics. Therefore, the oscillator input current is limited to approximately $\pm\frac{0.7}{R_1}$, and the tracking range may be calculated from the published oscillator conversion gain. The amplifier and diodes are built in to the HA-2800/.2805.

GLOSSARY OF PLL TERMS

Acquisition Range(Capture Range): The range of input frequency about f_O under which a PLL, which is initially unlocked, will become locked. This range is narrower than the normal tracking range, and is a function of the loop filter characteristics and the input amplitude.

Conversion Gain: The ratio of output change to input change in a portion of the loop. In the phase detector, this is the ratio of output signal change, to a change in phase angle between the two inputs (volts/radian or μA/radian). Since the phase detector characteristic is generally a cosine curve, the gain is measured for small excursions about the 90° point. In the oscillator this is the ratio of output frequency change to an input change (% Δf/volt or % Δf/μA).

Current Controlled Oscillator (C.C.O.): A circuit which creates an A.C. output signal whose frequency is a function of the D.C. input current.

f_O: The free running frequency of the oscillator under a zero input signal condition.

Loop Gain: The product of the conversion gains of the loop elements (% Δf/radian), which is the ratio of change in input (and oscillator) frequency to the change in phase shift between input and oscillator. Therefore, loops with higher gains will hold the phase relationship closer to 90° for a given input frequency change, and conversely will have a broader tracking range.

Phase Detector (Phase Comparator): A circuit which creates an output level which is a function of the phase angle between two A.C. input signals. Most phase detectors are also amplitude sensitive.

Tracking Range (Lock-In Range): The range of input frequency about f_O under which a PLL, once locked, will remain locked. This is a function of loop gain, since the phase detector output is bounded and can drive the oscillator only over a certain frequency range. The tracking range may be controlled, if desired, by limiting the input signal to the oscillator.

Voltage Controlled Oscillator (V.C.O.): A circuit which creates an A.C. output signal whose frequency is a function of the D.C. input voltage.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 602

A GENERAL ANALYSIS OF THE PHASE LOCKED LOOP

BY J.A. CONNELLY

INTRODUCTION

The concept of phase locked loops (PLL) was first proposed over forty years ago by de Bellescize in 1932.[1] De Bellescize investigated the subject of synchronous reception of radio signals where a receiver consisting of only a local oscillator, a mixer, and an audio amplifier was employed. The oscillator was adjusted to exactly the same frequency as the carrier frequency. With no frequency modulation of the carrier, an intermediate frequency of zero hertz was created. However, when the carrier was frequency modulated, the output from the mixer represented the desired demodulated information carried by the signal.

The principal shortcoming of the receiver system as proposed by de Bellescize was the practical limitation of achieving perfect synchronization between the carrier frequency and the frequency of the local oscillator. Any frequency mismatch hopelessly garbled the information. To achieve the desired operation, the local oscillator and transmitted signal had to be frequency and phase locked together with a degree of synchronization which was impractical at that time. Thus, the more complicated but more practical technique of the superhetrodyne receiver became the accepted approach for demodulation.

Subsequent to these early investigation by de Bellescize, numerous systems employing phase locked loops have been designed which overcame the practical constraints that plagued previous attempts. A few examples where successful phase locked loop operation has been achieved include the synchronization of horizontal and vertical scanning signals in television receivers, removal of the Doppler frequency shift in satellite tracking, stabilization of the frequency of klystron oscillators, and noise filtering in many communication systems. Virtually all of these applications of PLLs employ a variety of sophisticated circuit techniques utilizing complex, inductively tuned filters to achieve the required frequency stability. Other potential application areas of PLLs exist where the employment of this technique using discrete components remained either too complex or too expensive to be justifiable until the advent of the integrated circuit PLL.

The recent development of the integrated circuit phase locked loop (PLL) has enabled many of the practical limitations to be overcome which prevented utilization of most of the simpler and more direct instrumentation techniques.

Synchronous detection without tuned circuits is now feasible and economically advantageous. Also, PLLs can now be employed economically in a variety of related applications such as frequency multiplication and division, frequency synthesizers, tracking filters, motor speed monitoring and controls, modems, tone decoders, and FSK receivers. The purpose of this application note is to present the fundamental concepts involved with phase locked loops and to describe the operation of a typical PLL system.

PRINCIPLES OF PHASE LOCKED LOOPS

The function of a phase locked loop system is to detect and track small differences in phase and frequency existing between an incoming signal and a secondary reference signal. As shown in Figure 1, the PLL is basically an electronic servo loop consisting of a phase detector (PD), a low pass filter (LPF), and a controlled oscillator whose frequency is a linear function of either a dc voltage or current. In the following discussion, current control will be assumed to produce a current controlled oscillator (CCO).

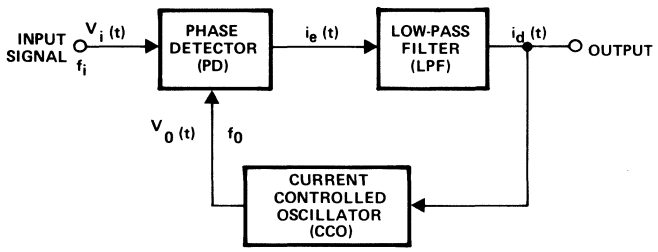


Figure 1

As the loop tracks the input signal, the PD compares the frequency of the input signal with the output from the CCO. A change in the phase of the input signal indicates that the incoming frequency is beginning to change. This change is detected by the PD, which produces and output directly proportional to the sum and difference in frequency and/or phase between the input signal and the signal from the CCO. The high frequency (sum) component of the phase detector's output is removed by the low pass filter, leaving a low frequency current signal. The output current from the LPF is an error signal whose magnitude is directly proportional to the phase difference between the two signals applied to the phase detector. This error signal is then used to adjust the frequency, and, consequently, the phase of the current controlled oscillator in such a direction as to establish phase synchronization between the two signals applied to the phase detector.

The closure of the loop and the establishment of phase lock between the PD inputs produces a configuration with negative feedback typical of those encountered in classical control systems. As such, many of the analytical techniques developed for determination of system stability, frequency response, tracking, and system optimization are directly applicable to phase locked loops. Since it is beyond the scope of the treatment intended here, the more interested reader is referred to several sources where developments of these techniques may be found.[2-4] It is hoped that the discussion which follows covering the operation of the phase detector, low pass filter, and current controlled oscillator will provide the necessary background for applying the control system techniques in the design of a particular phase locked system.

A LINEAR MODEL FOR A PLL SYSTEM

Whenever a phase lock is established between v_i (t) and v_o (t), the linear model of Figure 2 can be used to predict the performance of the PLL system. ϕ_i and ϕ_o represent the phase angles associated with the input and CCO respectively. F (s) represents a generalized current transfer function of the low pass filter in the frequency domain. K_d and K_o are the conversion gains of the phase detector and current controlled oscillator, each having units as shown.

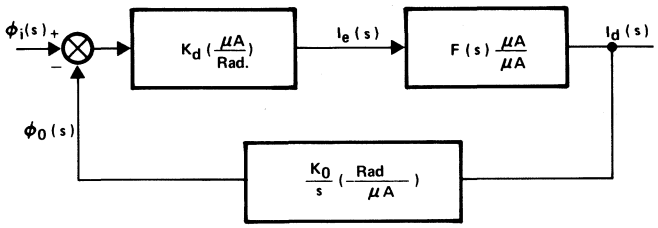


Figure 2

The representation of the phase detector as a summing network for combining ϕ_i (s) and ϕ_o (s) can be explained as follows. The phase detector is an analog multiplier which forms the product of an RF input signal v_i (t) and the output signal, v_o (t), from the current controlled oscillator. Assume that these two signals can be described by:

$$v_i(t) = V_i \sin w_i t \quad \text{and}$$

$$v_o(t) = V_o \sin (w_o t + \phi) \quad \text{where}$$

w_i, w_o, and ϕ are the frequency and phase characteristics of interest. The product of these two signals is an output current signal given by:

$$i_e(t) = K_1 V_i V_o (\sin w_i t)\,[\sin (w_o t + \phi)]$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of i_e (t) is directly proportional to the amplitude of the input signal V_i.

The two cases of $w_i \neq w_o$ and $w_i = w_o$ are of interest and will now be considered separately.

Case I: $w_i \neq w_o$
When the two input frequencies to the phase detector are not synchronized, the loop is not locked. Furthermore, the phase angle ϕ is meaningless for this case since it can be eliminated by appropriately choosing the time origin. The phase detector's output current signal is given by:

$$i_e(t) = \frac{V_i V_o K_1}{2} [\cos (w_i - w_o)t - \cos(w_i + w_o)t]$$

When i_e (t) is passed through the low pass filter, F(s), the summed frequencies are attenuated, leaving:

$$i_d (t) = V_i V_o K \cos (w_i - w_o)t \quad \text{where}$$

K is a constant. This equation represents the signal current which is supplied to the CCO to control its output frequency. The equation shows that this signal sets up a beat frequency between w_i and w_o, causing the CCO's frequency to deviate by $\pm \Delta w$ from w_o in proportion to the signal amplitude ($V_i V_o K$) passing through the filter. If the amplitude of V_i is sufficiently large, and signal limiting or saturation does not occur, the CCO's output frequency will be shifted from the free running frequency, w_o', by some Δw until lock is established where $w_i = w_o = w_o' \pm \Delta w$. If lock cannot be established, then either (1) the input signal amplitude is too small to drive the CCO to produce the necessary $\pm \Delta w$ deviation, or (2) w_i is beyond the dynamic range of the CCO, i.e. $w_i \lesssim w_o' \pm \Delta w$. Obvious remedies for these "no lock conditions" are:

1. Increase the input signal's amplitude. This can be done either internally or externally to the loop by employing additional amplification.

2. Increase the internal loop gain by adjusting upward (larger - 3dB frequency) the response of the low pass filter.

3. Shift the free running frequency, w_o', of the CCO closer to the expected w_i frequency. Establishing frequency lock for the loop leads to the second case, namely phase lock where $w_i = w_o$.

Case II: $w_i = w_o$
When w_i and w_o are frequency synchronized, the output signal from the phase detector for $w_i = w_o = w$ and phase shift ϕ is:

$$i_e (t) = K_1 V_i V_o (\sin wt)(\sin wt + \phi)$$

$$= \frac{K_1 V_i V_o}{2} [\cos \phi - \cos (2wt + \phi)]$$

The low pass filter removes the high-frequency, ac part of $i_e(t)$ while leaving the dc component as a current signal for the CCO. Thus:

$$i_d (t) = I_d = \frac{K_2 V_i V_o}{2} \cos \phi$$

where K_2 is a dimensional constant.

Suppose w_i and w_o are perfectly synchronized to the free-running frequency w_o'. For this case I_d will be zero indicating that the ϕ must be 90°. Thus the error signal, I_d, is proportional to a phase difference between w_i and w_o centered about a reference phase angle of 90°. If w_i now changes from w_o', I_d will adjust and settle out to some non-zero value in order to correct w_o so that frequency lock is maintained with $w_i = w_o$. ϕ will be shifted by some amount, $\Delta \phi$, from the reference phase angle of 90°. This concept can be simplified by redefining ϕ as:

$$\phi = \phi_o \pm \Delta \phi \quad \text{where}$$

ϕ_o is the inherent 90° phase shift and $\Delta\phi$ represents departures from this reference value. Now the I_d becomes:

$$I_d = V_i V_o K_2 \cos(\phi_o \pm \Delta \phi) = \pm V_i V_o K_2 \sin \Delta\phi$$

Since the sine function is odd, a momentary change in $\Delta\phi$ contains information as to which way to adjust the CCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta \phi$ changes can be tracked is from -90° to +90°. This corresponds to a ϕ range from 0 to 180°.

In addition to being an error signal, I_d represents the demodulated output of an FM input applied as v_i (t) assuming a linear CCO characteristic. Thus, FM demodulation can be accomplished with the PLL without the inductively tuned circuits employed using conventional detectors.

The useful frequency range over which the PLL can track an input signal is called the Lock Range or alternatively, the Tracking Range. The lock range is determined primarily by the maximum frequency swing possible in the CCO and the maximum output current from the phase detector for the input signal level.

When the frequency of the input signal deviates from the reference frequency w_o', of the CCO by more than the tracking range, the loop becomes unlocked and the linear model of Figure 2 no longer describes the system. When this happens, the CCO runs at w_o' and the output current, I_d becomes zero.

Phase lock is reestablished when the input frequency approaches w_o'. The frequency range over which the PLL can acquire an input signal is denoted as the Capture Range which is set by the low pass filter's characteristics. The capture range is limited to a value less than the lock range.

For normal, phase lock operation, the frequency of the reference signal input, w_o', is first set under zero input signal conditions to establish the free-running frequency of the loop. A particular w_o' is normally positioned in the center of the frequency band of interest so that both positive and negative deviations of the input signal frequency about w_o' can be detected by the PLL. Next, the particular LPF configuration necessary from design considerations is determined for the system. The factors to be considered are the necessary capture range for the $\pm \Delta w$ modulations expected, high attenuation of the 2 w_i component from the phase detector, and the desired loop response to rapid changes in input frequency.

STABILITY CONSIDERATIONS OF PLL

Unexpected oscillations are always a possibility whenever feedback is employed to close a loop containing active elements. The stability, as well as the operation of the PLL of Figure 2, principally depends upon the characteristics of the low pass filter. A stability analysis using root locus techniques is given for several typical low pass filters. The purpose of the low pass filter is to surpress the summed frequencies ($w_i + w_o = 2w$) from the multiplier while preserving the dc signal represented by i_d. The selectivity, i.e. tracking and capture ranges, as well as the time response to changes in input frequency or phase angle, depend upon the frequency characteristics of this low pass filter. Any linear low pass filter will have the generalized response given by:

$$F(s) = \frac{\sum_{i=o}^{m} a_i s^i}{\sum_{j=o}^{n} b_j s^j} \qquad \text{where } m \leq n$$

In typical filter applications, one particular pole will dominate in the F(s) expression, i.e. the lowest of the high frequency poles. As the location of this pole is moved closer to the zero frequency origin, the frequency selectivity of the PLL to the $w_i - w_o$ difference increases. This increase in frequency selectivity naturally reduces both the tracking and capture ranges.

When the PLL is tracking an input signal, the loop gain of Figure 2 is given by:

$$G(s)\,H(s) = \frac{K_d K_o F(s)}{s}$$

The simplest low pass filter is the RC network shown in Figure 3 which has a current transfer function given by:

$$F(s) = \frac{I_2(s)}{I_1(s)} = \frac{1}{1+\tau_f s} \qquad \text{where } \tau_f = RC$$

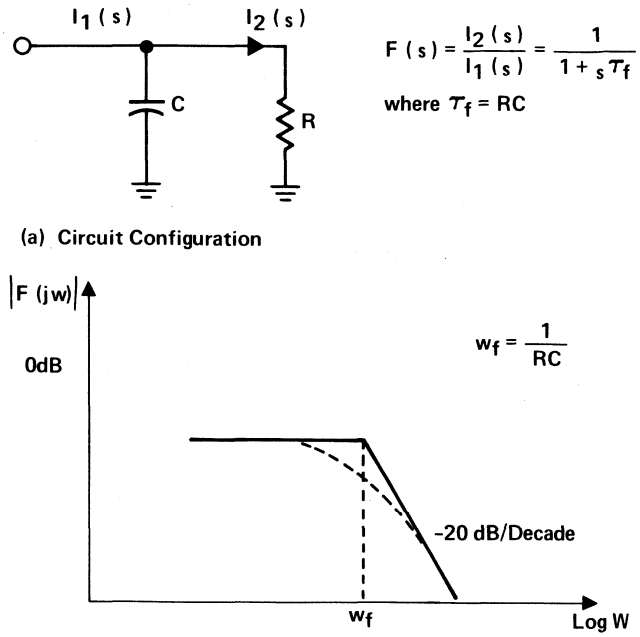


Figure 3

With this filter, the loop gain is:

$$G(s)\,H(s) = \frac{K_d K_o}{s\,(1+\tau_f s)} = \frac{K}{s\,(1+\tau_f s)} \quad \text{where}$$

$$K = K_d K_o$$

The root locus for the PLL with the simple RC filter is shown in Figure 4. This locus shows the behavior of the PLL when the loop is closed for all positive values of gain K. The locus begins on the poles, corresponding to K = 0 and preceeds along the real axis until the critical value of gain is reached. For $K = K_{crit}$, the closed loop response has the form:

$$\frac{I_d(s)}{\phi_i(s)} = \frac{K_{crit}}{s^2 + \frac{s}{\tau_f} + \frac{K_{crit}}{\tau_f}} = \frac{K_{crit}}{(s + \frac{1}{\tau_{crit}})^2}$$

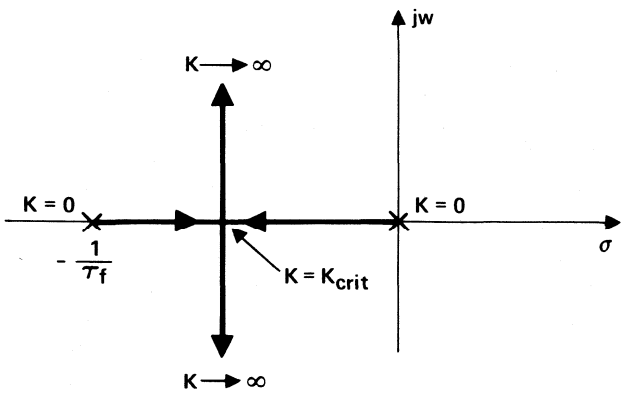


Figure 4

This equation shows that the system is critically clamped for this gain. When $K > K_{crit}$, the system will exhibit a damped sinusoidal response to an input phase angle step function. Since the root locus always lies in the left-half of the complex plane, the system is unconditionally stable for all K values.

In most phase lock loop systems, the conversion gains K_o and K_d are functions of parameters internal to the integrated circuit, and therefore not easily adjustable to achieve the desired system response. To overcome this shortcoming, an amplifier whose gain, A, is easily adjusted, can be inserted in the loop. When a typical amplifier with a single high frequency pole is employed, the loop gain becomes:

$$G(s)H(s) = \frac{K_o K_d A}{s(1+s\tau_f)(1+s\tau_a)} = \frac{K_1}{s(1+s\tau_f)(1+s\tau_a)}$$

where A and τ_a represent the amplifier's characteristics. The root locus describing this loop gain is shown in Figure 5. In constructing this plot, the pole due to the amplifier was arbitrarily made larger than the filter's pole. However, the general shape of the root locus is independent of the relative positions of these two poles. This locus illustrates that the system will become unstable for all values of gain K_1 greater than K_{crit}. However, stable operation can be achieved by limiting the maximum gain of the amplifier (as well as $K_o K_d$) to a value less than that which produces K_{crit}.

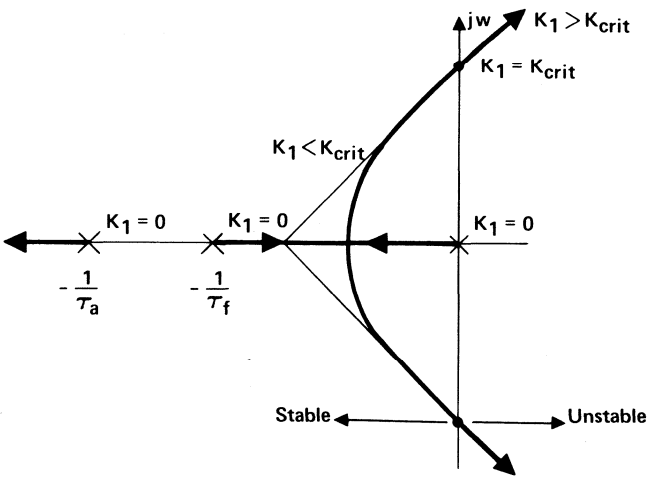
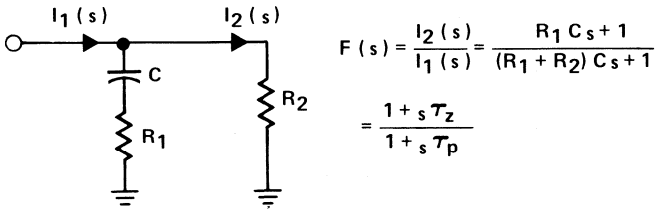


Figure 5

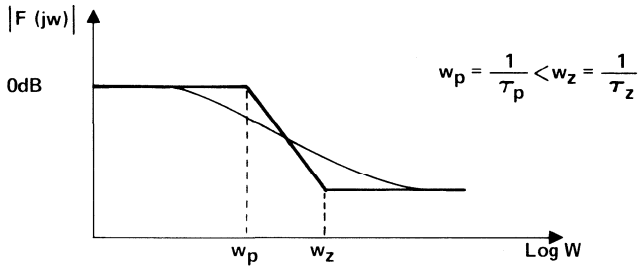
Stable PLL operation with adjustable gain can be achieved by utilizing a filter having both a pole and a zero such as that shown in Figure 6. When this filter and the previous amplifier are employed, the loop gain becomes:

$$G(s)H(s) = \frac{K_o K_d A\,(1 + s\tau_z)}{s(1 + s\tau_p)(1 + s\tau_a)}$$



$$F(s) = \frac{I_2(s)}{I_1(s)} = \frac{R_1 C s + 1}{(R_1 + R_2) C s + 1} = \frac{1 + s\tau_z}{1 + s\tau_p}$$

(a) Circuit Configuration

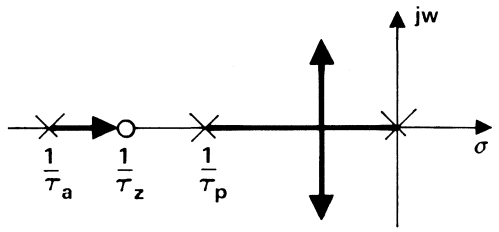


$$w_p = \frac{1}{\tau_p} < w_z = \frac{1}{\tau_z}$$

(b) Frequency Response

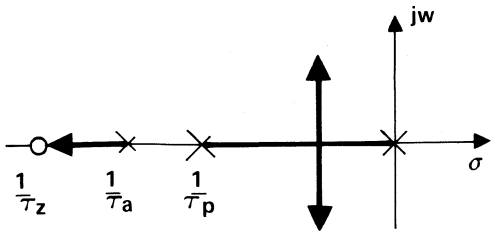
Figure 6

A number of different root loci are possible for this loop gain expression depending upon the relative locations of τ_z, τ_n, and τ_a. Figure 7 illustrates all possibilities and shows the loop is now stable for all values of gain. Introduction of the zero has the effect of pulling the root locus to the left away from the right-half plane where instability would result. The case shown in part (e) of Figure 7 is of particular interest, since it shows pole-zero cancellation between the amplifier and the low pass filter, resulting in the same root locus as previously given in Figure 3.



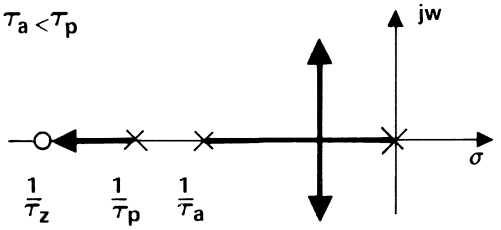
$\tau_a < \tau_z < \tau_p$

(a) Zero located between poles



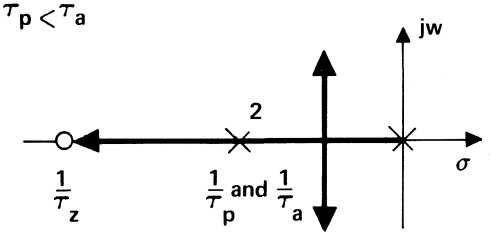
$\tau_z < \tau_a < \tau_p$

(b) Zero to the left of both poles with $\tau_a < \tau_p$



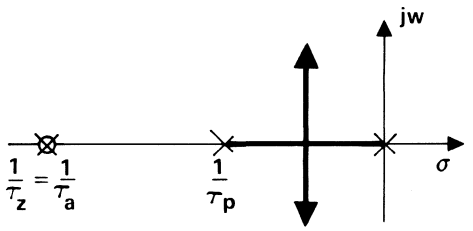
$\tau_z < \tau_p < \tau_a$

(c) Zero to the left of both poles with $\tau_p < \tau_a$



$\tau_z < \tau_p = \tau_a$

(d) Equal poles



$\tau_z = \tau_a < \tau_p$

(e) Poles - Zero cancelation

Figure 7

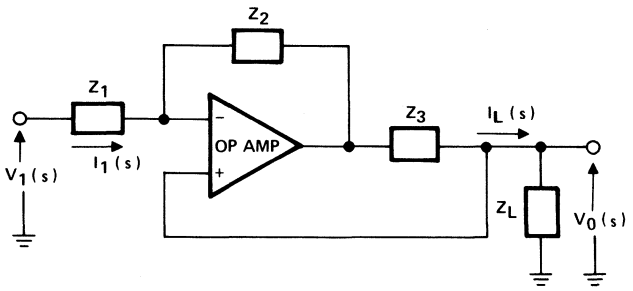
Many other filter configurations for PLL operation could be examined if space permitted. However, the utilization of active filters with PLL presents many especially interesting possibilities, one example of which follows. Figure 8 shows a typical, generalized circuit configuration for an active filter, which has the voltage and current transfer responses indicated. These transfer responses were obtained assuming an ideal operational amplifier ($A_V \rightarrow \infty$, $Z_{in} \rightarrow \infty\ \Omega$, $Z_{out} \rightarrow 0\ \Omega$).

The current transfer function is particularly significant since it indicates that the output current is not a function of the load impedance Z_1. Thus, in addition to being an active filter, this network can be made to supply a constant current to a varying load impedance.

As a special example of the active filter of Figure 8, assume that impedances are chosen according as:

$$Z_1 = 0 \quad Z_2 = R_2 + \frac{1}{sC_2}$$

$$Z_3 = R_3 \qquad Z_1 = R_1$$



$$\frac{V_0(s)}{V_1(s)} = \frac{Z_L Z_2}{Z_L Z_2 - Z_1 Z_3}$$ Forward Voltage Transfer Function

$$\frac{I_L(s)}{I_1(s)} = -\frac{Z_2}{Z_3}$$ Forward Current Transfer Function

Figure 8

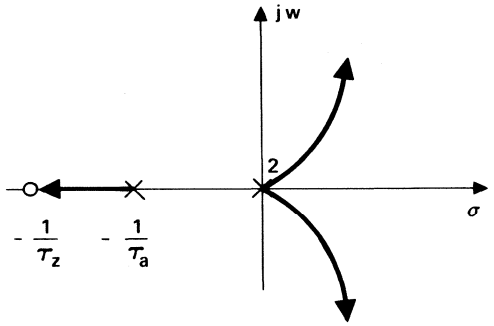
Chosen thusly, the response of the active filter is given by:

$$F(s) = \frac{I_L(s)}{I_1(s)} = -\frac{1}{R_3C_2}\left[\frac{1+s\tau_Z}{s}\right] = K_f\left[\frac{1+s\tau_Z}{s}\right]$$

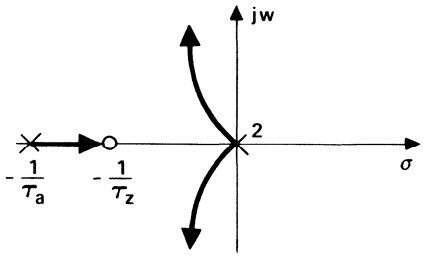
where $\tau_Z = R_2C_2$. For very small τ_Z, the low pass filter is essentially an integrator. When this filter is employed in the PLL, the loop gain becomes:

$$G(s)H(s) = \frac{K_0K_dK_fA(1+s\tau_Z)}{s^2(1+s\tau_a)} = \frac{K_2(1+s\tau_Z)}{s^2(1+s\tau_a)}$$

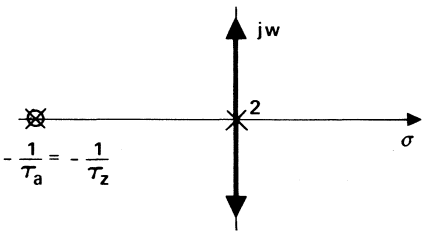
Three root loci are possible depending upon the relative locations of τ_Z to τ_a, as shown in Figure 9. As can be seen, stability is only guaranteed for part (b) where the zero of the filter lies between the poles. Part (c) where the locus coincides with the imaginary axis is considered "marginally stable". However, it is not useful practically.



(a) Zero to the left of amplifier's pole



(b) Pole to the left of active filter zero



(c) Pole-zero cancellation

Figure 9

STEADY-STATE RESPONSE OF PLL

The steady-state response of a phase locked loop system to stimulation afforded by various types of input signals is of equal importance to the system's stability. Frequently, while the employment of a certain low pass filter may guarantee stability, it may produce a system with unsatisfactory steady-state characteristics for the types of input signals expected. The development which follows will be useful for determining the particular type of low pass filter needed to enable the system to respond to step function, ramp and acceleration inputs.

With reference again to the linear model of the PLL system shown in Figure 2, the current signal $I_e(s)$ represents the phase error that exists between the incoming reference signal $\phi_i(s)$ and the feedback signal $\phi_o(s)$. The final value theorem associated with Laplace transformations, namely:

$$\lim_{t \to \infty} [I_e(t)] = \lim_{s \to 0} [s\, I_e(s)]$$

will be used to find the steady state error without transforming back to the time domain. The phase error signal is given by:

$$I_e(s) = \frac{K_d s}{s + K_d K_o F(s)} \phi_i(s)$$

For unit step function input,

$$\phi_i(s) = \frac{1}{s}$$

For a unit ramp input,

$$\phi_i(s) = \frac{1}{s^2}$$

For a unit acceleration input.

$$\phi_i(s) = \frac{1}{s^3}$$

The steady state responses of the error signal for these three inputs are:

STEP: $\lim_{t \to \infty} [I_e(t)] = \lim_{s \to 0} \frac{K_d s}{s + K_d K_o F(s)}$

RAMP: $\lim_{t \to \infty} [I_e(t)] = \lim_{s \to 0} \left[\frac{K_d}{s + K_d K_o F(s)} \right]$

ACCELERATION:

$$\lim_{t \to \infty} [I_e(t)] = \lim_{s \to 0} \left\{ \frac{K_d}{s[s + K_d K_o F(s)]} \right\}$$

As long as the filter is truly low pass, namely having a general response given by:

$$F(s) = \frac{\sum_{i=0}^{m} a_i s^i}{\sum_{j=0}^{n} b_j s^j} \qquad \text{where } m \leq n$$

the following simplifications are possible:

STEP: $\lim_{t \to \infty} [I_e(t)] = 0$ for any $F(s)$

RAMP: $\lim_{t \to \infty} [I_e(t)] = \frac{1}{K_o} \lim_{s \to 0} \frac{1}{F(s)}$

ACCELERATION:

$$\lim_{t \to \infty} [I_e(t)] = \frac{1}{K_o} \lim_{s \to 0} \frac{1}{s F(s)}$$

Thus the PLL will track a step input with zero steady state error regardless of the low pass filter. In order to achieve zero steady state error for an acceleration input, the low pass filter must have at least two poles positioned at the origin (type 2 filter). Table I shows the expected steady state error for the different inputs when type 1, type 2, and type 3 low pass filters are employed.

INPUT	TYPE 0	TYPE 1	TYPE 2
STEP	ZERO	ZERO	ZERO
RAMP	CONSTANT	ZERO	ZERO
ACCELERATION	CONTINUALLY INCREASING	CONSTANT	ZERO

TABLE 1
STEADY-STATE ERRORS OF VARIOUS FILTER TYPES FOR THREE DIFFERENT INPUTS

CONCLUSIONS

This application note describes the basic theory of Phase Locked Loop operation and develops a linear model for predicting the performance of a typical system. The effects of several typical low pass filters upon system stability and response are described using root locus and steady state error analysis techneques.

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3. D'Azzo, J. J. and C. H. Houpis, Feedback Control System Analysis and Synthesis, McGraw - Hill, New York, 1966
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HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 603

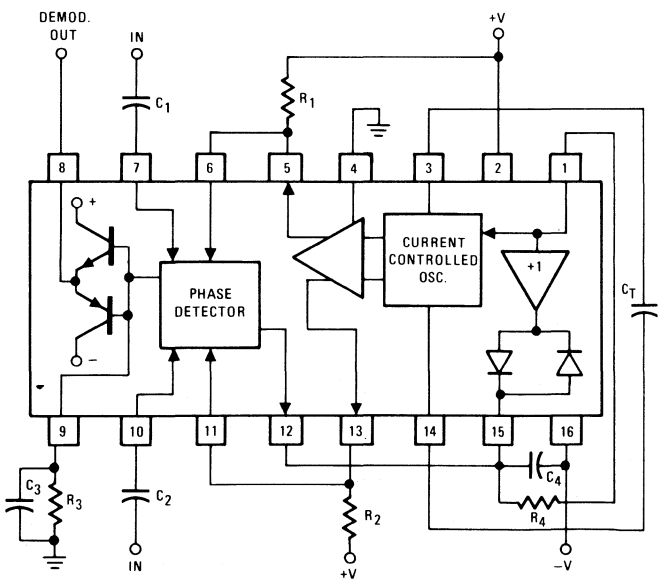
OF THE HA-2800/2805 HIGH FREQUENCY PHASE LOCKED LOOPS

BY J.A. CONNELLY

APP. NOTES

INTRODUCTION

The HA-2800/2805 are monolithic integrated circuits capable of phase locked loop (PLL) operation over an extremely broad band of high frequencies from 1kHz to 25MHz. In actuality, these integrated circuits function as a total system containing a dual-input phase detector with two buffered outputs, a current-controlled oscillator, a drive amplifier with dual outputs, a limiting network, and a complementary NPN-PNP pair of transistors. A block diagram of the HA-2800/2805 illustrating these functions as well as the pin out locations is shown in Figure 1.



HA-2800
High Frequency PLL

Figure 1

Block Diagram Representation of the Functions Contained in the HA-2800/2805 PLL System

BASIC PLL OPERATION

Fundamental PLL operation can be understood by considering the system shown in Figure 2. The phase detector (PD) compares the phase of a sinusoidal input signal with the output from the current-controlled oscillator (CCO) and produces an error current signal proportional to the phase difference between the two signals. After being filtered, the error signal is applied as a control current to the CCO to change its frequency in the direction that reduces the phase difference between the signals applied to the phase detector. Thus a corrective loop is formed using negative feedback. The loop becomes "locked" when the frequency of the input signal is sufficiently close to the free-running frequency of the CCO. When lock occurs, the CCO frequency tracks the signal frequency over small frequency deviations, thus forming a signal tracking filter. If the input signal is frequency modulated, the control current for the CCO is the demodulated output. The PLL operates as an effective noise filter at selected frequencies when the output is taken from the CCO since this output tracks the input frequency at a higher power level with a much improved signal-to-noise ratio.

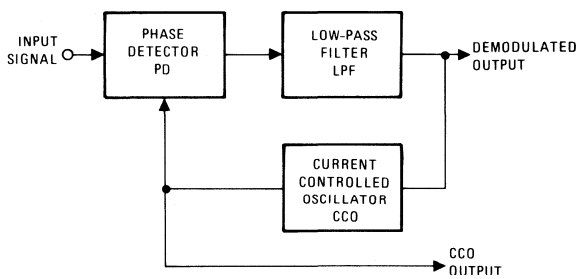


Figure 2

Basic PLL Block Diagram

Potential applications for PLL's are limited only by the designer's imagination. A few of the more general applications where PLL's have already been employed include:

1. FM IF-strip and demodulator for commerical FM receivers
2. Data modems
3. Data synchronizers
4. Motor speed controllers
5. FM modulators
6. Frequency multipliers and dividers
7. Tracking filters
8. Frequency synthesizers
9. Tuned AM detectors
10. SCA "storecast music" demodulators
11. Frequency-shift-keyed (FSK) telegraph receivers and phase modulators
12. Tone decoders

PLLS USING THE HA-2800/2805

The HA-2800/2805 monolithic IC's are extremely versatile PLLs designed for a maximum number of general purpose applications such as those just cited. The HA-2800/2805 is also well suited for specialized designs and applications because it has provisions for:

a. Opening the loop at several points for including special purpose circuitry such as between the phase detector and CCO to employ the designer's choice of active and/or passive low pass filters, or between the CCO and phase detector to employ flip-flops for frequency division.

b. Independent, external adjustment of both demodulation gain and loop gain.

c. Phase demodulation through independent adjustments of loop and demodulation bandwidths.

d. Direct CCO output compatibility with either TTL or ECL when used with a logic power supply and -V.

e. Controllable tracking range without disturbing the temperature coefficient of the free-running frequency, f_o. (Typical T.C. for f_o is 250ppm/°C and 0.1%/volt). These features coupled with the excellent performance parameters of the HA-2800/2805 present the designer with many degrees of freedom for tailoring PLL techniques to his particular application.

The significant characterization parameters for the HA-2800/2805 PLLs can be interpretated by considering the linear model shown in Figure 3. This model is applicable whenever lock is established between the input signal and the CCO output. The conversion gains, K_d and K_o, are treated as constants in the "small-signal", linear model of Figure 3. However, the specific values of K_d and K_o which should be used depend upon the parameters of the "quiescent operating point", particularly the free-running frequency and the input signal level.

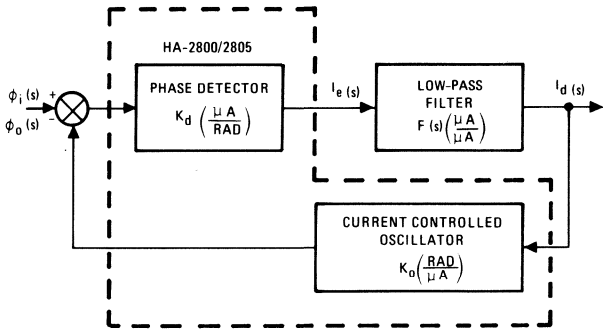


Figure 3

Linear Model of a PLL System Showing Coefficients and Dimensional Parameters of Phase Detector, Low-Pass Filter and Current Controlled Oscillator.C

Evaluation of K_d and K_o for virtually any set of operating conditions is a straightforward process using the graphs and information supplied on the HA-2800/2805 data sheet. An example will illustrate their evaluation.

EXAMPLE OF K_d AND K_o DETERMINATION

Consider that a 10mV rms input signal is to be applied to the PLL which has a free-running frequency of 1MHz. Figure 4 shows graphs of typical HA-2800/2805 loop gain and oscillator frequency vs. input current performance. From (a), the slope of the loop gain characteristic is approximately 1% $\Delta f/f_o$ per degree

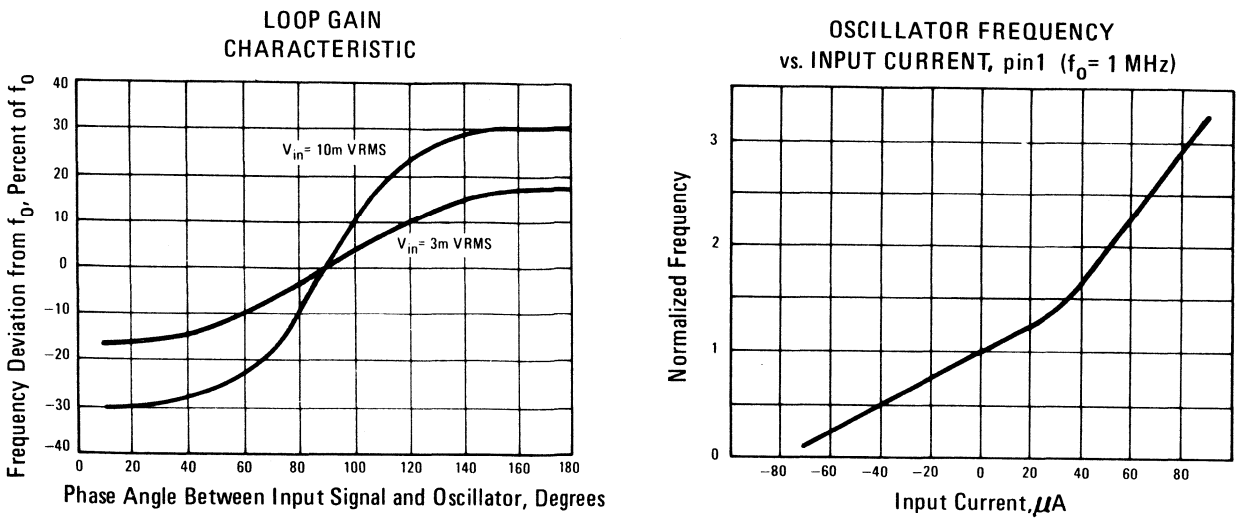


Figure 4

Characteristics of the HA-2800/2805 for Determination of K_d and K_o Conversion Gains.

phase angle about the 90° reference phase. As is obvious from the graph, the slope (and ultimately K_d) depends upon the input signal level. This is typical for signal amplitudes from a few microvolts to slightly above 10mV rms where nonlinear operation occurs because of signal-swing limitations. For operation with signal levels below 10mV rms simply scale the slope by a factor of $\frac{V_{in}}{10}$ where V_{in} is the expected input voltage in mV rms.

The graph in (a) was obtained under closed-loop conditions where a simple, passive, R-C, low pass filter was included in the loop whose transfer function was of the form:

$$F(s) = \frac{1}{1+\tau s}$$

at dc:

$$F(0) = 1$$

and the low pass filter does not affect the overall loop gain*. To employ some other type of low pass filter whose transfer function is $F_1(s)$, the slope of the loop gain characteristic would be multiplied by $F_1(0)$.

Part (b) shows the open-loop variation of the CCO frequency as a function of the controlling input current. The slope of this characteristic is approximately $1.2\%\,\Delta f/f_o$ per μA for input current variations less than $30\mu A$. The conversion gain K_d is the quotient of these two slopes, or

$$K_d \cong \frac{\left(1\%\,\frac{\Delta f/f_o}{\text{degree}}\right)}{1.2\%\,\frac{\Delta f/f_o}{\mu A}} \cong .83\frac{\mu A}{\text{degree}} = 48\frac{\mu A}{\text{radian}}$$

The K_o conversion gain of the CCO is the slope of Figure 4 (b) multiplied by the desired free-running frequency, or

$$K_o @ 1MHz = 1.2\%\,\frac{\Delta f/f_o}{\mu A} \times 1MHz =$$

$$1.2 \times 10^4\,\frac{Hz}{\mu A} = 7.5 \times 10^4\ \text{Rad/sec}/\mu A$$

The value of K_o at other frequencies between the limits of 1kHz and 25MHz may be found by scaling K_o according to

$$K_o @ f_o = (.012)(2\pi f_o)\ \text{Rad/sec}/\mu A$$

Where f_o is the free-running frequency of the CCO.

The product of K_d, K_o, and F(0) constitute the dc loop gain. Note that the dimensions of $K_dK_oF(0)$ are 1/sec. The dc loop gain defines the tracking range Δw_T, which is the range of frequencies centered about the free-running frequency over which the PLL can maintain lock. Note that additional dc gain may be easily designed into the HA-2800/2805 because the loop is not closed internally, allowing one or more amplifiers to be included in both the forward and feedback signal paths.

* For a further explanation, see Harris Application note 602.

The tracking range for the 1MHz example is:

$$\Delta w_T = \pm K_d K_o F(0) = \pm(48)(7.5 \times 10^4)(1) =$$

$$\pm 3.6 \times 10^6 \text{ Rad/sec}$$

This Δw_T corresponds to a frequency deviation of ±570kHz indicating that the PLL can track input frequencies from approximately 430kHz to 1.5MHz. The Δw_T expression is valid as long as nonlinear operation due to saturation or limiting do not occur within the loop, thereby producing a smaller value of Δw_T. (This effect will be discussed subsequently).

CONNECTING THE HA-2800/2805

As was previously shown in Figure 1, the HA-2800/2805 PLL features a dual-ended input to the phase detector through external capacitors C_1 and C_2 at pins 7 and 10. The size of these coupling capacitors isn't critical except that they be large enough to pass the minimum input frequency of interest. They should be chosen in accordance with:

$$C_1 = C_2 \geq \frac{10}{2\pi(2K + R_S)f_{min}}$$

where 2KΩ is the typical input impedance between pins 7 and 10 and R_S is the source impedance. For a typical 50Ω coaxial line,

$$C_1 = C_2 \geq \frac{.78}{f_{min}} \ \mu f$$

where f_{min} is in kHz. The input terminal to either capacitor may be grounded through a resistor equal to R_S if single-ended operation is desired.

The phase detector supplies two balanced, high impedance (typically 8MΩ), current-source outputs at pins 9 and 12. Since these outputs are isolated from one another, different filter functions can be connected at the two outputs without interaction. One such filter for de-emphasis in the standard FM broadcast band is obtained by connecting a parallel resistor-capacitor combination at pin 9 (R_3 and C_3 of Figure 1). The R_3C_3 time constant is nominally chosen as 75 microseconds. The amplitude of the demodulated output voltage available at pin 8 is adjustable via R_3 as shown in Figure 5. The low impedance level afforded by the NPN-PNP complementary emitter followers makes this output particularily useful for driving virtually any power amplifier.

DEMODULATED OUTPUT SWING
vs. INPUT FREQUENCY DEVIATION

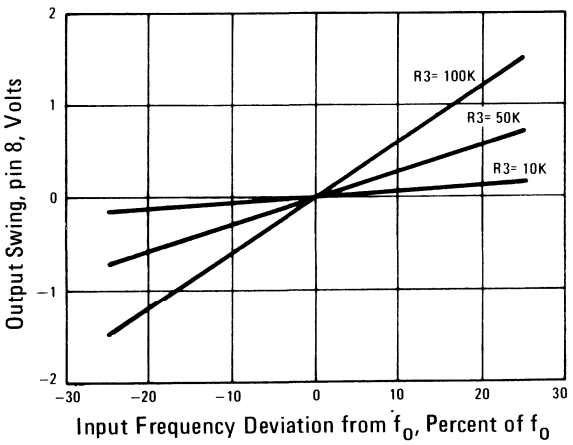
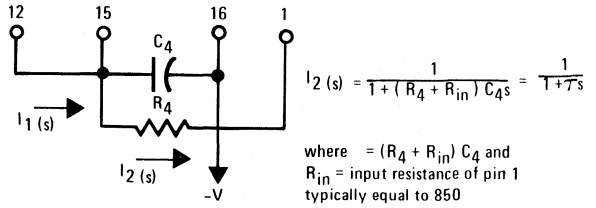


Figure 5

The second output from the phase detector (pin 12) is not internally connected to the CCO which allows the designer to choose the low pass filter needed for a particular application. The frequency characteristics of this filter determine the sensitivity of the PLL by setting the capture range, Δw_C, which is the band of frequencies centered at f_O where the PLL can move from the unlocked state to establish or acquire lock with an input signal. The capture range is always less than the lock range, and can be estimated by:

$$\Delta w_C \approx K_O K_d \ |F(j\Delta w_C)| \quad \text{where} \quad |F(j\Delta w_C)|$$

represents the magnitude of the low pass filter at a radian frequency, W, equal to the capture range Δw_C.



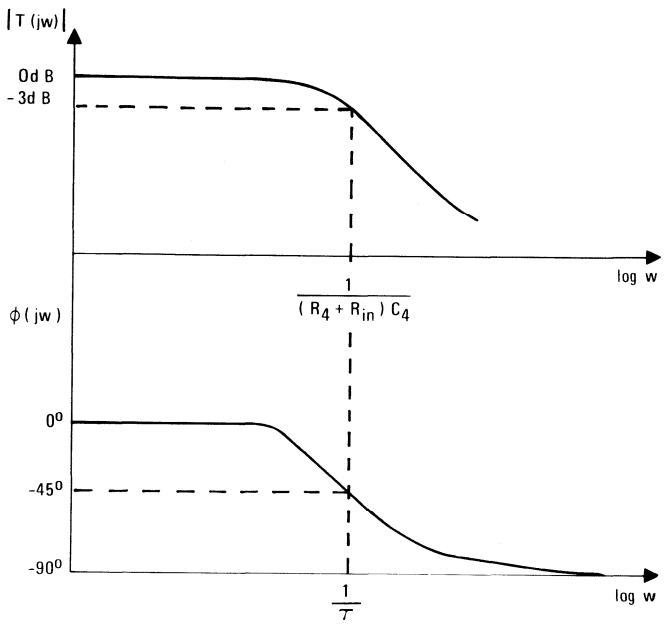


Figure 6

Simple RC Low Pass Filter Connections and Response

The connection scheme for a simple low pass RC filter to the PLL is shown in Figure 6, together with a Bode plot indicating the filter's frequency characteristics. If the time constant τ of this filter is chosen such that

$$\tau \gg \frac{1}{2\Delta w_T}$$

the capture range can be approximated as

$$\Delta w_C \approx \pm \sqrt{\frac{\Delta w_T}{\tau}}$$

As a practical example, for R_4 = 10K and C_4 = 200pF at f_o = 1MHz,

$$\Delta w_C \cong 1.3 \times 10^6 \text{ Rad/sec}$$

giving a capture frequency range of approximately 200kHz. Thus for f_o = 1MHz with this filter, the frequency of the input signal must be in the range between approximately 800kHz and 1.2MHz to establish phase lock. However, once lock is established, the PLL system will track all input frequencies between 430kHz and 1.5MHz. The capture range may be adjusted between the limits of 0 to Δw_T by varying filter time constant τ.

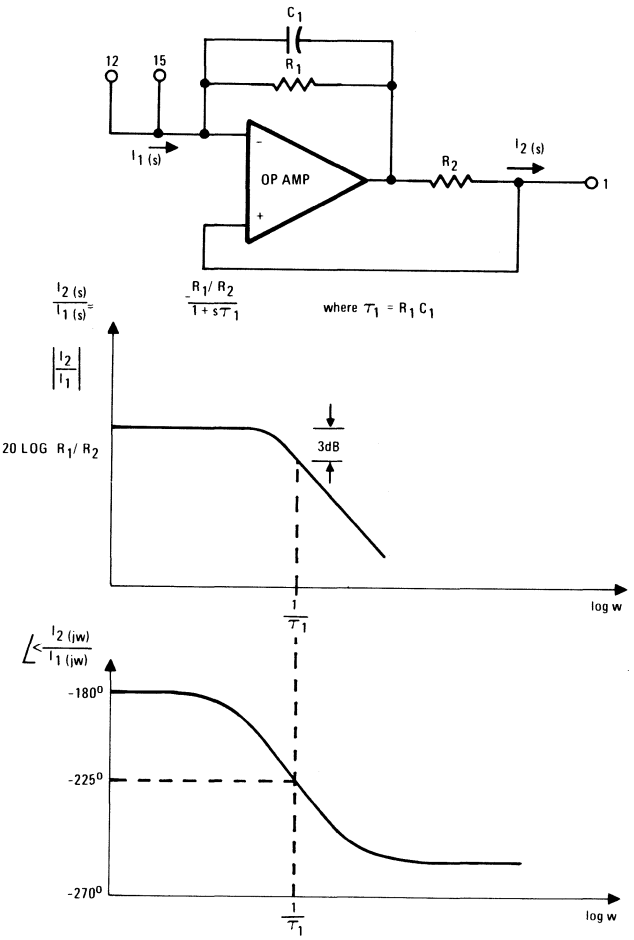


Figure 7

An Active RC Low Filter And its Bode Plot

An active, low pass filter such as shown in Figure 7, may be employed in the PLL system. The response of this filter is identical to that of the passive filter except for the gain term R_1/R_2. By varying the forward current gain of the filter, the loop gain can be adjusted to control both the tracking range Δw_T and the capture range Δw_C.

Internal bandwidth control is provided by the clipping network and unity gain amplifier (pins 1 and 15 of Figure 1). Figure 8 shows an isolated view of this stage, together with a sketch of its current transfer function. The current I_d represents the dc component of the output signal from the phase detector. I_{cco} is the input current to the CCO which adjusts its frequency about f_o. R_{cco} is the input resistance of the CCO (typically 850Ω at pin 1). The clipper diodes short when $V_d - V_{cco} = \pm 750mV$, limiting I_{cco} to maximum and minimum values of $\pm \frac{750}{R_4}\ \mu A$ (R_4 in K Ωs). By this clipping action, the bandwidth of the CCO is limited to

$$\Delta w_{cco} = \pm \frac{750}{R_4} K_o \quad \text{Rad/sec}$$

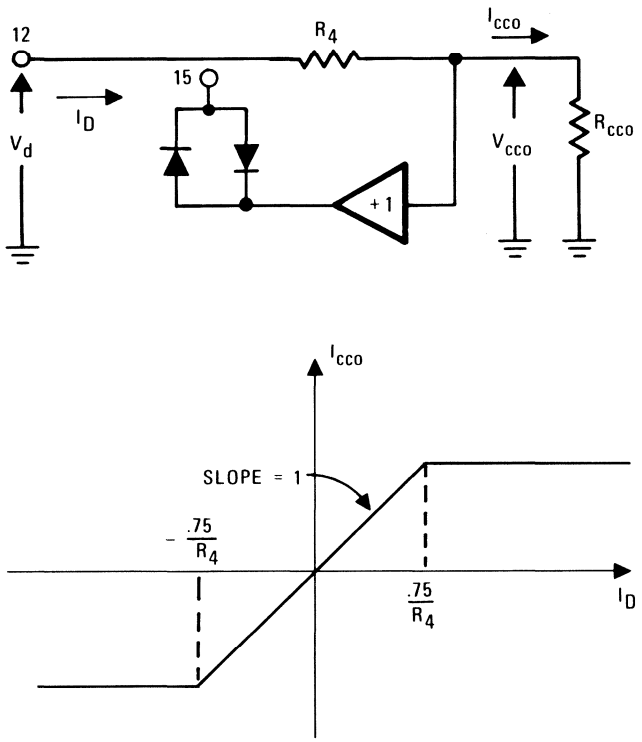


Figure 8

The Current Clipping Network and its Transfer Characteristic

Evaluating Δw_{cco} for the previous 1MHz example with R_4 = 10KΩ gives

$$\Delta w_{cco} = \pm 5.6 \times 10^6 \quad \text{Rad/sec}$$

or a possible CCO frequency change of ±900kHz. Since $\Delta w_{cco} > \Delta w_T$ for this R_4 = 10K, the tracking range is controlled by the dc loop gain and not this clipping network. If R_4 were adjusted to 100KΩ, the tracking range bandwidth would be set by the clipping network to 90kHz. Figure 9 shows the typical variation of the tracking range for three different R_4 settings.

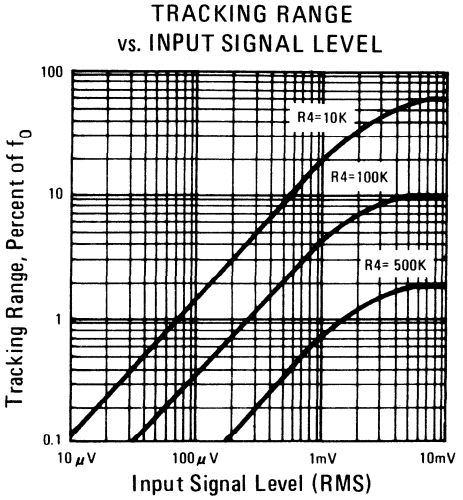


Figure 9

The clipping network also controls the maximum detectable phase shift in the loop. The phase detector's output current is

$$I_D = K_d (\phi_i - \phi_o)$$

where ϕ_i and ϕ_o are the phase angles of the input and CCO signals, respectively. Current limiting in the clipper of I_{cco} gives a maximum phase shift of:

$$(\phi_i - \phi_o)\ max = \pm \frac{750}{R_4 K_d} \quad \text{(Radians)}$$

The free-running frequency of the current controlled oscillator is determined by the value of capacitance C_T connected between pins 3 and 14. Figure 10 shows typical C_T values for setting f_o over its specified range of 1kHz to 25MHz. The f_o temperature coefficient of the HA-2800/2805 is a remarkable 250ppm/°C over their full temperature ranges. This high degree of stability makes these devices particularly useful as narrowband filters in remote locations.

CENTER FREQUENCY, f_0
vs.
TIMING CAPACITOR, C_t

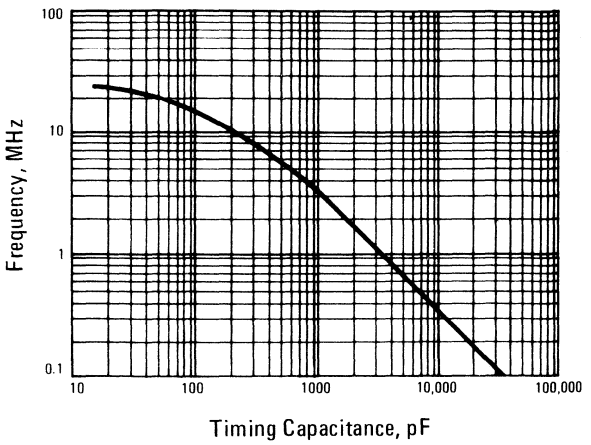


Figure 10

The dual outputs from the CCO (pins 5 and 13) are 180° out of phase and isolated from one another and can be made directly compatible with ECL or TTL by simply operating the HA-2800/2805 at the appropriate logic power supply levels. Because of this compatibility and because no internal connection is made between the CCO's output and phase detector's input, virtually any type of digital counter/divider can be inserted into the loop at this point. Thus, the PLL can be easily programmed to lock on subharmonics of f_0.

CIRCUIT ANALYSIS OF THE HA-2800/280

The schematic diagram of the HA-2800/2805 phase-locked loop system is shown in Figure 11. The circuit configurations for the basic phase detector, current-controlled oscillator, buffer amplifier and clipper network are partitioned by the dashed lines to better identify these functions on the schematic diagram.

As explained previously, the phase detector is basically an analog multiplier. The circuit employed in the HA-2800/2805 multiplies by using the transconductance principle. The input signal applied at pins 7 and 10 produces ac currents I_1 and I_2 which are directly proportional to the applied input signal or:

$$I_1 = K_1 V_X = -I_2$$

where K_1 is a constant and V_X represents the ac input voltage. Changing I_1 in accordance with V_X changes the effective input impedance of the difference amplifier composed of Q10, Q11, Q12 and Q13. The input impedance at the Y input (pins 6 and 11) is inversely proportional to the current I_1, or

$$R_i = \frac{R_2}{I_1} \quad (K_2 \text{ is a constant})$$

The voltage gain of the Q10 - 13 difference amplifier is given by

$$A_V = \frac{V_O}{V_X} = A_I \frac{R_L}{R_i} = \frac{K_3}{R_i} \quad (K_3 = \text{constant})$$

where A_I is the effective current gain of the stage and R_L is the effective load impedance. Thus, the output voltage from the phase detector can be expressed as

$$V_O = V_X \frac{K_3}{R_i} = V_X \frac{K_3}{K_2/I_1} = \frac{K_3}{K_2} K_1 V_X V_Y$$

$$V_O = K_4 V_X V_Y \quad \text{where } K_4 = \text{constant.}$$

This output voltage is converted to an output current signal ($I_O = K_5 V_X V_Y$) by the Q5 stage. Thus the current signal at pin 12 represents the analog multiplication between the two x and y inputs. A second current signal, proportional to the $V_X V_Y$ product and buffered from the first is available at pin 9.

The current controlled oscillator is basically an astable multivibrator with coupling between the emitters of Q72 and Q73 via the C_T tuning capacitor. The quiescent collector currents of Q72 and Q73 are modulated by the document supplied at the low impedance input of pin 1. An increase in the input current at this input is amplified by the Q59-Q60 emitter-follower stages to produce an increase in the collector currents of Q72 and Q73. When the timing capacitor C_T is in position, astable operation occurs because of

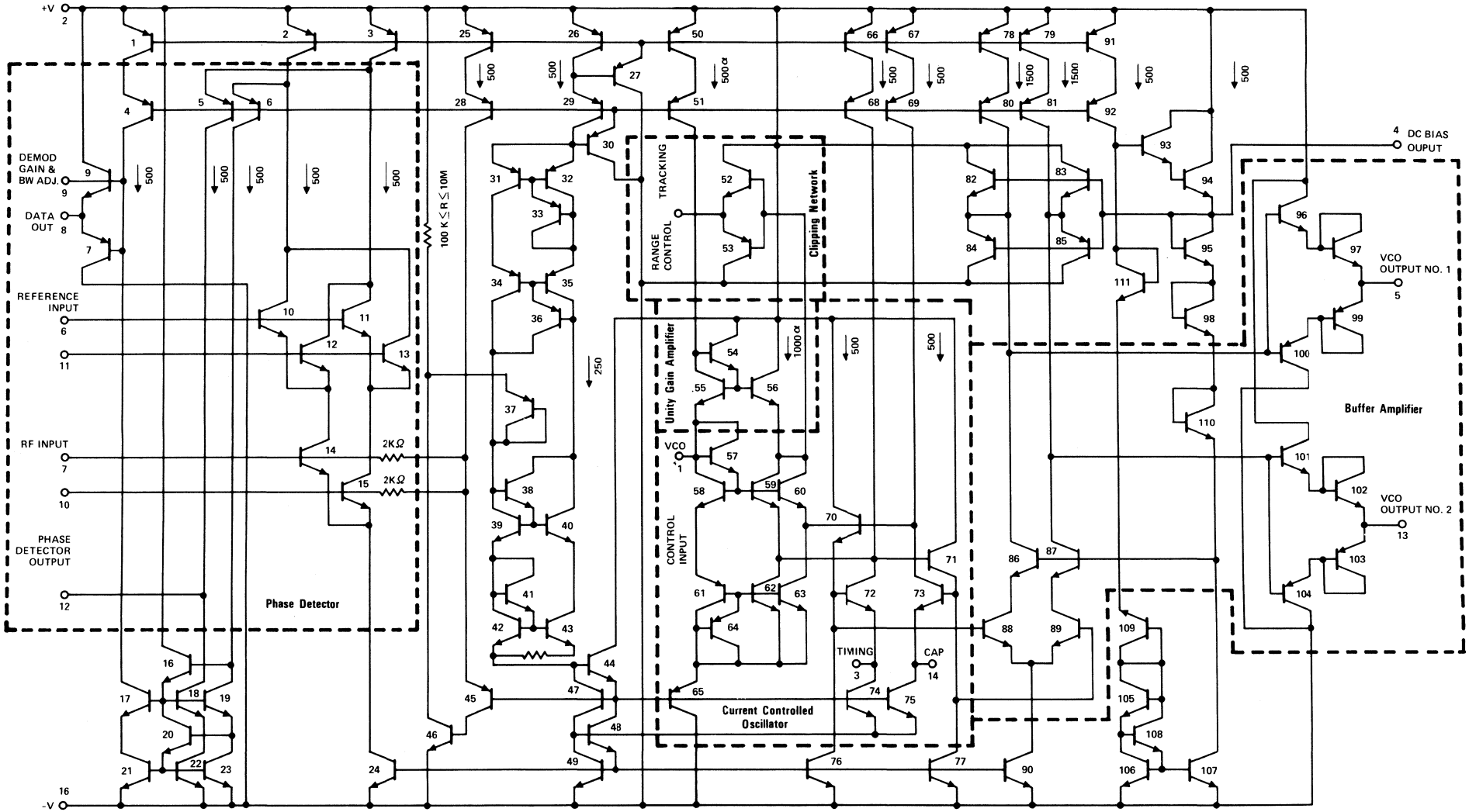


Figure 11

High Frequency Phase Locked Loop

the presence of positive feedback where the loop gain around Q70 through Q73 is greater than unity. The frequency of oscillation is directly proportional to the input current externally supplied at pin 1. Thus, $f_o = KI_{in}$. Figure 4b shows the effect supplying an external dc current to the CCO has upon its output frequency.

Two differential outputs are taken from the current controlled oscillator at the bases of Q72 and Q73. These signals are used to drive the differential input stage of the buffer amplifier (Q88 and Q89). Complementary outputs are provided to pins 5 and 13 through the identical NPN-PNP stages of Q96(Q101), Q97(Q102), Q99(Q103), and Q100(Q104). The low impedance levels at pins 5 and 13 allow for external monitoring of the controlled frequency as well as for using these points as source signals for the phase detector via pins 6 and 11. Up to 10mA of drive current can be supplied by this buffer amplifier.

P.L.L. PARAMETERS

This section briefly explains the meaning attached to several key specifications of the HA-2800/2805 High Frequency Phase Lock Loop. We will discuss these parameters in the order in which they appear on the data sheet.

The question most often asked about certain phase locked loop parameters appearing on a specification sheet is, "What do they mean and how can I interpret them for my application?"

The Input Voltage entry of 2 VRMS under the absolute maximum ratings heading represents an upper limit for amplitude of the input signal to the phase detector at pins 7 and 10. This rating will be significant in TTL frequency synthesizer applications where the input signal (or signals) is obtained from the output of a counter. (See Application Note 604 for a further discussion.) All other entries under this maximum ratings heading are self-explanatory or conform to conventional definitions.

Our remaining discussion will relate to the noteworthy parameters entered under the electrical characteristics heading.

PHASE DETECTOR

The typical 2KΩ input impedance is measured between pin 7 and pin 10. It is not the impedance from pin 7 or pin 10 to ground. This distinction is important when the PLL is connected to differential signal sources. The 2KΩ value is considered when choosing the size of the input coupling capacitors.

Linear operation of the Phase Locked Loop (PLL) is possible over the .02 to 400mV rms Input Voltage Range specified. Phase lock is difficult to achieve at the 20μ V lower limit. Saturation and nonlinear operation occurs at the 400mV rms upper limit. The input signal amplitude also affects the loop's tracking range.

The typical 8MΩ Output Impedance is significant only to illustrate that these outputs represent a current source rather than a voltage source.

The Output Offset Current at pins 9 and 12 is the phase detector's output current measured with the loop opened between the phase detector and the low pass filter. The test is made under zero input signal conditions applied at pins 7 and 10. Under closed-loop conditions, the offset current will be reduced by a factor of K_d. K_d is the phase detector's conversion gain — see next entry for a further explanation. This, in turn, causes a small phase offset within the loop, i.e. the phase angle between the input and the CCO will not be exactly 90^o ($\pi/2$ radians) but $\pi/2 \pm I_{offset}/K_d$ radians. Any temperature drift in offset current will cause a drift in the closed-loop center frequency; but this effect is included in the guaranteed temperature drift curve.

The Conversion Gain of the phase detector, K_d, is a measure of detector's sensitivity to phase differences between the input signal

and the signal fed back from current controlled oscillator. From the data entry here, we see that the phase detector will typically give an output signal of 50 μA for every 1 radian of phase difference. The characteristic of the phase detector is similar to a cosine curve, so the conversion gain is measured as the slope of the characteristic as it passes through 90°. At input levels less than 5mV rms, K_d will vary with input level. The Performance Curves on the last page of the data sheet show that the oscillator frequency will typical change 70% for a 50 μA input current.

Specific values of conversion gain in an open-loop environment are highly dependent upon the test conditions, most notably the amplitude of the input signal. However, closing the loop and utilizing negative feedback reduces K_d variations. Application Notes 602, 603, and 606 present a further clarification of this concept.

CURRENT CONTROLLED OSCILLATOR

The free-running or center frequency, f_o, (unlocked loop condition) of the oscillator is set by the size of an external capacitor. Practical limitations of this capacitance affect both the upper and lower frequency ranges. Highly stable, low leadage capacitors are rare above 10μf, which limits the lower end of the frequency range to approximately 1kHz. The Maximum Frequency is limited by internal and external stray capacitances to typically 30MHz.

The Frequency Drift is the change in f_o under open-loop conditions per °C change in temperature. The curve on page three of the data sheet shows typical and guaranteed frequency drifts.

The Frequency Change with Supply Voltage is the percent f_o change (open-loop) accompanying a one volt change in the power supply voltages. The change is taken about the +5 and -15 volt test levels.

The low value of 850Ω Input Resistance implies that the CCO is sensitive to a current (as opposed to a voltage) input signal. This resistance should be considered in the design of the low pass filter.

The Input Open Circuit Voltage, pin 1 represents a dc reference level at the CCO input. This level should be taken into consideration if an active, low pass filter is used here or if an external ramp current is applied to pin 1 to sweep the CCO frequency.

The Clipping Level, pin 15, of ±0.7 volts results from the two parallel diodes connected to the output of the unity gain amplifier. The clipping level is referenced about the Input Open Circuit Voltage of pin 1. The clipping network provides independent control of the tracking range through R_4 selection.

The Conversion Gain, K_o, specifies the sensitivity of the oscillator's frequency to change in accordance with changes in the input current from the pahse detector and low pass filter. We see that 1 μA will typically change the CCO frequency by 1%. This Conversion Gain is simply the slope of oscillator frequency vs. input current curve shown on the last page of the data sheet.

The Output Voltage and Output Rise and Fall Times are particularly significant when interfacing the CCO output with a digital counter. Application Notes 604 and 606 describe the specifics of interfacing the HA-2800/2805 with ECL and TTL lines.

CLOSED LOOP CHARACTERISTICS

The Loop Gain is the product of the phase detector's and current controlled oscillator's conversion gains, i.e. K_dK_o. We see from the typical specification that a 1 radian difference in phase will change the free-running frequency of the CCO by 50%.

The Tracking Range is significant when phase lock has been established. The typical specification shows that the frequency of the input signal may change by 50% from the free-running frequency before lock is broken.

The HA-2800/2805 has been designed so that the Tracking Range is externally controllable.

The amplitude of the Demod. Output Swing at pin 8 depends upon the R_3 resistor connected at pin 9. As the figure on the last page of the data sheet shows, making R_3 a variable resistance provides a convenient "volume control" for the demodulated output signal.

The high stability of the PLL against temperature variations is reflected in the remarkable Frequency Drift specification of 250ppm/^{o}C.

POWER SUPPLY CHARACTERISTICS

Proper operation of the HA-2800/2805 requires a minimum of 12 volts difference between pin 4 and pin 16.

However, the Power Supply Voltage Range of from $\pm$15 volts adds to the versatility and flexibility of the PLL for many combined linear and digital applications.

CONCLUSIONS

This application note summarizes the basic concepts of phase locked loops. A useful linear model applicable to the HA-2800/2805 high frequency PLL is presented and techniques are illustrated for modifying the parameters of this model to accommodate custom designs. The circuit operation of the HA-2800/2805 is also discussed in order to provide a better interpretation of the performance characteristics of the device.

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APPLICATION NOTE 604

F.M. DEMODULATION AND FREQUENCY SYNTHESIS

BY J. A. CONNELLY

APP. NOTES

Several of the most common applicatons for the HA-2800/2805 are discussed in this application note. For applications not described, Harris application notes 601, 602, and 603 should prove helpful by providing an understanding of phase lock loop operation.

FM DETECTOR

The phase locked loop (PLL) accomplishes FM demodulation in a simple manner because the loop locks the frequency of the current controlled oscillator (CCO) to the frequency of the incoming signal. The error signal generated by the phase detector and filtered by the low pass filter keeps the loop locked and constitutes the demodulated FM information. The PLL may be thought of as a matched filter operating as a coherent detector.

The HA-2800/2805 can easily be employed to demodulate the 10.7MHz IF signal in commercial FM receivers. Figure 1 shows the external circuit connections to the HA-2800/2805 for frequency-selective FM demodulation. If demodulation at a frequency other than 10.7MHz is desired, the value of the required tuning capacitor, C_T, may be found from Figure 2. The potentiometer, R_3, provides a convenient method of adjusting the amplitude of the demodulated output signal. Variation of R_3 will typically change this amplitude from 3mV rms to 30mV rms when a 3mV rms, 10.7MHz input signal modulated at 1kHz by a ±75kHz deviation is applied. Figure 3 shows the variation of the demodulated output versus input frequency deviation for different R_3 settings of 10K, 50K, and 100KΩ.

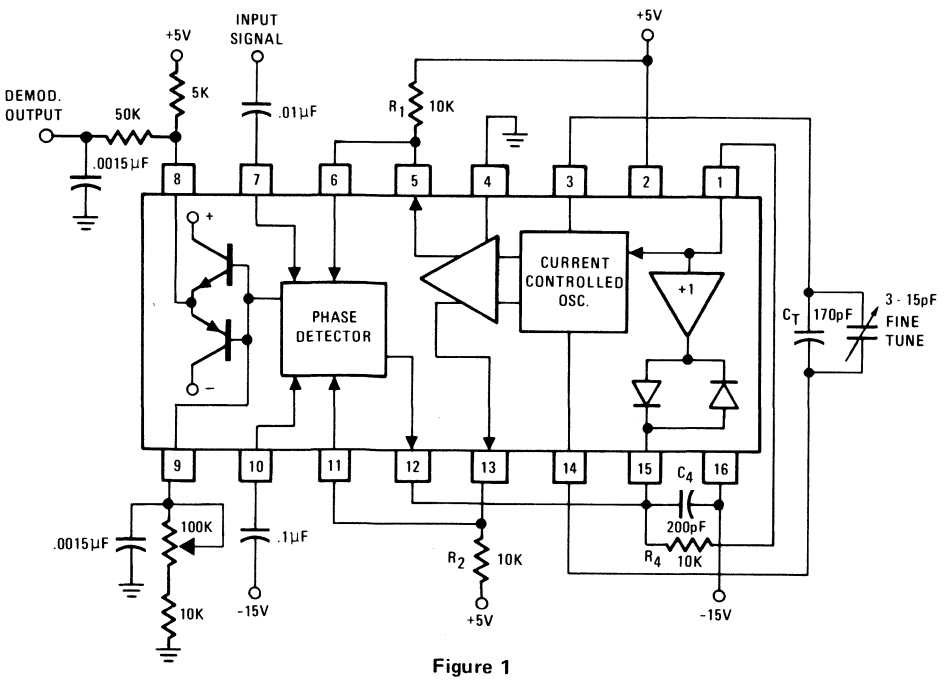

Figure 1

Circuit Connections for FM Detector with the HA-2800/2805 High Frequency PLL

A simple, passive, low pass filter (R4 - C4) is used between the phase detector and the current-controlled oscillator. It is recommended that one terminal of C4 be tied to the negative power supply as shown instead of being grounded. This will provide better rejection of power supply noise. Adjustment of R4 gives independent control of the PLLs tracking range as is shown in Figure 4. Setting R4 to 10K gives a typical tracking range of 4MHz for the same 10.7MHz input signal described previously. The capture or acquisition range is independently controlled by the time constant of the low pass filter. For the R4 - C4 filter shown, the capture range may be approximated by:

$$\Delta w_C \approx \pm\sqrt{\frac{w_T}{R_4C_4}}$$

where Δw_T is the tracking range. The capture range is nominally 900kHz for the test circuit of Figure 1.

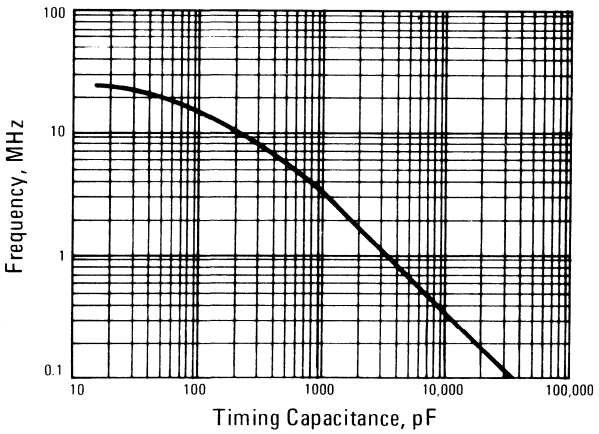

Figure 2
Center Frequency, f_o vs. Timing Capacitor, C_T

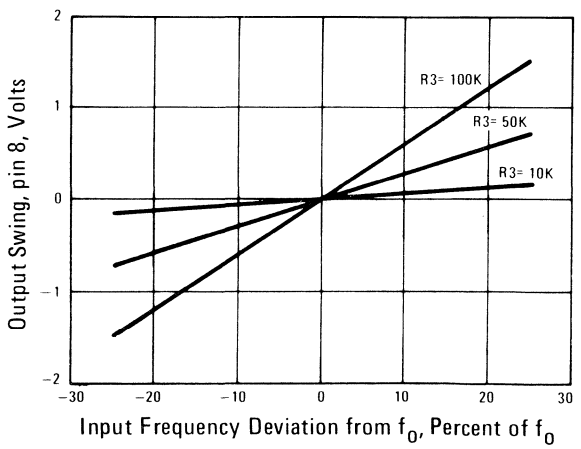

Figure 3
Demodulated Output Swing vs. Input Frequency Deviation

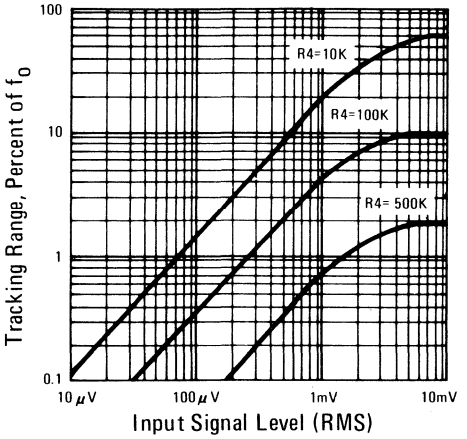

Figure 4
Tracking Range vs. Input Signal Level

The maximum nonlinearity of the FM detector is typically less than 1% at 100% modulation. Signal-to-noise ratio is greater than 40dB for the 0.7% frequency deviation about the 10.7MHz carrier. Total harmonic distortion is less than 1% for the 1kHz modulation Frequency. AM rejection exceeds 45dB.

FREQUENCY SYNTHESIS

Another improtant application of the PLL is for frequency synthesis where a large number of discrete frequencies can be synthesized from a given reference source. Using PLL techniques, the temperature stability and drift characteristics of the synthesized frequencies will be identical to those of the reference source since the loop is phase locked.

Frequency synthesis with PLLs utilizes a programmable counter (divide by N circuit) connected between the output of the current-controlled oscillator (pins 5 and 13) and the input to the phase detector (pins 6 and 11). The counter divides the CCO's output frequency by a programmable integer, N.

Figure 5 shows the circuit connections to the HA-2800/2805 for a frequency synthesizer with N = 4. When the loop is locked to an input signal of fundamental frequency f_S, the synthesized output frequency from the CCO is $Nf_S = 4f_S$. Values of N other than 4 can be easily employed by substituting standard logic connections to produce the desired count/divide sequence.

The output from the CCO can easily be made compatible with TTL and ECL by selecting appropriate power supply voltages. This allows direct connections to be made between the CCO and TTL flip flop, as shown in Figure 5. Virtually any type of flip flop may

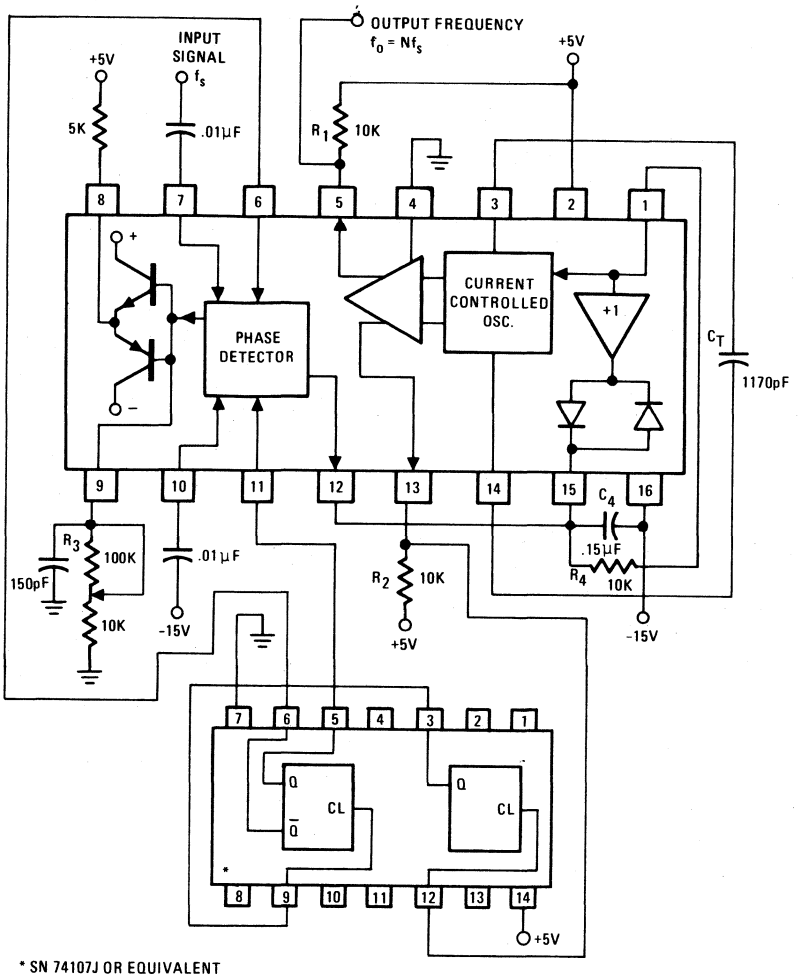

Figure 5
Circuit Connections for Frequency Synthesis

be used provided its $f_{max} \geq f_o$. Both Q and $\overline{Q}$ outputs from the last flip flop are used to drive the differential inputs to the phase detector (pins 7 and 10).

A 1170pF tuning capacitor sets the free-running frequency of the current-controlled oscillator to 1.6MHz. The divide-by-four counter provides a 400kHz as one input to the phase detector and a 3mV rms sinusoidal input signal acts as the other. Phase lock and tracking are possible for the fundamental frequency, (f_S = 400kHz) as well as a number of add harmonics of f_S. Lock could be established for all odd harmonics up to and including the 11th (4.4MHz) with the test circuit of Figure 5. Locking onto odd harmonics is to be expected, since the phase detector acts as an analog multiplier forming the product between the sinusoidal input signal and the square-wave output from the CCO. The product of the odd valued sine wave and the even valued square wave is an odd time function whose fourier spectrum contains only odd terms. When locked to the k^{th} harmonic of f_S, namely f_{Sk} the output frequency at pin 5 is given by:

$$f_o = N \frac{f_{sk}}{k}$$

A second counter may be added to the previous circuit to synthesize numerous output frequencies which are fractionally related to the reference input frequency. The block diagram for such a scheme is shown in Figure 6. The reference frequency input, f_r, is first divided by an integer, M, and applied as the input to the PLL. The PLL then functions as previously explained, but now

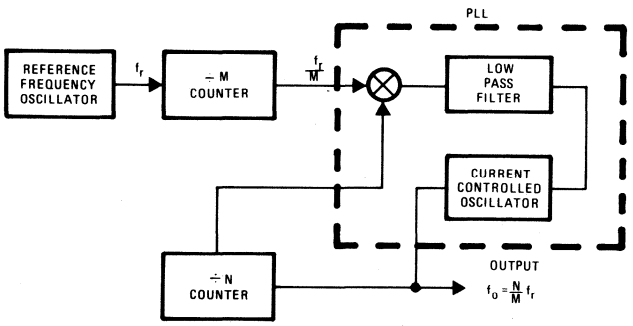

Figure 6

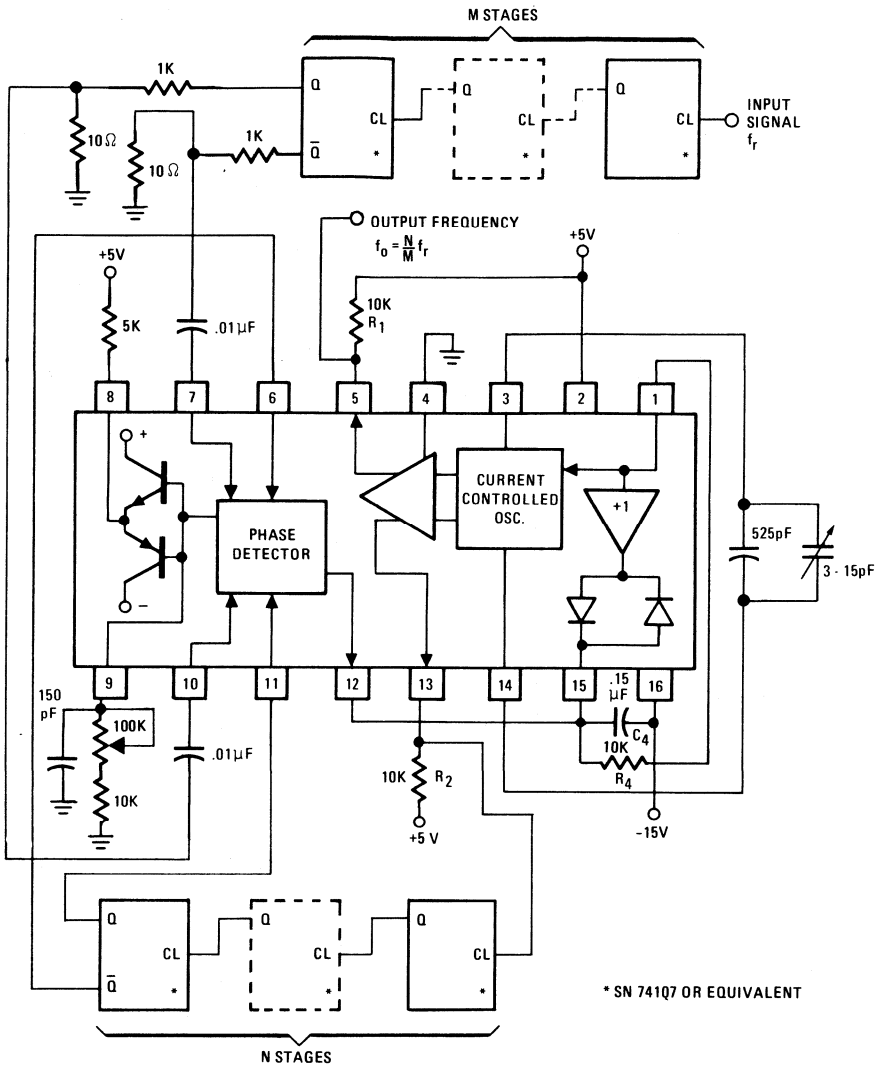

Figure 7
A Synthesizer for Generation Fractional Frequencies

with an input of f_r/M. The synthesized frequency at the output is $f_o = Nf_r/M$. Therefore, by programming M and N, any of a large number of frequencies fractionally related to f_r can be synthesized, each with the stability of the single reference frequency.

The circuit of Figure 7 shows connections to the HA-2800/2805 for fractional frequency synthesis. This circuit is identical to that of Figure 5 except for the divide by M counter stages at the input. The signal level from the last flip flop in this chain should be attenuated to a level less than 400mV rms before being applied to the phase detector (pins 7 and 10). Large voltages here will exceed the input voltage range of the phase detector, thereby causing saturation and preventing the loop from locking into f_r.

This circuit produces an output signal at pin 5 whose frequency is (N/M) times f_r when the loop is locked. Locking of the loop on to harmonics of f_r may occur for the same reasons as discussed previously for Figure 5. Adjustment of the low pass filter time constant by increasing R4 - C4 presents the most direct way to insure proper locking and generation of an output frequency of N/Mf_r.

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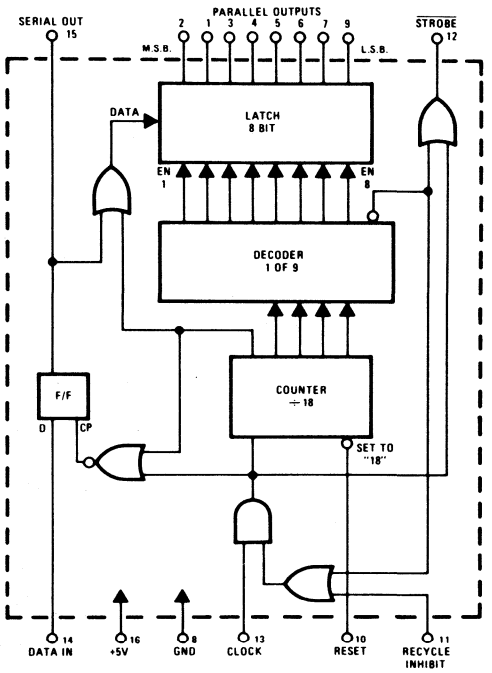
CF-0185

8-Bit A To D Encoder Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.113" x .124"
DIE THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

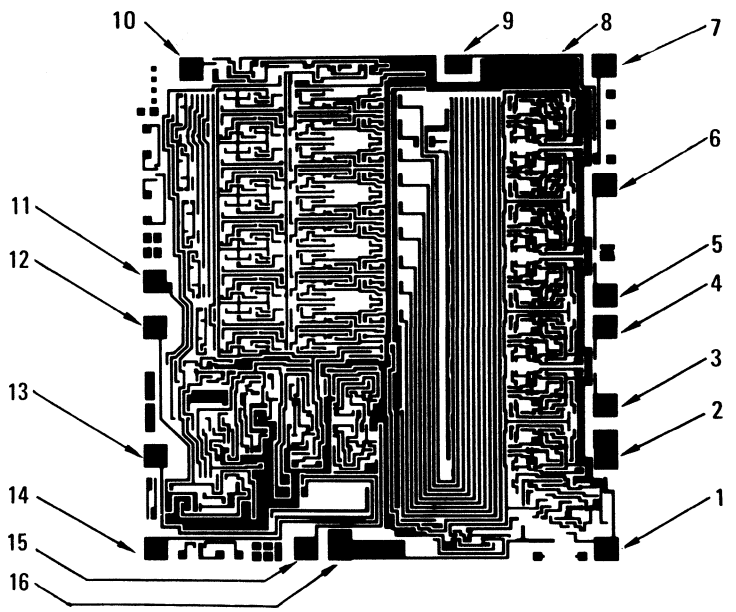
LOGIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	O_1 (M.S.B.)
2	O_2
3	O_3
4	O_4
5	O_5
6	O_6
7	O_7
8	Ground
9	O_8 (L.S.B.)
10	Reset
11	Recycle Inhibit
12	$\overline{\text{Strobe}}$
13	Clock
14	Data In
15	Serial Out
16	+5.0V Supply

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0V
Input Voltage	5.5V
Operating Die Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

$+4.75V \leq V_{CC} \leq +5.25V$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IH}, High Level Input Voltage		2.0			V
V_{IL}, Low Level Input Voltage				0.8	V
V_{OH}, High Level Output Voltage	$I_{OH} = -200\,\mu A$	2.4			V
V_{OL}, Low Level Output Voltage	$I_{OL} = 8.0$ mA			0.4	V
I_{IH}, High Level Input Current	Clock, Data Inputs: $V_I = +2.4V$			200	μA
	Clock, Data Inputs: $V_I = V_{CC}$			2.0	mA
	Reset, Inhibit Inputs: $V_I = +2.4V$			100	μA
	Reset, Inhibit Inputs: $V_I = V_{CC}$			1.0	mA
I_{IL}, Low Level Input Current	Clock, Data Inputs: $V_I = 0.4V$			1.0	mA
	Reset, Inhibit Inputs: $V_I = 0.4V$			0.5	mA
I_{CC}, Power Supply Current			25	60	mA

NOTE: Consult HI-0185 data sheet for typical performance characteristics.

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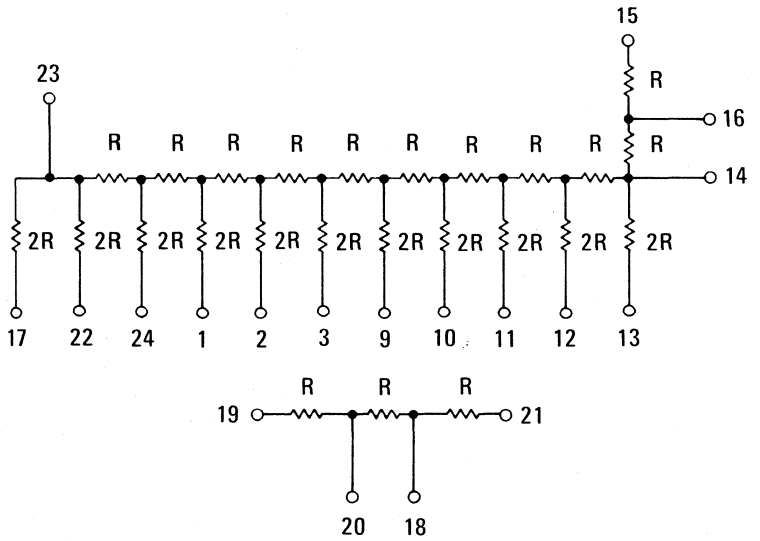
CF-0910/1010

10-Bit D/A Ladder Network Chip

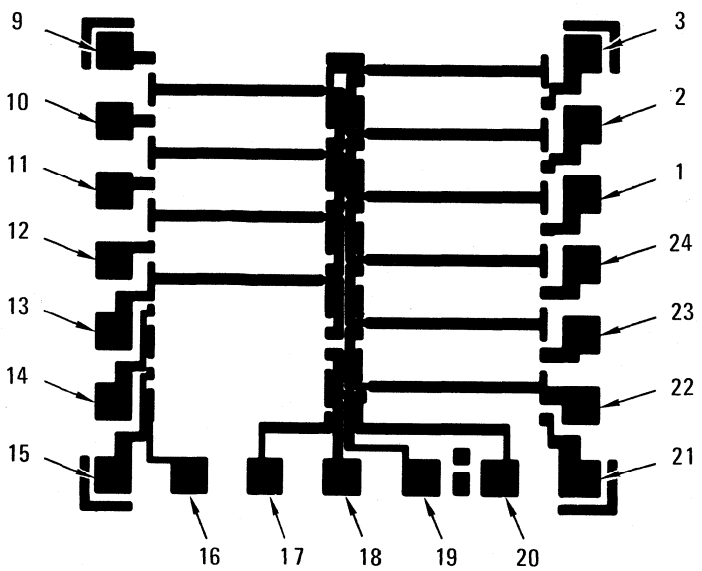
DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.092" x .127"
THICKNESS:	0.0065" ± 0.0010"
PAD DIMENSIONS:	.004" x .004" Min.

SCHEMATIC DIAGRAM



MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Applied: ± 20.0V

Storage Temperature: −65°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions: Applied Voltage: +5.0V or Ground

T_{AMB} = +25°C

Unless Otherwise Specified

PARAMETER	DEVICE TYPE		UNITS
	CF-0910-6	CF-1010-6	
Resistor Value "R" Nom. ± 20%	5K	5K	Ohms
Accuracy (Note 1)	1 Typ.	½ Max.	L.S.B.
Settling Time (Note 2) Typ.	500	500	ns

NOTES: (1) Accuracy is worst case deviation of output voltage from perfect value for any of the 1024 input combinations.

(2) Settling time is the total time measured from an input change until the output settles within ± ½ L.S.B. of its final value.

Test Conditions: $R_L > 1$ megohm, $C_L < 5pF$

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

CF-911

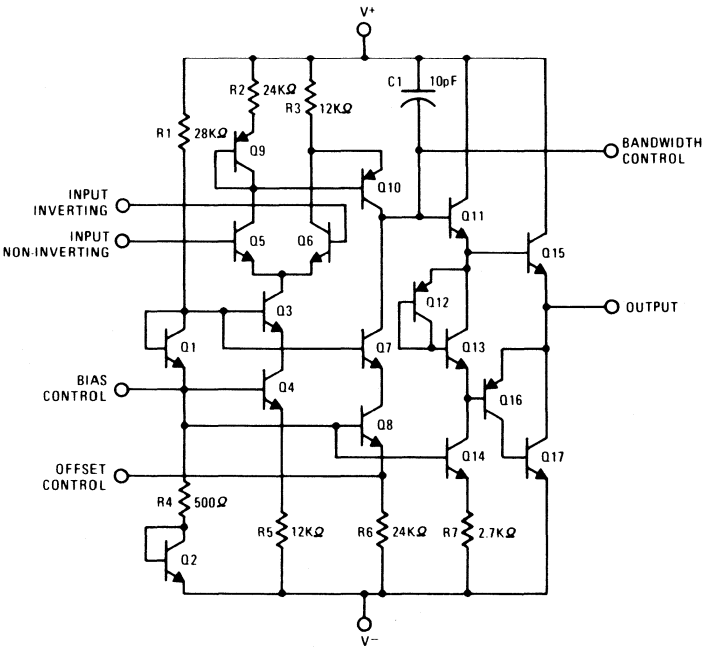
High Performance, Low Noise Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

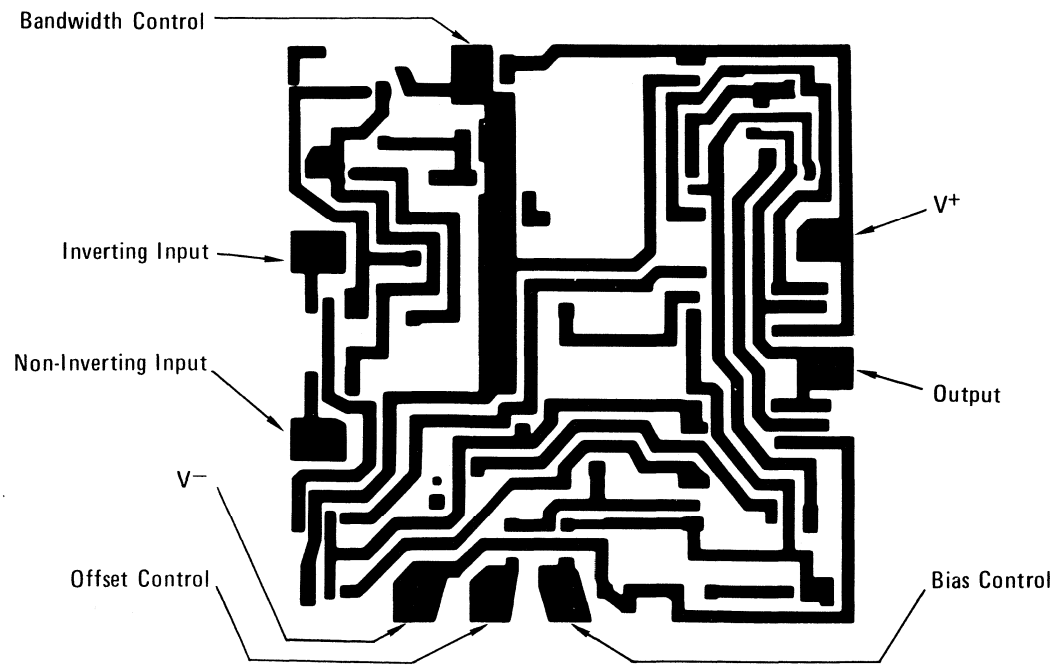
DIE SIZE:	.046" x .046"
THICKNESS:	0.0065" ± 0.0010"
PAD DIMENSIONS:	.003" x .004"

DIELECTRIC ISOLATION

SCHEMATIC DIAGRAM



MASK PATTERN



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	50.0V
Differential Input Voltage	±7.0V
Peak Output Current	±50mA
Operating Die Temperature	-55°C to +125°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		6	mV
Bias Current		500	nA
Offset Current		300	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	20K		V/V
Common Mode Rejection Ratio	74		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±11		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		2.5	mA
Power Supply Rejection Ratio	74		dB

NOTE: Consult HA-911 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

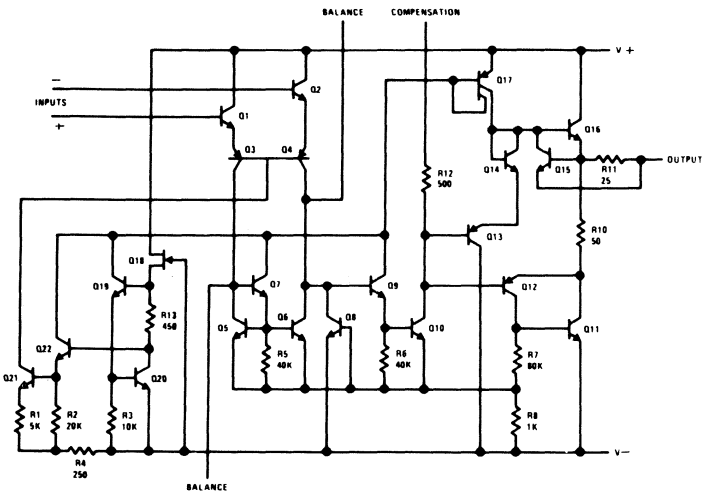
CF-2101

General Purpose Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.050" x .056"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

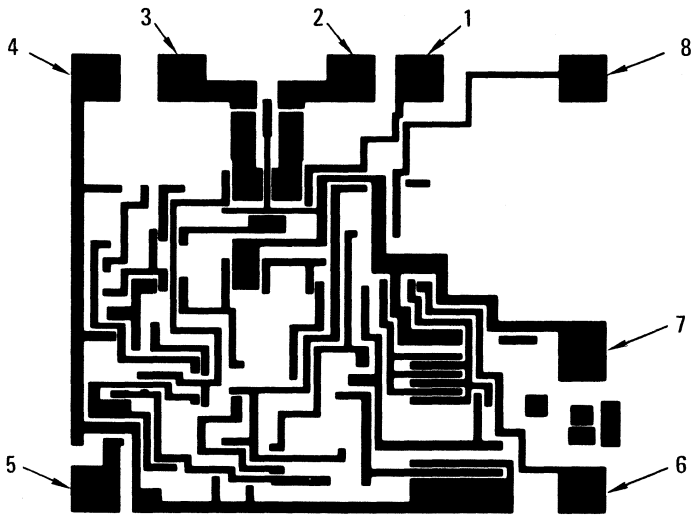
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Compensation

MASK PATTERN



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±30.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		5	mV
Bias Current		500	nA
Offset Current		200	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	50K		V/V
Common Mode Rejection Ratio	70		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		3.0	mA
Power Supply Rejection Ratio	70		dB

NOTE: Consult HA-2101 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

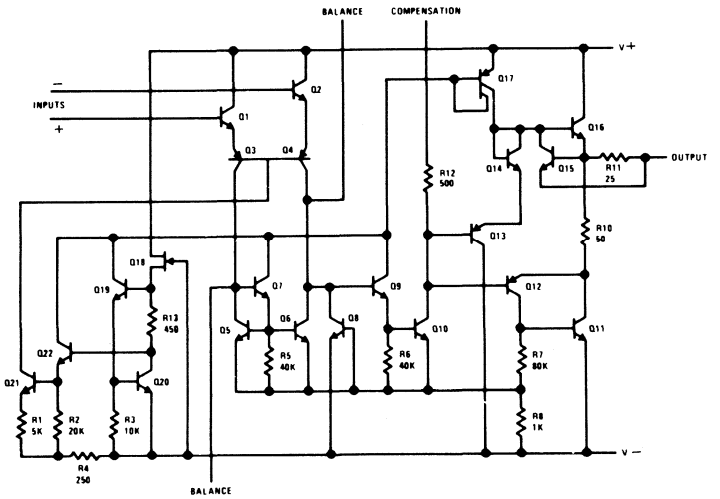
CF-2101A

General Purpose, Low Offset Current Operational Amplifier Monolith Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.050" x .056"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

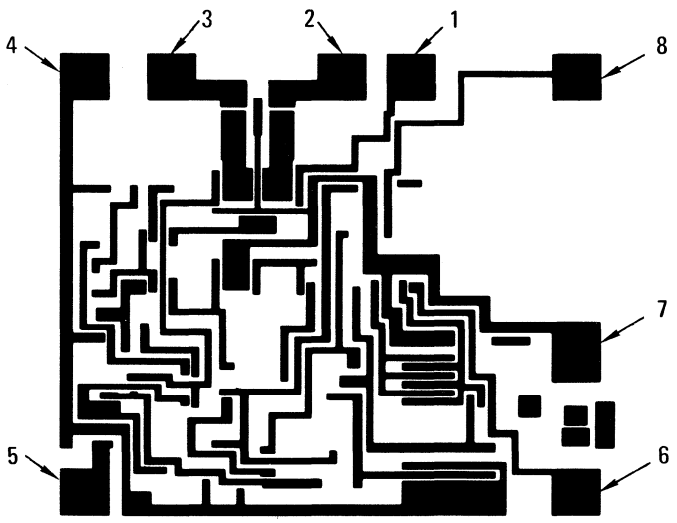
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V−
5	Offset Null
6	Output
7	V+
8	Compensation

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±30.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		2	mV
Bias Current		75	nA
Offset Current		10	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	50K		V/V
Common Mode Rejection Ratio	80		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		3.0	mA
Power Supply Rejection Ratio	80		dB

NOTE: Consult HA-2101A data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

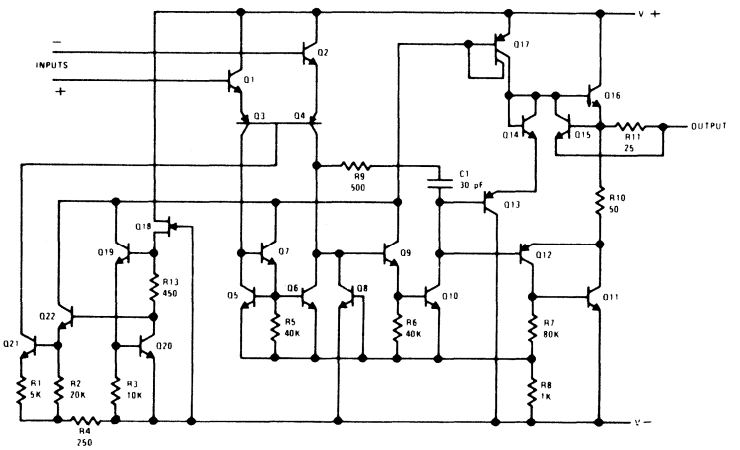
CF-2107

General Purpose, Low Offset Current, Internally Compensated Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.050" x .056"
DIE THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

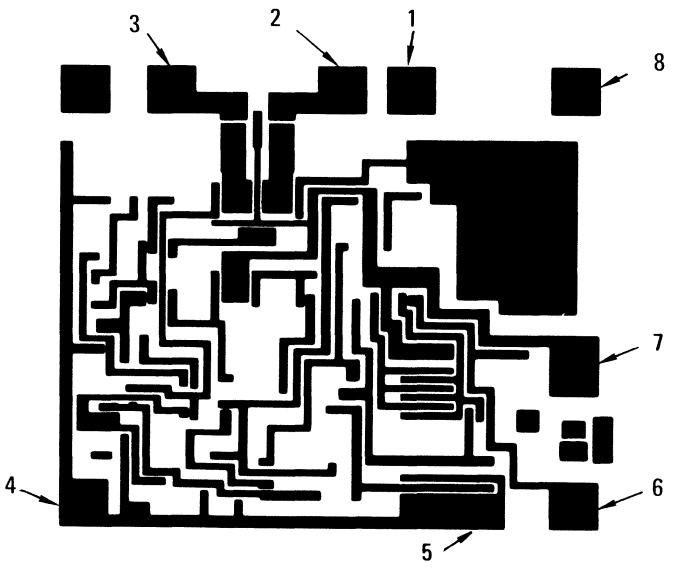
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	NC
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	NC
6	Output
7	V^+
8	NC

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±30.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		2	mV
Bias Current		75	nA
Offset Current		10	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	50K		V/V
Common Mode Rejection Ratio	80		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		3.0	mA
Power Supply Rejection Ratio	80		dB

NOTE: Consult HA-2107 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

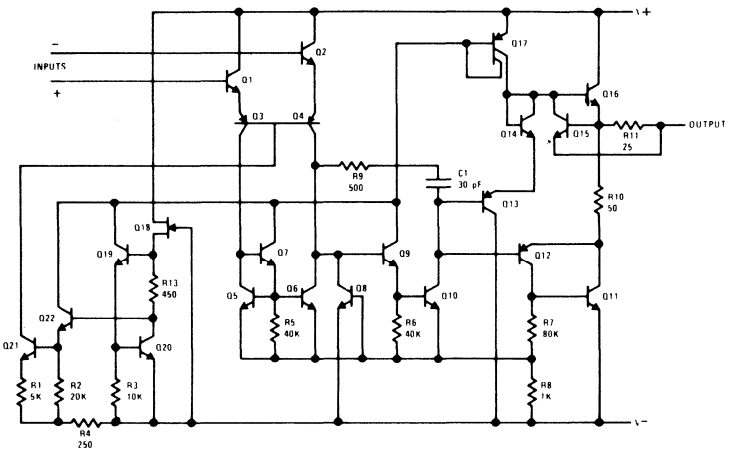
CF-2107-3

General Purpose, Internally Compensated Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.050" x .056"
DIE THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

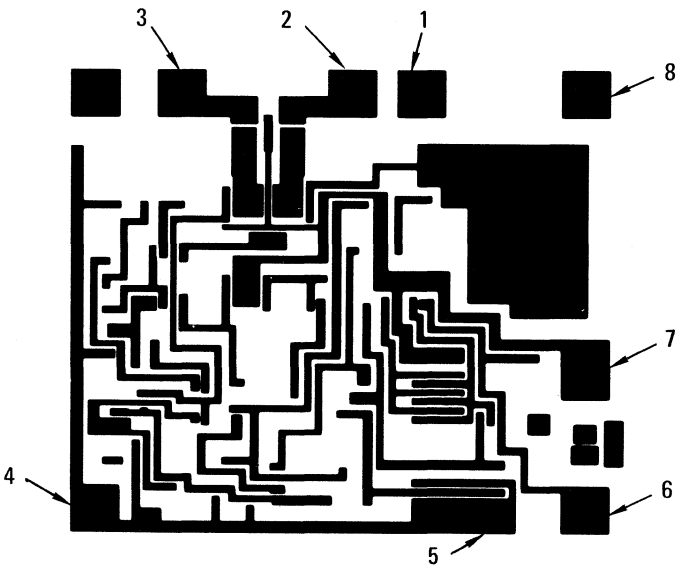
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	NC
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	NC
6	Output
7	V^+
8	NC

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±30.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		5	mV
Bias Current		500	nA
Offset Current		200	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	50K		V/V
Common Mode Rejection	70		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		3.0	mA
Power Supply Rejection Ratio	70		dB

NOTE: Consult HA-2107-3 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

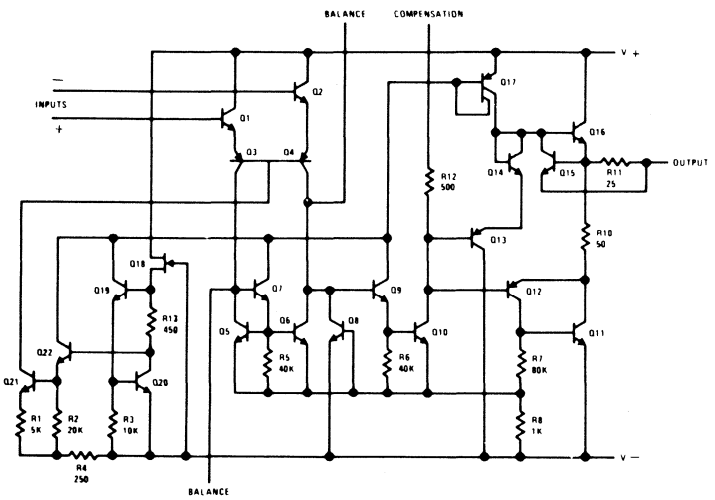
CF-2301A

General Purpose Operational Amplifier Monolitic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.050" x .056"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

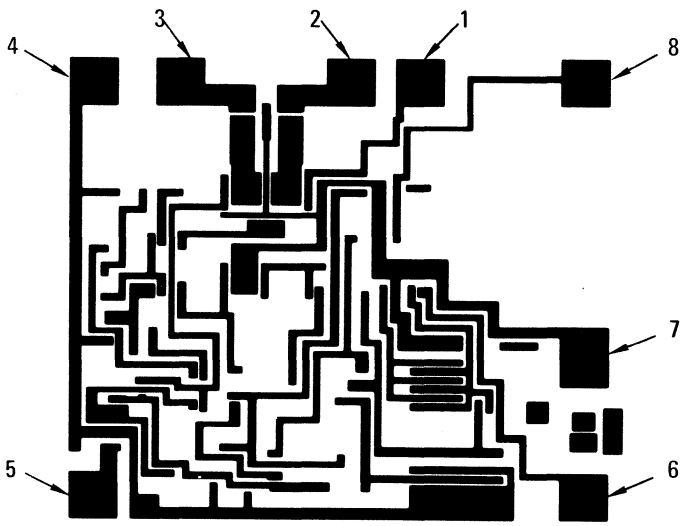
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Compensation

MASK PATTERN



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	36.0V
Differential Input Voltage	±30.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		7.5	mV
Bias Current		250	nA
Offset Current		50	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	25K		V/V
Common Mode Rejection Ratio	70		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		3.0	mA
Power Supply Rejection Ratio	70		dB

NOTE: Consult HA-2301A data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

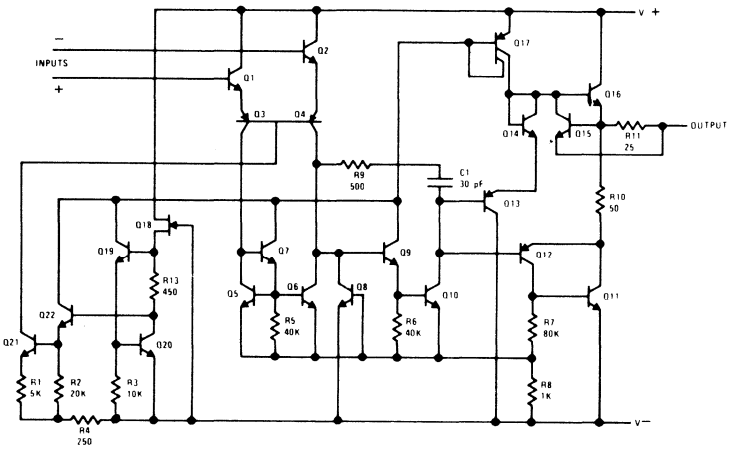
CF-2307

General Purpose, Internally Compensated Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.050" x .056"
DIE THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

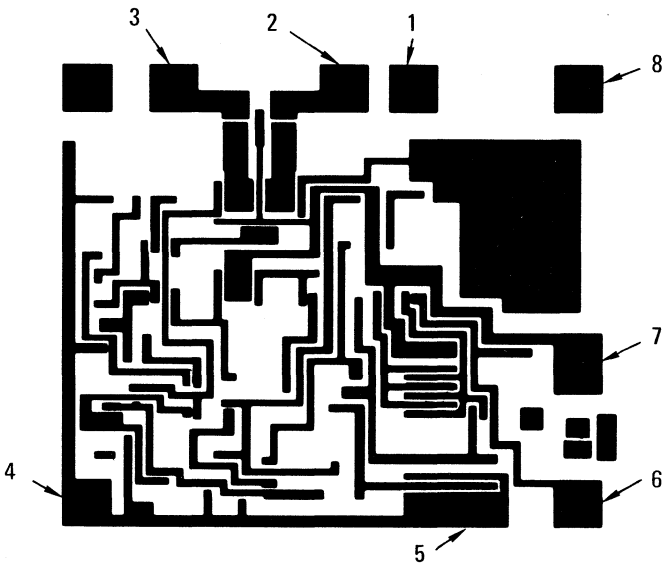
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	NC
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	NC
6	Output
7	V^+
8	NC

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	36.0V
Differential Input Voltage	±30.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		7.5	mV
Bias Current		250	nA
Offset Current		50	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	25K		V/V
Common Mode Rejection Ratio	70		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CURRENT			
Supply Current		3.0	mA
Power Supply Rejection Ratio	70		dB

NOTE: Consult HA-2207 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

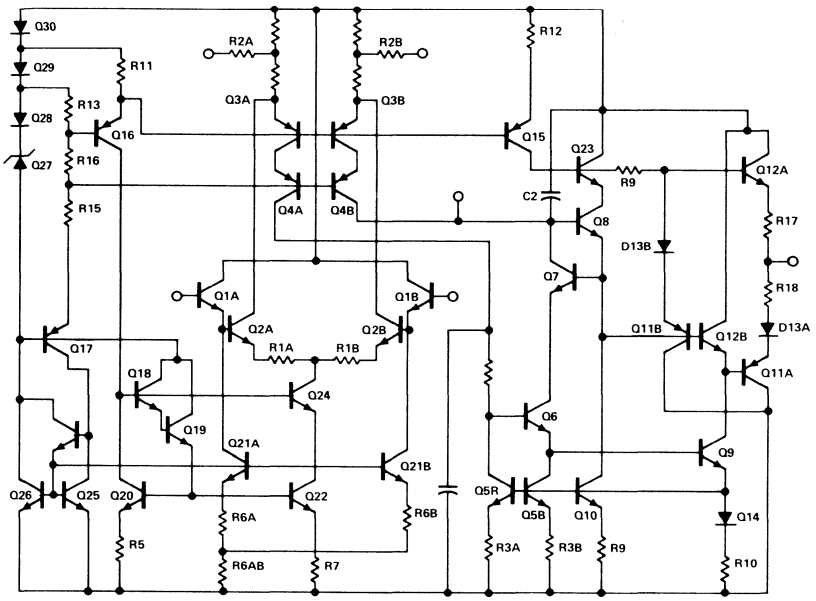
CF-2505

High Slew Rate Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.064" x .056"
THICKNESS:	0.0065 ± 0.0020"
PAD DIMENSIONS:	.004" x .004"

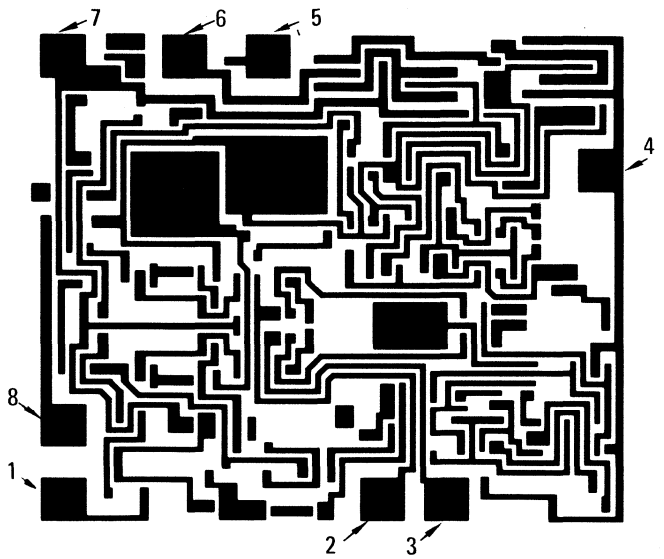
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Bandwidth Control

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V
Differential Input Voltage	±15.0V
Peak Output Current	±50mA
Operating Die Temperature	-55°C to +125°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		8	mV
Bias Current		250	nA
Offset Current		50	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	15K		V/V
Common Mode Rejection Ratio	74		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		6	mA
Power Supply Rejection Ratio	74		dB

NOTE: Consult HA-2505 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

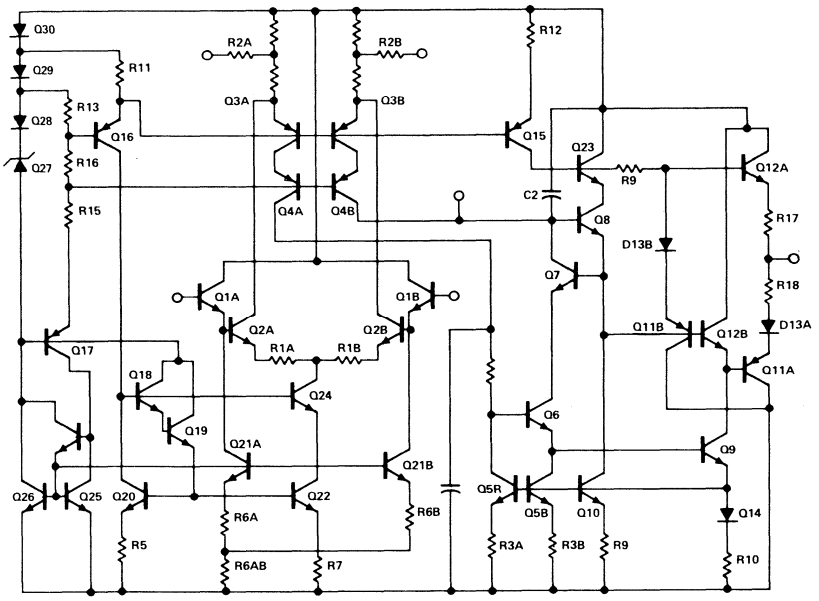
CF-2515

High Slew Rate Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.064" x .056"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004"

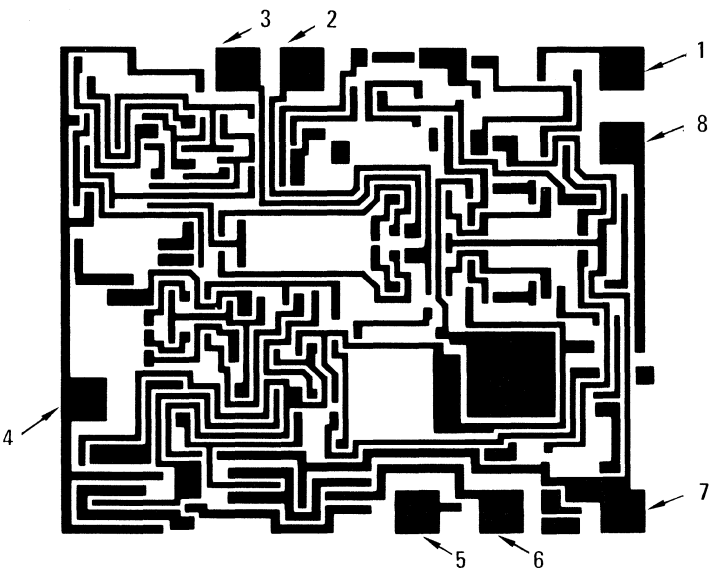
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Bandwidth Control

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V
Differential Input Voltage	±15.0V
Peak Output Current	±50mA
Operating Die Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		10	mV
Bias Current		250	nA
Offset Current		50	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	7.5K		V/V
Common Mode Rejection Ratio	74		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		6	mA
Power Supply Rejection Ratio	74		dB

NOTE: Consult HA-2515 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

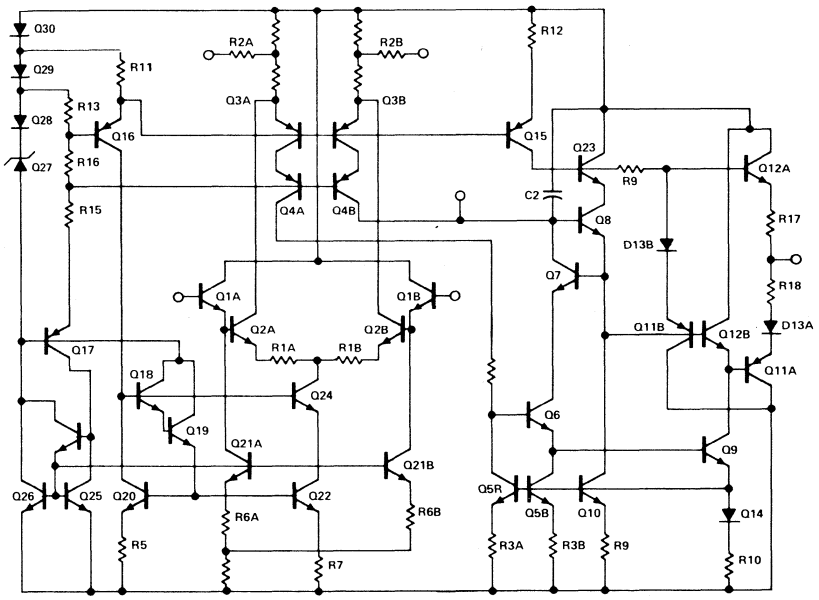
CF-2525

High Slew Rate Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.064" x .049"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004"

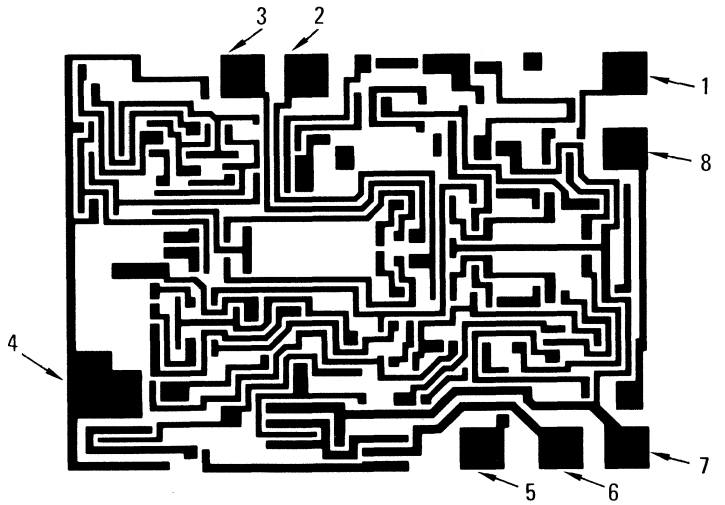
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Bandwidth Control

MASK PATTERN



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V
Differential Input Voltage	±15.0V
Peak Output Current	±50mA
Operating Die Temperature	-55^oC to $+125^oC$
Storage Temperature	-65^oC to $+150^oC$

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at $+25^oC$

$V^+ = +15$ V.D.C. $V^- = -15$ V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		10	mV
Bias Current		250	nA
Offset Current		50	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	7.5K		V/V
Common Mode Rejection Ratio	74		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		6	mA
Power Supply Rejection Ratio	74		dB

NOTE: Consult HA-2525 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

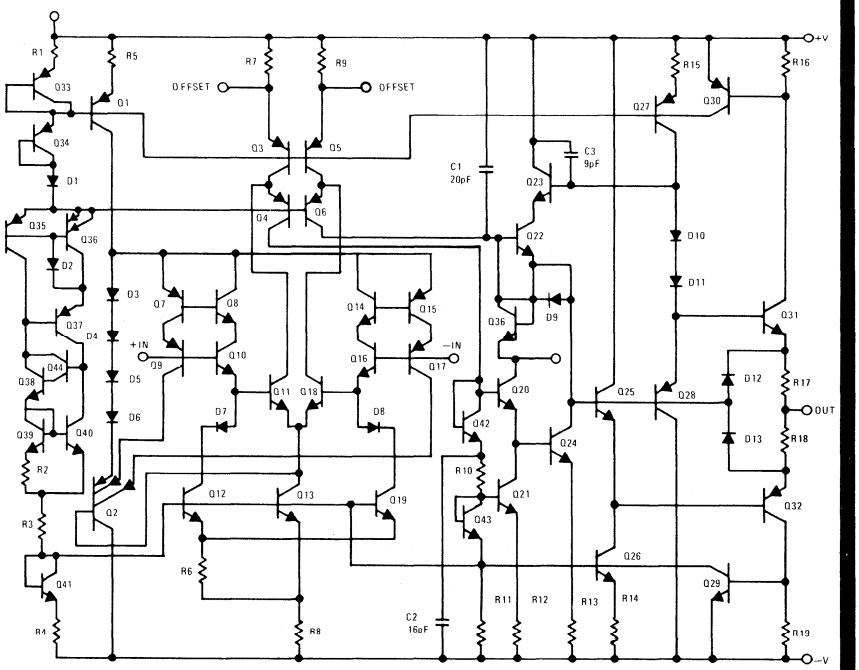
CF-2605

High Input Impedance Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.072" x .051"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

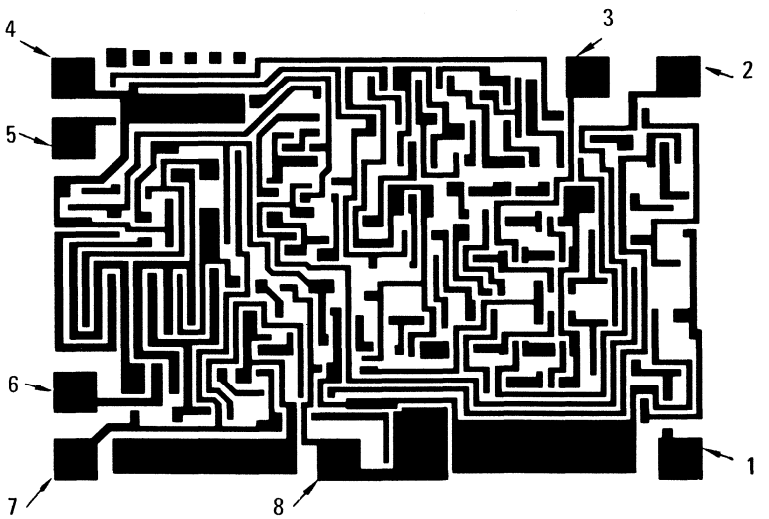
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Bandwidth Control

MASK PATTERN



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	-55^oC to $+125^oC$
Storage Temperature	-65^oC to $+150^oC$

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at $+25^oC$

$V^+ = +15$ V.D.C. $V^- = -15$ V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		5	mV
Bias Current		25	nA
Offset Current		25	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	80K		V/V
Common Mode Rejection Ratio	74		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		4	mA
Power Supply Rejection Ratio	74		dB

NOTE: Consult HA-2605 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

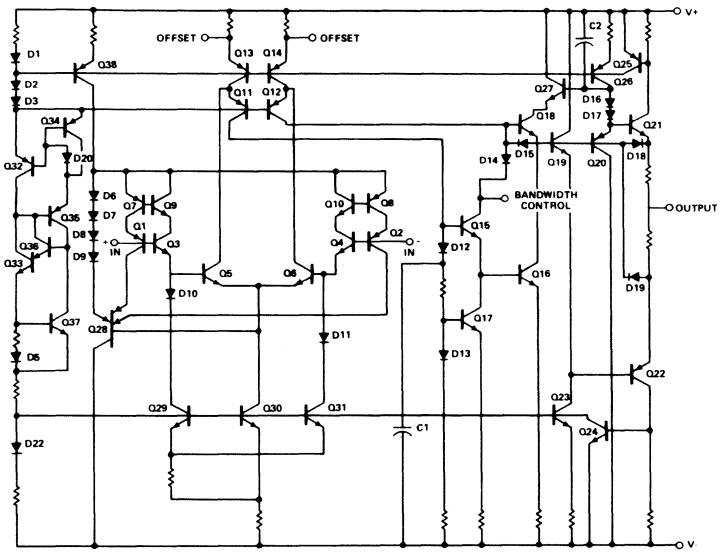
CF-2625

Wide Band Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.072" x.051"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004" Min.

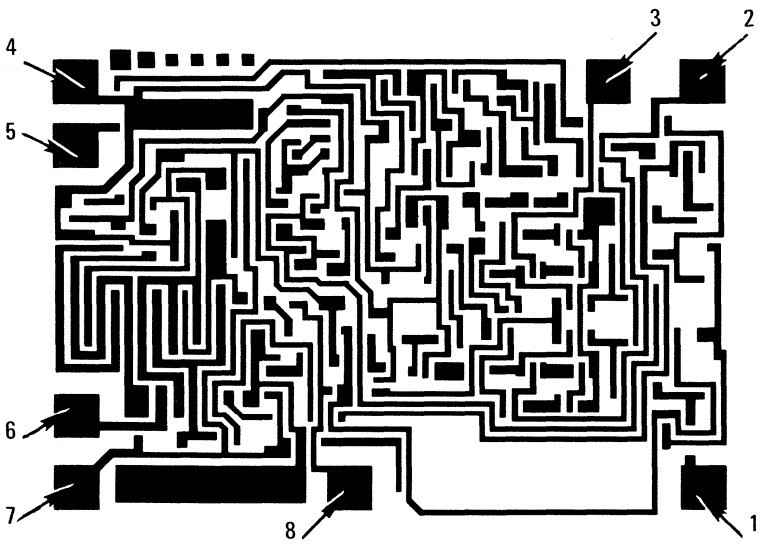
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	Offset Null
6	Output
7	V^+
8	Bandwidth Control

MASK PATTERN



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	-55°C to +125°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		5	mV
Bias Current		25	nA
Offset Current		25	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	80K		V/V
Common Mode Rejection Ratio	74		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±10		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		4	mA
Power Supply Rejection Ratio	74		dB

NOTE: Consult HA-2625 data sheet for typical performance characteristics.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

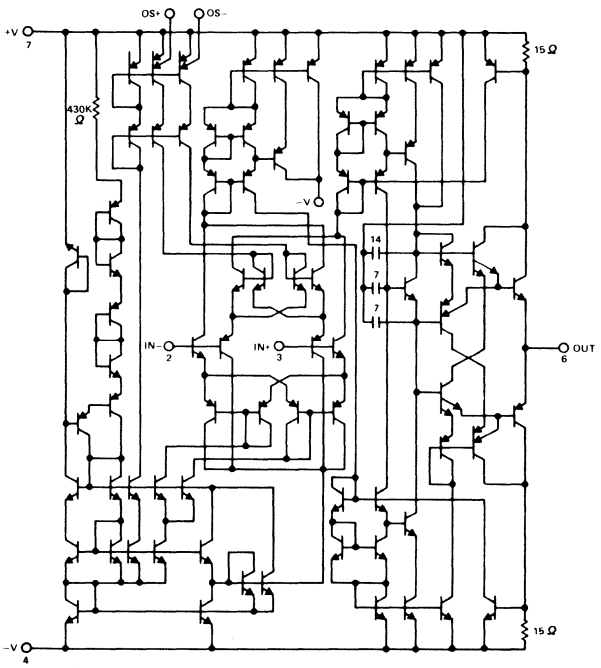
CF-2705

High Performance Operational Amplifier Monolithic Chip

DIE PHYSICAL CHARACTERISTICS

DIE SIZE:	.058" x .068"
THICKNESS:	0.0065" ± 0.0020"
PAD DIMENSIONS:	.004" x .004"

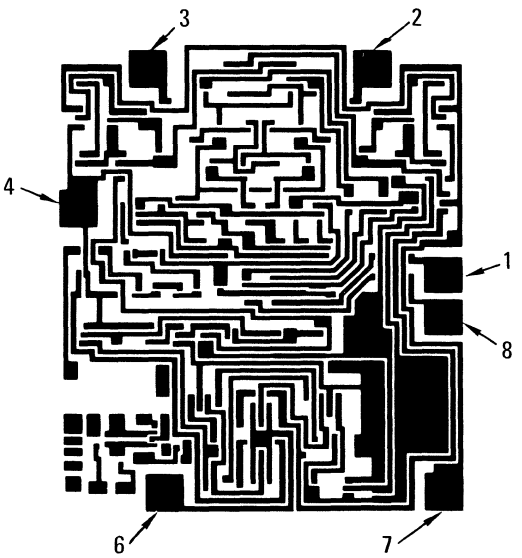
SCHEMATIC DIAGRAM



PAD SEQUENCE

PAD NO.	FUNCTION
1	Offset Null
2	Inverting Input
3	Non-Inverting Input
4	V^-
5	NC
6	Output
7	V^+
8	Offset Null

MASK PATTERN



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±18.0V
Peak Output Current	Full Short Circuit Protection
Operating Die Temperature	−55°C to +150°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Guaranteed Probe Limits at +25°C

V^+ = +15 V.D.C. V^- = −15 V.D.C.

PARAMETER	LIMITS		UNITS
	MINIMUM	MAXIMUM	
INPUT CHARACTERISTICS			
Offset Voltage		5	mV
Bias Current		40	nA
Offset Current		15	nA
TRANSFER CHARACTERISTICS			
Large Signal Voltage Gain	200K		V/V
Common Mode Rejection Ratio	80		dB
OUTPUT CHARACTERISTICS			
Output Voltage Swing (R_L = 2KΩ)	±12		V
POWER SUPPLY CHARACTERISTICS			
Supply Current		150	μA
Power Supply Rejection Ratio	80		dB

NOTE: Consult HA-2705 data sheet for typical performance characteristics.

Digital

Data Sheets

Application Notes

DIGITAL DATA SHEETS

HD-0140/HD-0140A	Four-Bit Latch/Seven Segment Decoder/Driver
HD-0165	Keyboard Encoder
HD-245/545	Triple Line Transmitter
HD-246/546/249/549	Triple Line Receivers
HD-248/548	Triple Party Line Receivers
HD-1488	Quad Line Driver
HD-1489	Quad Line Receiver
HD-1489A	Quad Line Receiver
HT-6500/6501/6502	New Quad Core Drivers

LOGIC INTERFACE CIRCUITS

DI/CMOS

HD-4000	Dual 3-Input 'NOR' Gate Plus Inverter
HD-4001	Quad 2-Input 'NOR' Gate
HD-4009	Hex Inverter/Buffer
HD-4010	Hex Buffer
HD-4011	Quad 2-Input 'NAND' Gate
HD-4012	Dual 4-Input 'NAND' Gate
HD-4013	Dual 'D' Flip Flop
HD-4809	Triple True/Complement Buffer

DIGITAL APPLICATION NOTES

NOTE 204	Designing with the HD-0165 Keyboard Encoder
NOTE 205	High Speed Digital Communications
NOTE 207	Receiver/Transmitter Noise Immunity

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-0140/HD-0140A

Four-Bit Latch/Seven Segment Decoder/Driver

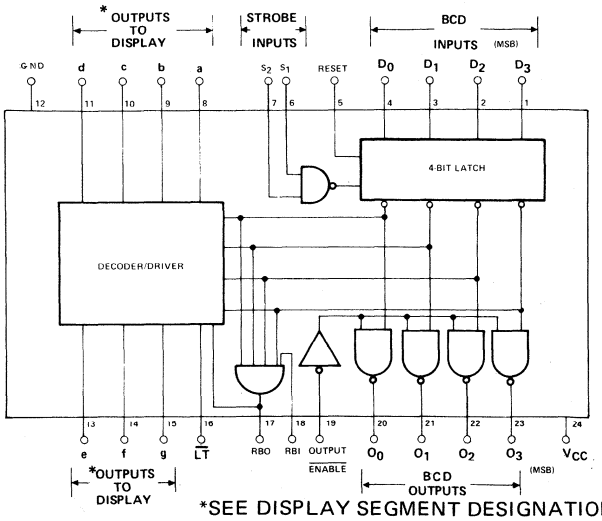
FEATURES

- DRIVES LED INCANDESCENT DISPLAYS
- STORES AND SHIFTS BCD DATA
- 40 mA DISPLAY DRIVE CAPABILITY
- EDGE TRIGGERED LATCH WITH GATED STROBE
- LAMP TEST PROVISIONS
- ZERO BLANKING PROVISIONS
- DISPLAY VOLTAGES UP TO 20V
- GATED BCD PUTPUTS

GENERAL DESCRIPTION

The HD-0140/HD-0140A consists of a four-bit edge-triggered latch, a seven segment decoder and seven display drivers. The four-bit latch is loaded on the falling edge of either strobe while the other strobe is high. The BCD output is available when the output $\overline{\text{ENABLE}}$ is low. The BCD outputs of the HD-0140 have internal 2KΩ pull up resistors while the HD-0140A BCD outputs are open collector. A low input on the $\overline{\text{LAMP TEST}}$ will turn on all seven display drivers. A high on the Ripple Blanking Input (Zero Blanking) will turn off the display drivers and produce a high on the Ripple Blanking Output if the latch contains a "Zero". A high on the RESET will reset the latch to a BCD zero. An "F" will be displayed if the latch contains a binary number greater than 9.

BLOCK DIAGRAM



*SEE DISPLAY SEGMENT DESIGNATION

TRUTH TABLE

BINARY INPUT D_3	D_2	D_1	D_0	CHARACTER DISPLAYED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	F
1	0	1	1	F
1	1	0	0	F
1	1	0	1	F
1	1	1	0	F
1	1	1	1	F

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

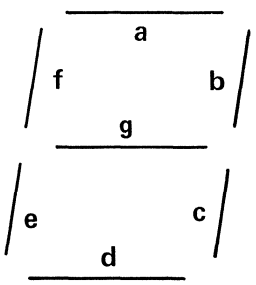
Power Supply Voltage, V_{CC}	7.0V
Display Driver Voltage	20.0V
Power Dissipation at 75°C T_A	1 W
Derate by 15 mW/°C Above 75°C T_A	

ELECTRICAL CHARACTERISTICS

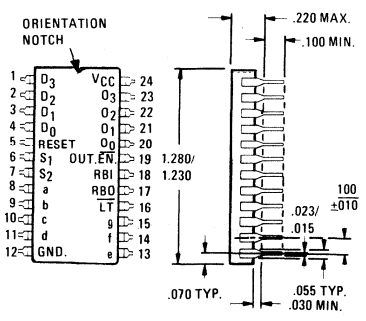
Test Conditions - unless otherwise specified: V_{CC} = 5.0V ±5%
T_C = -55°C to +125°C HD-0140-2, HD-0140A-2
T_A = 0°C to +75°C HD-0140-5, HD-0140A-5

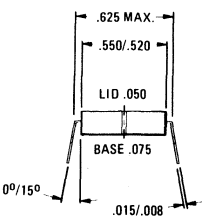
	PARAMETER	SYM	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
D.C.	INPUT CURRENT						
	Input High	I_{IH}			40	µA	V_{IH} = 2.4V, V_{CC} = 5.25V
	Input Low	I_{IL}			-1.0	mA	V_{IL} = 0.4V, V_{CC} = 5.25V
	INPUT THRESHOLD						
	Input High	V_{IH}	2.0			V	
	Input Low	V_{IL}			0.8	V	
	SEGMENT DRIVER						
	Output Leakage	I_{OH}			100	µA	V_{OH} = 20.0V
	Output Low Voltage	V_{OL}		0.2	0.4	V	I_{OL} = 20mA
		V_{OL}		0.4	0.6	V	I_{OL} = 40mA
	BCD OUTPUTS						
	Output High Voltage - HD-0140	V_{OH}	2.4			V	I_{OH} =-400µA, V_{CC} = 4.75V
	Output High Leakage - HD-0140A	I_{OH}			100	µA	V_{OH} = 2.4V
	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10mA
	RIPPLE BLANKING						
	Output High Voltage	V_{OH}	2.4			V	I_{OH} =-400µA, V_{CC} = 4.75V
	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.8mA
	Supply Current	I_{CC}		60	100	mA	V_{CC} = 5.25V
A.C.	STROBE TO OUTPUT	t_{pd+}		150		ns	T_A = +25°C
		t_{pd-}		50		ns	
	Output Enable to Output	t_{pd+}		35		ns	V_{CC} = 5.0V
		t_{pd-}		25		ns	

DISPLAY SEGMENT DESIGNATION



PACKAGE





24 LEAD DUAL IN LINE PACKAGE
HERMETIC
ALL DIMENSIONS IN INCHES

DIGITAL DATA

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-0165

Keyboard Encoder

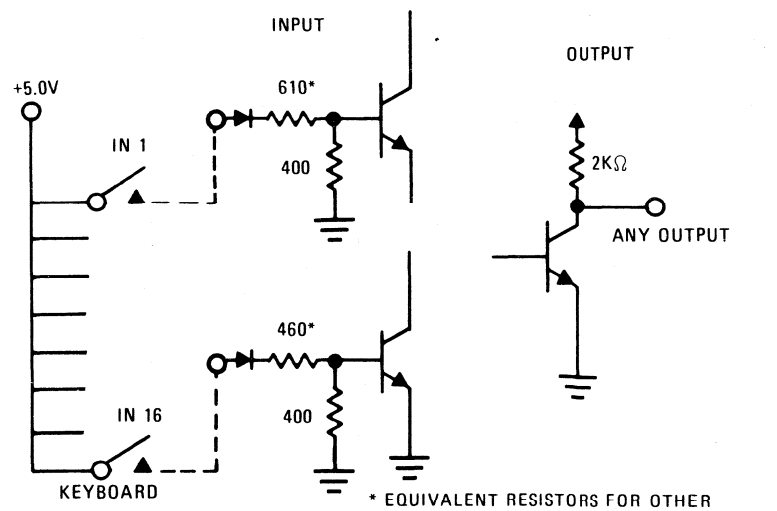
FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED, DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

GENERAL DESCRIPTION

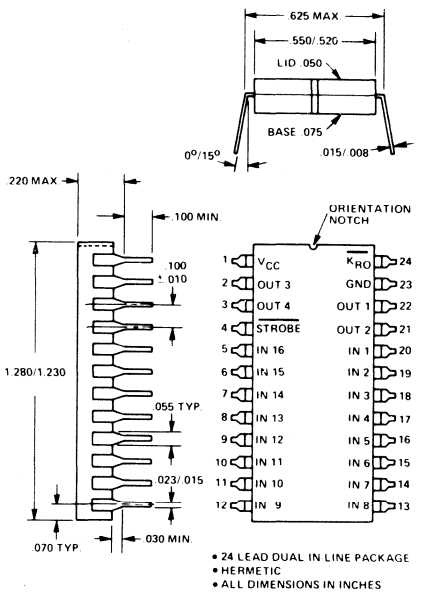
The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual in-line package and operates over the temperature range of $0^{o}C$ to $+75^{o}C$.

EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

PACKAGE



- 24 LEAD DUAL IN LINE PACKAGE
- HERMETIC
- ALL DIMENSIONS IN INCHES

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^{o} to $+150^{o}C$
Output Voltage	+5.5V	Operating Temperature (Case)	$0^{o}C$ to $+75^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^{o}C$ to $+75^{o}C$
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current "1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
D.C.	Output Voltage "0"	V_{OL}			+0.4	V	$V_{IH} = +3.5V$ $I_{OL} = 3.2mA$
D.C.	Output Voltage "1"	V_{OH}	+2.4	+4.0		V	V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
D.C.	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
D.C.	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	$T_{Case} = 25^{o}C$, $V_{CC} = V_{IN} = +5.0V$, $C_L < 50pF$

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including $\overline{\text{strobe}}$ and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

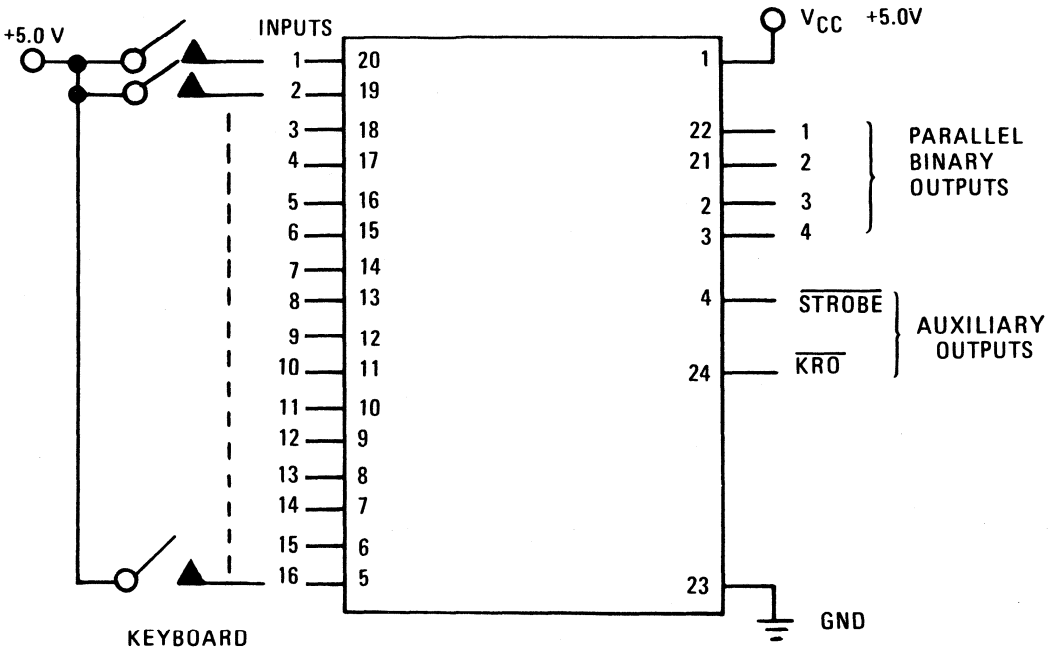


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

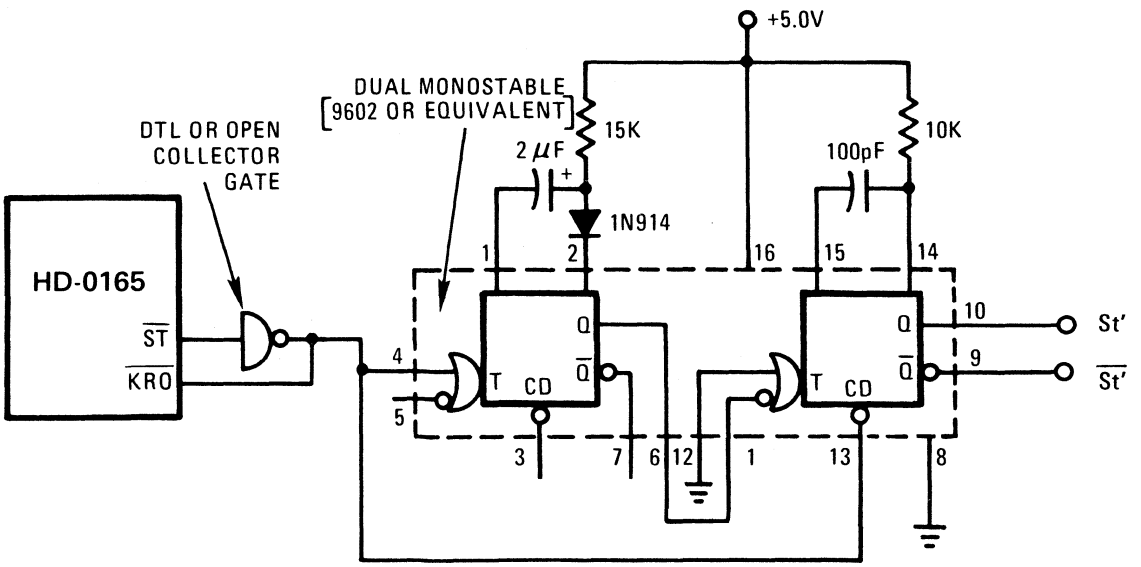


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (St'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions.

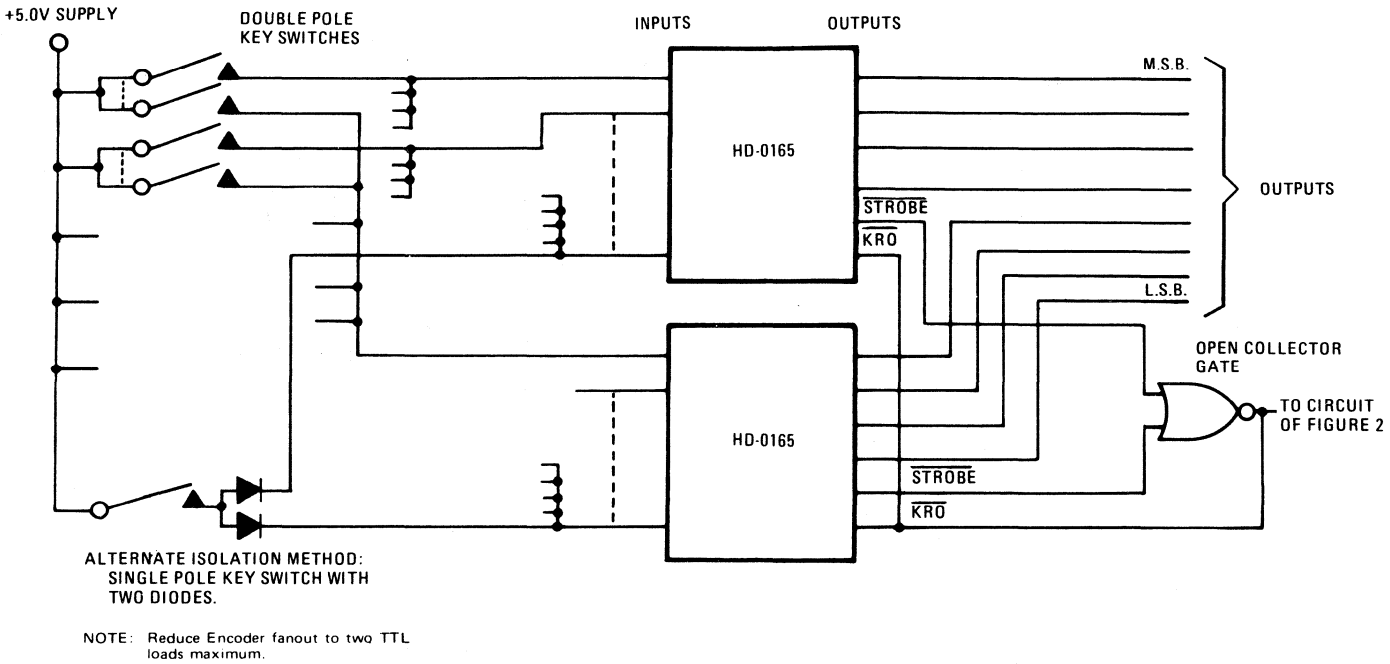


Figure 3. ENCODING UP TO 256 KEYS

Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-245/545 *Triple Line Transmitter*

HD-246/546/249/549 *Triple Line Receivers*

HD-248/548 *Triple Party Line Receiver*

FEATURES:

- CURRENT MODE OPERATION
- HIGH SPEED: 15MHz WITH 50FT. CABLE; 2MHz WITH 1,000FT. CABLE
- HIGH NOISE IMMUNITY
- LOW EMI GENERATION
- LOW POWER DISSIPATION
- HIGH COMMON MODE REJECTION
- TRANSMITTER AND RECEIVER PARTY LINE CAPABILITY
- TOLERATES -2.0V TO +20.0V GROUND DIFFERENTIAL (Transmitter with respect to receiver)
- TRANSMITTER INPUT/RECEIVER OUTPUT TTL/DTL COMPATIBLE

GENERAL DESCRIPTION

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monolithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off", allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the following table:

	INPUT	OUTPUT
HD-246 / 546	100 Ω	OPEN COLLECTOR
HD-248 / 548	HI-Z	6K PULL-UP RES.
HD-249 / 549	100 Ω	6K PULL-UP RES.

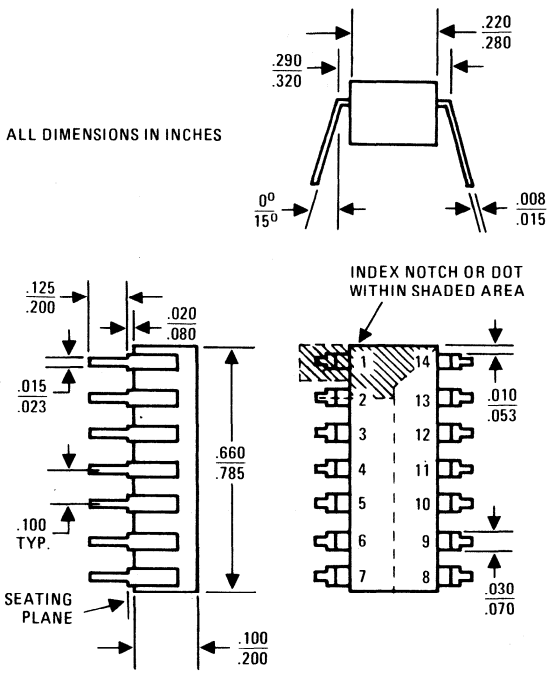
The internal 100 Ω cable termination consists of 50 Ω from each input to ground.

HD-248/548 "party line" receivers have a high-Z input such that as many as ten of these receivers can be used on a single transmission line.

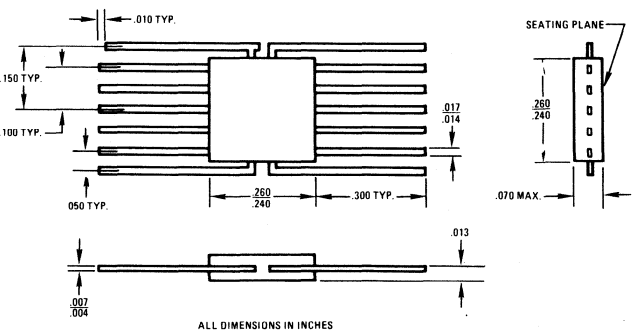
Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitive and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of -2.0 V to +20.0V (transmitter with respect to receiver).

PACKAGES

DUAL INLINE



TO - 86 FLAT - PAK



SPECIFICATIONS HD-245/545 TRANSMITTERS

ABSOLUTE MAXIMUM RATINGS

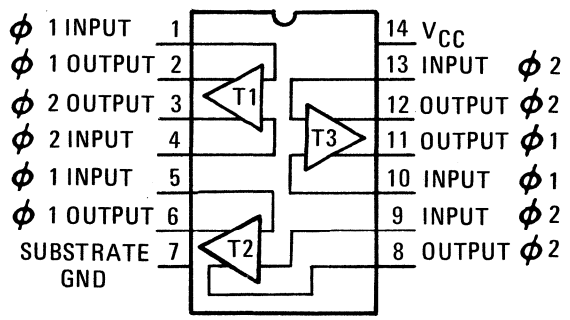
Input Voltage Range: -0.5V to +10V
Output Voltage Range: -30V to +0.5V with respect to V_{CC}
V_{CC} Range: -0.5V to +10V
Storage Temperature Range: -65°C to +150°C

ELECTRICAL CHARACTERISTICS

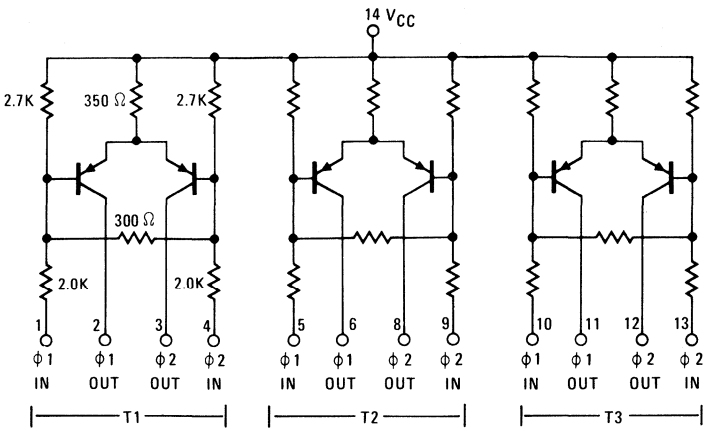
	PARAMETER	SYMBOL	TEMP.	HD-245 -55°C to +125°C MIN.	HD-245 TYP.	HD-245 MAX.	HD-545 0°C to +75°C MIN.	HD-545 TYP.	HD-545 MAX.	UNITS	TEST CONDITION V_{CC}	TEST CONDITION NOTES
DC	INPUT LOW CURRENT	I_{IL}	25°C Full		-1.5	-2.2 -2.5		-1.5	-2.3 -2.4	mA	5.5	1
DC	"ON" OUTPUT CURRENT	I_{OUT} "ON"	25°C Full Full	-2.3 -2.0 -1.6			-1.9 -1.8 -1.5			mA mA mA	4.5 4.5 4.5	1 1 2
DC			25°C Full		-4.1	-5.4 -5.6		-4.1	-6.3 -6.7	mA	5.5	1
DC	"ON" OUTPUT CURRENT UNBALANCE	ΔI_{OUT}	25°C Full		0.1	0.25 0.3		0.1	0.25 0.3	mA	5.5	3
DC	"OFF" OUTPUT CURRENT	I_{OUT} "OFF"	25°C Full		-30	-100 -100		-30	-100 -100	μA	4.5	1
DC	OUTPUT BREAKDOWN	BV_{CER}	25°C	-30	-50		-30	-50		V	GND	4
DC	POWER SUPPLY CURRENT-TOTAL		25°C 25°C		15	18.6 0.6		15	24 0.6	mA	5.0	5 6
AC	PROPAGATION DELAY	t_{PLH}	25°C Full		3	10 14		3	10 14	ns	5.0	
AC	TEST CIRCUIT 1, PAGE 4	t_{PHL}	25°C Full		3.2	10 14		3.2	10 14	ns	5.0	

NOTES:
1. One input at Gnd. one input open, each output at Gnd.
2. One input at 0.8V, one input open, each output at Gnd.
3. Difference between $\phi 1$ and $\phi 2$ "ON" output data current.
4. Each input at Gnd, one output at Gnd, $I_{Limit} \geq 100\mu A$ on output tested with -30V applied.
5. One input of each transmitter at Gnd and the other input open. All six output lines at Gnd.
6. All six input lines open, all six output lines at Gnd.

BLOCK DIAGRAM



SCHEMATIC



DIGITAL DATA

SPECIFICATIONS HD-246/546; HD-248/548; HD-249/549 RECEIVERS

ABSOLUTE MAXIMUM RATINGS

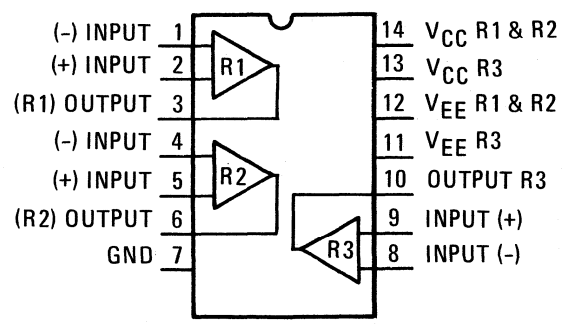
Input Voltage Range	-1.0V to +1.0V	Input Current	±25mA
Output Voltage Range	-0.5V to +6.0V	Output Current	+50mA
V_{CC} Range	-0.5V to +8.0V	Storage Temperature	-65°C to +150°C
V_{EE} Range	-8.0V to +0.5V		

ELECTRICAL CHARACTERISTICS

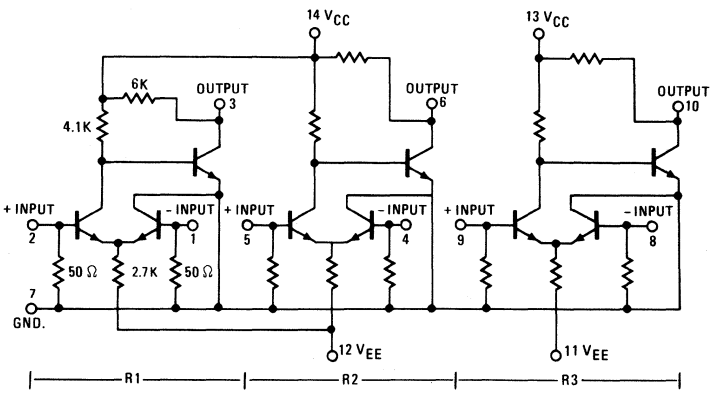
	PARAMETER	SYM.	TEMP.	HD-246 / 248 / 249 -55°C to +125°C MIN.	TYP.	MAX	HD-546 / 548 / 549 0°C to +75°C MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS V_{EE} = -5V V_{CC}	NOTES
	INPUT RESISTANCE (HD-246/546 & HD-249/549	R_{IN}	+25°C Full	40 39	47	61 68	35 33	47	65 70	Ohms		
	PULL-UP RESISTOR (HD-248/548 & HD-249/549)		+25°C Full	4.2 4.1	6	7.8 8.6	4.0 3.9	6	8.1 8.6	K Ohms		
DC	OUTPUT VOLTAGE (HIGH)	V_{OH}	+25°C Full	2.6 2.5			2.6 2.5			V	4.5	Note 1 I_{OH}=-120μA Ext. 6K Res. For HD-246/546
	OUTPUT VOLTAGE (LOW)	V_{OL}	+25°C Full			0.45 0.45			0.45 0.45	V	4.5	Note 2 I_{OL}=9.6mA 10mA For HD-246/546
	OUTPUT VOLTAGE (LOW) (INPUT SHORT CIRCUIT)	V_{OLSC}	+25°C		0.4			0.4		V	5.0	Note 3 I_{OL} = 3.2mA
	HD-246 / 546 POWER SUPPLY CURRENT (TOTAL)	I_{CC} I_{EE}	+25°C		3.3 5.1	4.8 6.0		3.3 5.1	5.7 6.3	mA	5.0	Note 4
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.0		3.9 5.1	7.5 6.3	mA	5.0	Note 5
	HD-248 / 548 & HD-249 / 549	I_{CC} I_{EE}	+25°C		6.3 5.1	7.8 6.0		6.3 5.1	8.7 6.3	mA	5.0	Note 4
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.0		3.9 5.1	7.5 6.3	mA	5.0	Note 5
	PROPAGATION DELAY	t_{PLH}	+25°C Full		18	30 30		18	30 30	ns	5.0	
AC	TEST CIRCUIT 2 PAGE 4	t_{PHL}	+25°C Full		25	30 30		25	30 30	ns	5.0	

NOTES:
1. (+) I_{IN} = 1.5mA; (–) Input = open (For HD-248/548; Ext. 50Ω Res. or 75mV).
2. (+) Input = open; (–) I_{IN} = 1.5mA. (For HD-248/548; Ext. 50Ω Res. or 75mV)
3. Both inputs shorted to Gnd; or both inputs open such that 50Ω termination resistors are in the circuit.
4. (+) Input = open; (–) I_{IN} = 3mA.
5. (+) I_{IN} = 3mA; (–) Input = open.

BLOCK DIAGRAM



SCHEMATIC

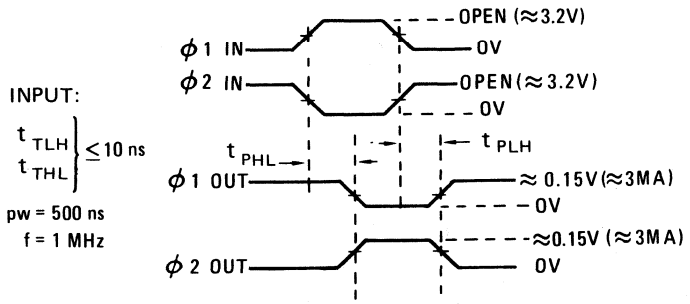


NOTES:
1. HD- 249/549 is as shown
2. HD- 246/546 does not have 6K output pull- up resistors.
3. HD- 248/548 does not have 50 Ω input termination resistors.
4. Resistor values are nominal

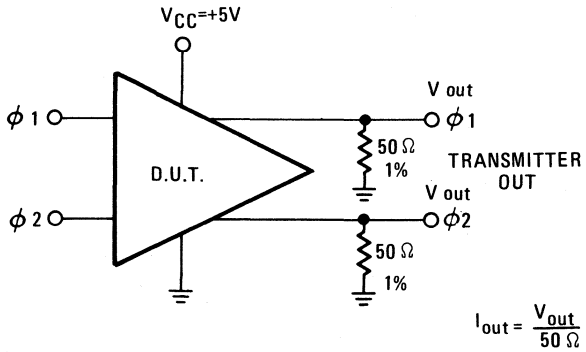
DIGITAL DATA

TEST CIRCUITS

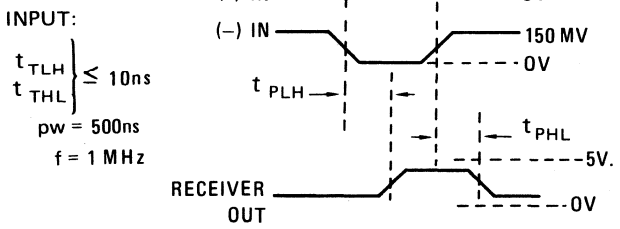
TEST CIRCUIT 1 - TRANSMITTER PROPAGATION DELAY



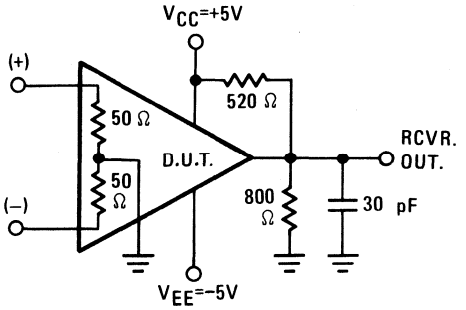
All measurements referenced to 50 % V points



TEST CIRCUIT 2 - RECEIVER PROPAGATION DELAY



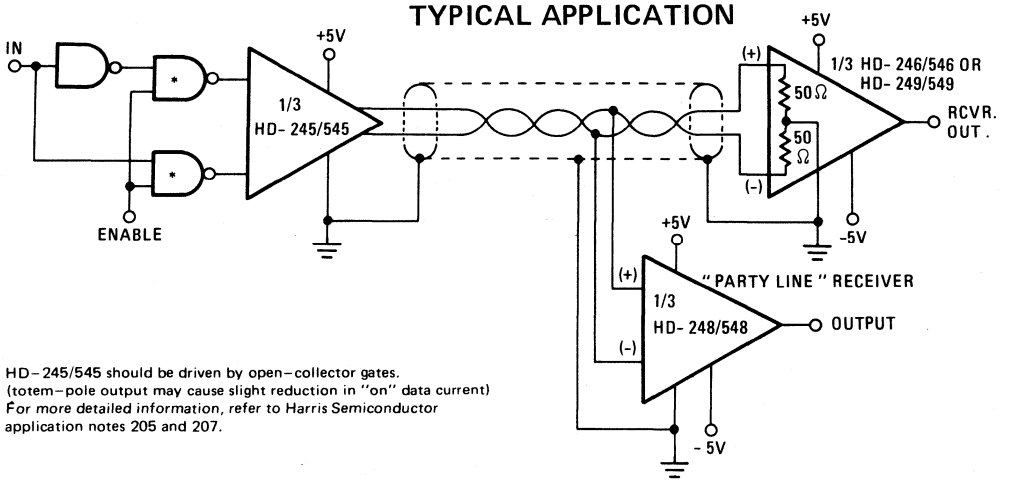
All measurements referenced to 50%V points.



NOTE: External 50Ω resistors needed for HD–248/548.

APPLICATIONS

TYPICAL APPLICATION



* HD–245/545 should be driven by open–collector gates. (totem–pole output may cause slight reduction in "on" data current) For more detailed information, refer to Harris Semiconductor application notes 205 and 207.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-1488

Quad Line Driver

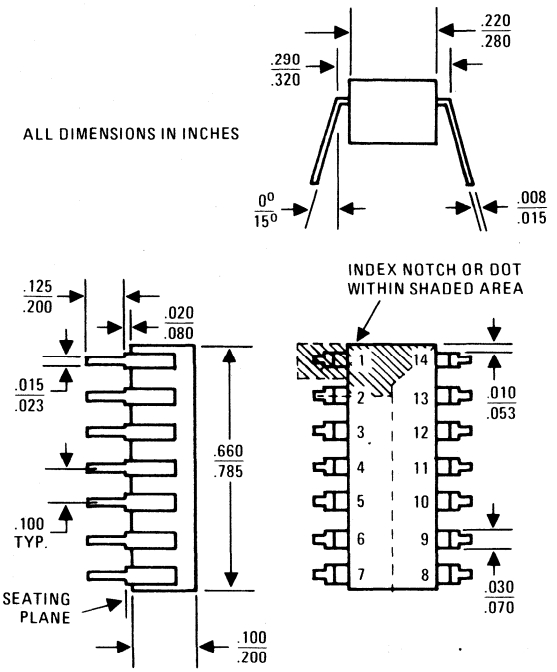
FEATURES

- ±6.0V OUTPUT LEVELS
- SHORT CIRCUIT PROTECTED
- USEFUL AS LOGIC LEVEL SHIFTER
- MONOLITHIC RELIABILITY

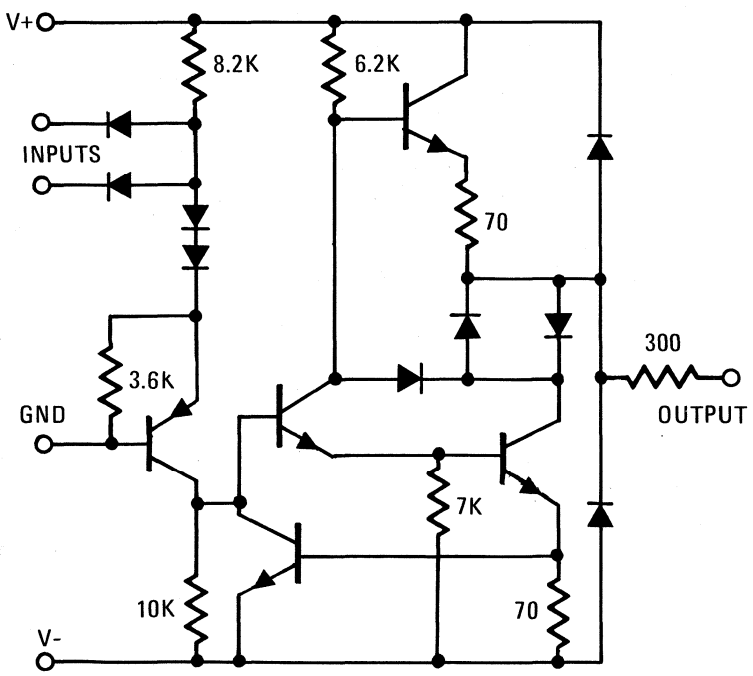
DESCRIPTION

The Harris HD-1488 is a quadruple line driver monolithic integrated circuit meeting the electrical requirements of EIA standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The driver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit inputs can be driven from any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line receiver circuit is the Harris HD-1489.

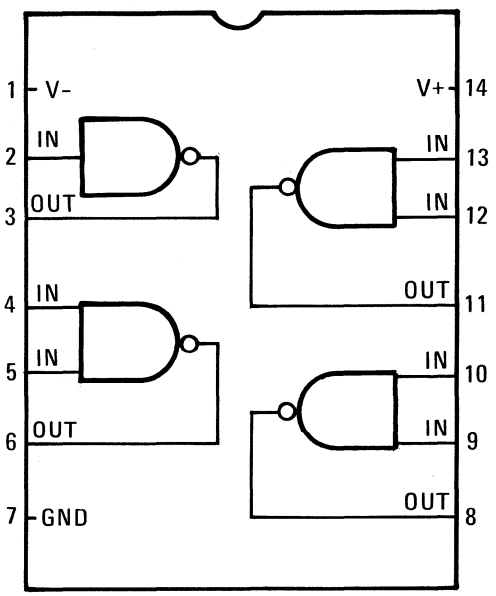
PACKAGE



SCHEMATIC



CONNECTION DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+, V- at +25°C ±15.0V
Derate by 35mV/°C

Input Voltage $V- \leq V_{IN} \leq 7.0V$

Output Voltage $V_{OUT} \geq V+ +5V$, $\leq V- -5V$

Storage Temperature -65°C to +150°C

Operating Temperature, T_A 0°C to +75°C

Power Dissipation at +25°C 1000mW
Derate by 6.7mW/°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = +9.0V, V- = -9.0V, T_A = 0°C to +75°C unless otherwise specified.

	PARAMETER		SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current	"0"	I_F		1.0	1.3	mA	V_{IN} = 0.0V
		"1"	I_R			10	µA	V_{IN} = +5.0V
	Output Voltage	"0"	V_{OL}	-6.0	-7.0		V	V_{IN} = +1.9V, R_L = 3K
		"1"	V_{OH}	+6.0	+7.0			V_{IN} = +0.8V, R_L = 3K
	Output Short Circuit Current		I_{SC+}	+6	+10	+12	mA	V_{IN} = 0.0V to +0.8V
			I_{SC-}	-6	-10	-12		V_{IN} = +1.9V to +5.0V
	Output Resistance		R_O	300			Ohms	V+ = V- = 0.0V, V_O = ±2.0V
	Supply Current		I+		+15	+20	mA	V+ = +9.0V
			I-		-13	-17		V- = -9.0V
			I+		+19	+25	mA	V+ = +12.0V
			I-		-18	-23		V- = -12.0V
	Power Dissipation		P_D			333	mW	V+ = +9.0V, V- = -9.0V
			P_D			576		V+ = +12.0V, V- = -12.0V
A.C.	Propagation Delay		T_{PD+}		250	300	ns	R_L = 3KΩ
			T_{PD-}		30	120		
	Rise Time (Note 1)		T_r		50	100	ns	C_L = 15pF
	Fall Time (Note 1)		T_f		25	75	ns	T_A = +25°C

NOTES: 1. To maintain a maximum rate of voltage change of 30V/µs, the load capacitance, including transmission line, should be at least 330pF.

DIGITAL DATA

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-1489

Quad Line Receiver

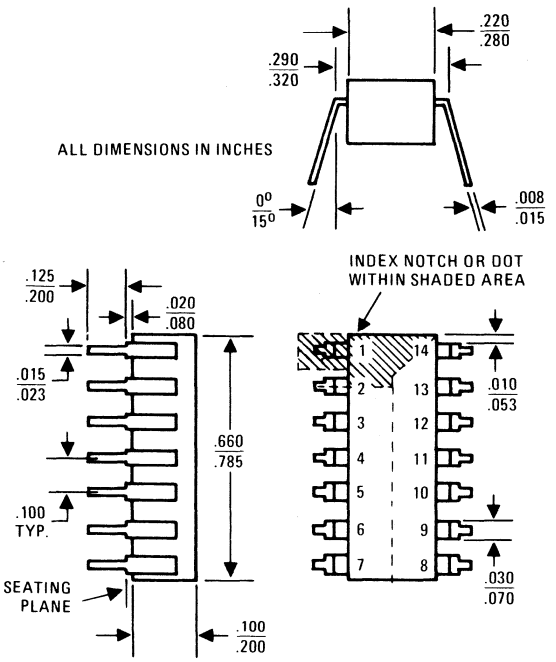
FEATURES

- INPUT LEVEL HYSTERESIS
- INPUTS WITHSTAND ±30.0V
- PROVISION FOR THRESHOLD ADJUSTMENT OR NOISE FILTERING
- MONOLITHIC RELIABILITY

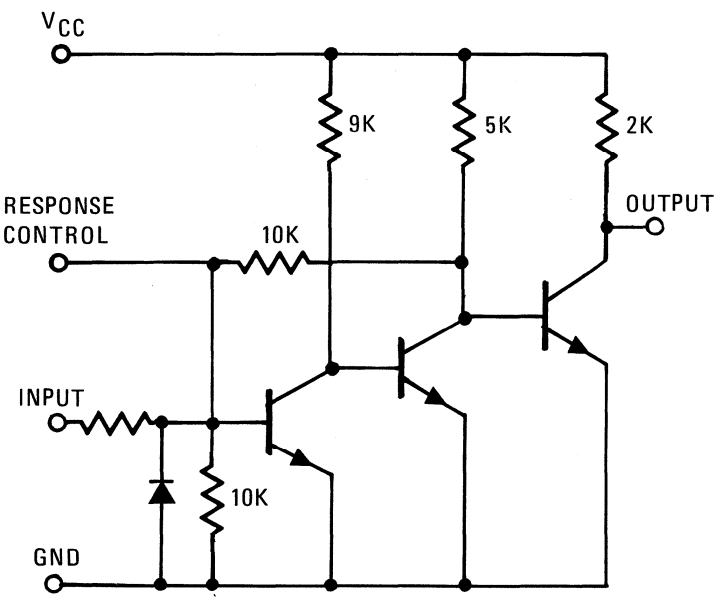
GENERAL DESCRIPTION

The Harris HD-1489 is a quadruple line receiver monolithic integrated circuit meeting the electrical requirements of EIA Standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The receiver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit outputs can drive any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line driver circuit is the Harris HD-1488.

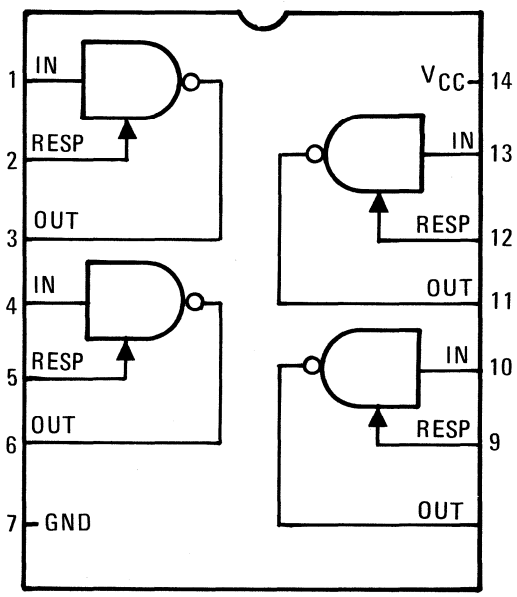
PACKAGE



SCHEMATIC



CONNECTION DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10.0V	Storage Temperature	-65°C to +150°C
Input Voltage	±30.0V	Operating Temperature	0°C to +75°C
Output Current	20mA	Power Dissipation at +25°C	1000mW
		Derate by 5mW/°C	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5.0V, T_A = 0°C to +75°C,
Response control pin open unless otherwise specified.

	PARAMETER		SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
D.C.	Input Current	"0"	I_{IL}	-.43			mA	V_{IN} = -3.0V	
		"1"	I_{IH}	+.43				V_{IN} = +3.0V	
		"0"	I_{IL}	-3.6		-8.3	mA	V_{IN} = -25.0V	
		"1"	I_{IH}	+3.6		+8.3		V_{IN} = +25.0V	
	Input Threshold Voltage (Note 1)	"0"	V_{IL}	0.75		1.25	V	$V_{OH} \geq$ 2.5V, $V_{OL} \leq$ .45V	T_A = +25°C
		"1"	V_{IH}	1.0		1.5			
	Output Voltage (Note 2)	"0"	V_{OL}		0.2	0.45	V	V_{IN} = +1.5V, I_{OL} = 10mA	
		"1"	V_{OH}	2.6	4.0	5.0		V_{IN} = +0.75V, I_{OH} = -0.5mA	
		"1"	V_{OH}	2.6	4.0	5.0		V_{IN} = Open, I_{OH} = -0.5mA	
	Output Short Circuit Current		I_{SC}		3.0		mA	V_{IN} = +0.75V	
	Supply Current		I_{CC}		20	26	mA	V_{CC} = +5.0V	
	Power Dissipation		P_D		100	130	mW	V_{CC} = +5.0V	
A.C.	Propagation Delay		T_{PD+}		60	85	ns	R_L = 3.9KΩ	T_A = +25°C
			T_{PD-}		25	50		R_L = 390Ω	
	Rise Time		T_r		90	175	ns	R_L = 3.9KΩ	
	Fall Time		T_f		8.0	20		R_L = 390Ω	

NOTES:

(1) Hysteresis is typically 250mV to prevent output chatter as input signal passes through the threshold region. If desired, thresholds can be made more positive by connecting a resistor from the response control pin to a negative supply; or more negative by connecting the resistor to a positive supply. A capacitor up to 500pF may be connected from the response control pin to ground, making the circuit output less sensitive to narrow noise spikes.

(2) This assures that the output will be in the "1" state if the input line is open or shorted to ground.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-1489A

Quad Line Receiver

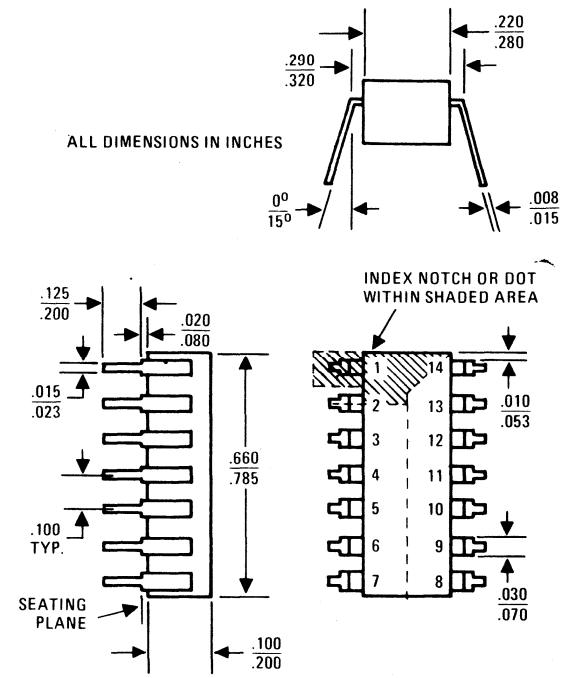
FEATURES

- INPUT HYSTERESIS 1.15V TYP.
- INPUTS WITHSTAND ±30.0V
- PROVISION FOR THRESHOLD ADJUSTMENT AND/OR NOISE FILTERING
- MONOLITHIC RELIABILITY

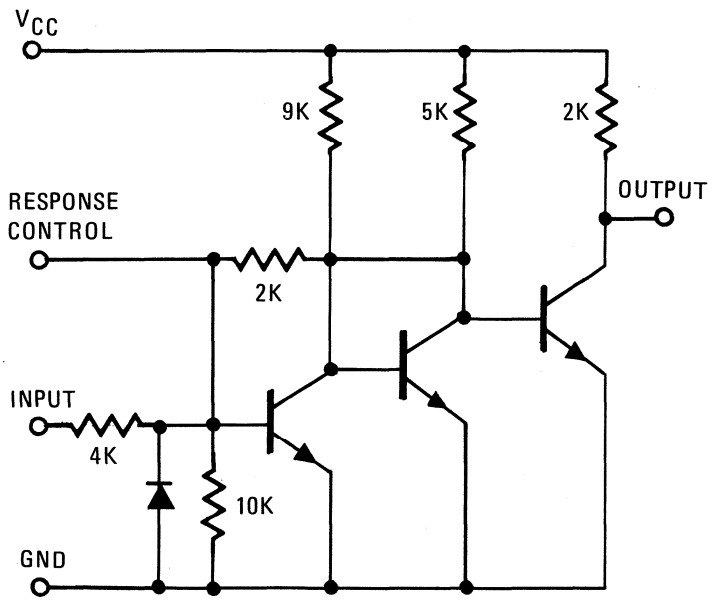
GENERAL DESCRIPTION

The Harris HD-1489A is a quadruple line receiver monolithic integrated circuit meeting the electrical requirements of EIA Standard RS-232-C for interface between data terminal equipment and data communication equipment. This standard assures electrical interface compatibility between data equipment made by different manufacturers. The receiver circuit is useful in any application requiring transfer of digital signals up to 20K bits per second using common-return signal lines over relatively short distances. The circuit outputs can drive any of the popular DTL or TTL logic families. It is available in a 14-pin hermetic dual in-line package for operation from 0°C to +75°C. The companion quad line driver circuit is the Harris HD-1488.

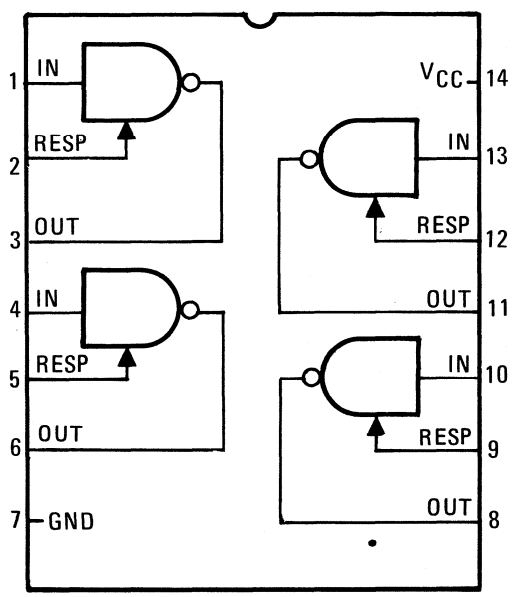
PACKAGE



SCHEMATIC



CONNECTION DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10.0V	Storage Temperature	-65°C to +150°C
Input Voltage	±30.0V	Operating Temperature	0°C to +75°C
Output Current	20mA	Power Dissipation at +25°C	1000mW
		Derate by 5mW /°C	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5.0V, T_A = 0°C to +75°C,
Response control pin open unless otherwise specified.

	PARAMETER		SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
D.C	Input Current	"0"	I_{IL}	-.43			mA	V_{IN} = -3.0V	
		"1"	I_{IH}	+.43				V_{IN} = +3.0V	
		"0"	I_{IL}	-3.6		-8.3	mA	V_{IN} = -25.0V	
		"1"	I_{IH}	+3.6		+8.3		V_{IN} = +25.0V	
	Input Threshold Voltage (Note 1)	"0"	V_{IL}	0.75		1.25	V	$V_{OH} \geq 2.5V$, $V_{OL} \leq .45V$	T_A = +25°C
		"1"	V_{IH}	1.75		2.25			
	Output Voltage (Note 2)	"0"	V_{OL}		0.2	0.45	V	V_{IN} = +1.5V, I_{OL} = 10mA	
		"1"	V_{OH}	2.6	4.0	5.0		V_{IN} = +0.75V, I_{OH} = -0.5mA	
		"1"	V_{OH}	2.6	4.0	5.0		V_{IN} = Open, I_{OH} = -0.5mA	
	Output Short Circuit Current		I_{SC}		3.0		mA	V_{IN} = +0.75V	
	Supply Current		I_{CC}		20	26	mA	V_{CC} = +5.0V	
	Power Dissipation		P_D		100	130	mW	V_{CC} = +5.0V	
A.C.	Propagation Delay		T_{PD+}		60	85	ns	R_L = 3.9KΩ	T_A = +25°C
			T_{PD-}		25	50		R_L = 390Ω	
	Rise Time		T_r		90	175	ns	R_L = 3.9KΩ	
	Fall Time		T_f		8.0	20		R_L = 390Ω	

NOTES:

(1) Hysteresis is typically 1.15V to prevent output chatter as input signal passes through the threshold region. If desired, thresholds can be made more positive by connecting a resistor from the response control pin to a negative supply; or more negative by connecting the resistor to a positive supply. A capacitor up to 500pF may be connected from the response control pin to ground, making the circuit output less sensitive to narrow noise spikes.

(2) This assures that the output will be in the "1" state if the input line is open or shorted to ground.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HT-6500/6501/6502

New Quad Core Drivers

FEATURES

- HIGH VOLTAGE — V_{CEO} up to 50V
- HIGH CURRENT — Up to 1.0 Amp
- FAST SWITCHING — 25ns, t_{on}; 45ns, t_{off}
- COMPACT — 4 Transistor/Chip

GENERAL DESCRIPTION

The HT-6500/HT-6501/HT-6502 consist of four high current NPN transistors on a single dielectrically isolated chip. These transistors are ideal for use as core drivers, relay drivers, and other applications requiring high current capability. These monolithic quad transistors are excellent for applications requiring transistors with matched parameters over temperature.

Ordering Information:

Military	HT 1-650X-2
Commercial	HT 1-650X-5
Chip	CF-650X-5

SPECIFICATIONS

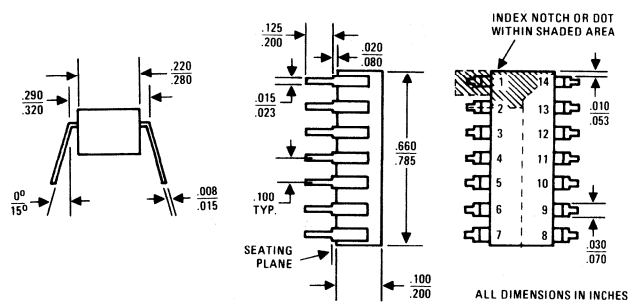
ELECTRICAL CHARACTERISTICS:

(25°C ambient temperature unless otherwise noted.)

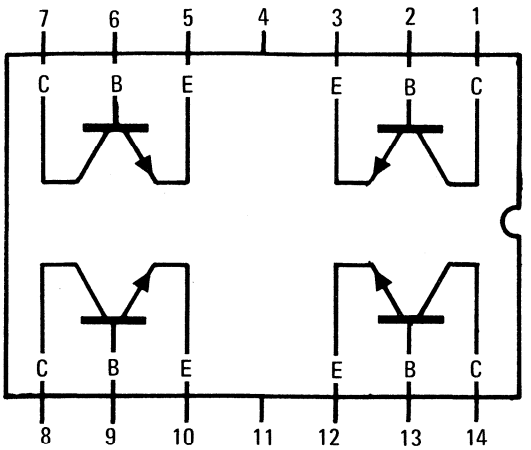
Operating Temperature (MAX) T_J = + 200°C
Power Dissipation (MAX) 1.5 Watts @ T_C = +25°C
0.8 Watts @ T_A = +25°C

	PARAMETER	SYM.	HT-6500 MIN.	HT-6500 TYP.	HT-6500 MAX.	HT-6501 MIN.	HT-6501 TYP.	HT-6501 MAX.	HT-6502 MIN.	HT-6502 TYP.	HT-6502 MAX.	UNITS	TEST CONDITIONS
DC	OFF CHARACTERISTICS												
	Collector-Emitter Breakdown Voltage	BV_{CEO}	50			40			20			V	I_C = 10mA, I_B = 0mA
	Collector Base Breakdown Voltage	BV_{CBO}	80			70			40			V	I_C = 10μA, I_E = 0μA
	Emitter-Base Breakdown Voltage	BV_{EBO}	6			6			6			V	I_E = 10μA, I_C = 0μA
	Collector Cutoff Current			0.1	1.7		0.1	1.7		0.1	10	μA	V_{CB} = 40.0V
	ON CHARACTERISTICS												
	Base-Emitter Saturation Voltage	V_{BE} (sat.)	0.9	0.95	1.2	0.9	0.95	1.2		0.95	1.5	V	I_C = 500mA, I_B = 50mA
				1.1	1.7		1.1	1.7				V	I_C = 1A, I_B = 100mA
	Collector Saturation	V_{CE} (sat.)		0.3	0.55		0.3	0.5		0.3	0.6	V	I_C = 500mA, I_B = 50mA
				0.5	1.0		0.5	0.9				V	I_C = 1A, I_B = 100mA
	D.C. Current Gain	h_{FE}	50	90		50	90		25	90			I_C = 100mA, V_{CE} = 1.0V
			20	50		30	50		10	50			I_C = 500mA, V_{CE} = 1.0V
			10	20		15	20						I_C = 1A, V_{CE} = 1.0V
AC	SWITCHING CHARACTERISTICS												
	Turn On Time	t_{on}		25	35		25	35		25	50	ns	I_C = 500mA
	Turn Off Time	t_{off}		45	60		45	60		45	75	ns	I_{B1} = I_{B2} = 50mA
	Emitter-Base Capacitance	C_{EB}		45			45			45		pF	V_{EB} = 0.5V
	Collector-Base Capacitance	C_{CB}		5	12		5	12		5	12	pF	V_{CB} = 10.0V

PACKAGE

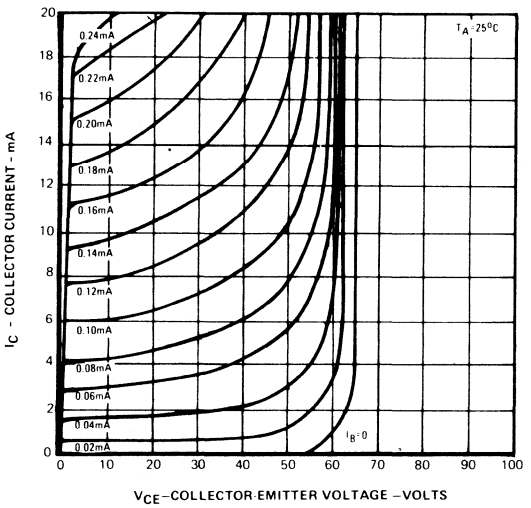


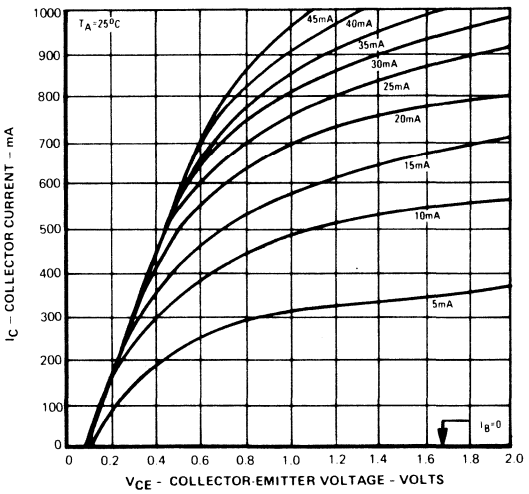
CONNECTION DIAGRAM



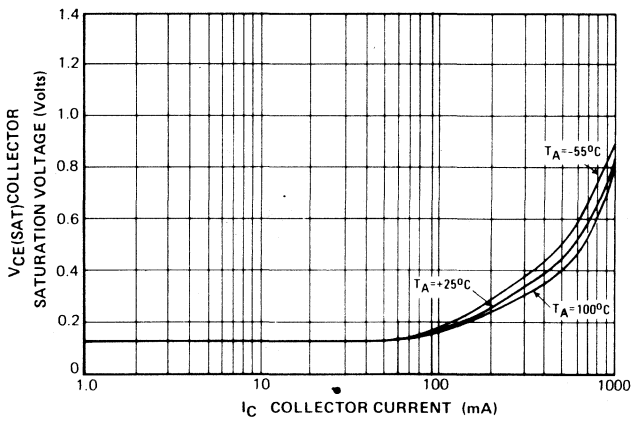
PERFORMANCE CURVES

COLLECTOR CHARACTERISTICS

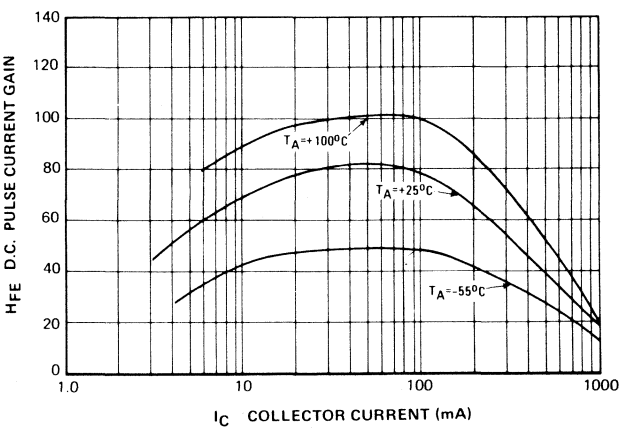




COLLECTOR SATURATION VOLTAGE vs COLLECTOR CURRENT



D.C. PULSE CURRENT GAIN vs COLLECTOR CURRENT



DIGITAL DATA

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

LOGIC INTERFACE CIRCUITS

GENERAL DESCRIPTION

The integrated circuits covered by this data sheet form a part of Harris' family of Military and Industrial Monolithic Interface Circuits intended for use as universal inverters, translators between logic families, as logic drivers in Monolithic Diode Matrix logic and in high voltage applications. The interface circuit with the node-input is compatible with all logic families, RTL, DTL, T^2L and CML. The circuits are fabricated within a single monolithic silicon chip using passivated epitaxial techniques and Harris' Dielectric Isolation method. Each circuit type consists of six node-input inverters as shown in the circuit schematic. Use of Dielectric Isolation provides parasitic-free operation with electrical performance surpassing that of conventionally constructed integrated circuits. Harris' Interface Circuits are designed to meet or exceed the mechanical and environmental requirements of MIL-STD-883.

MILITARY	**200**	**SERIES**
INDUSTRIAL	**500**	**SERIES**

BASIC TYPES OF INTERFACE CIRCUITS

HEX INTERFACE INVERTER

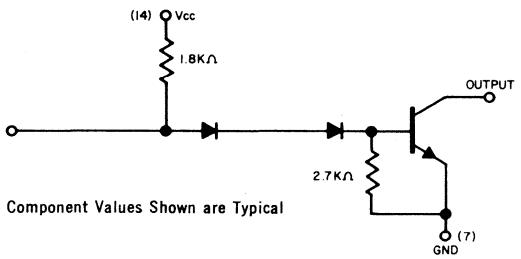
PROPAGATION DELAY	10ns
POWER DISSIPATION	10mW
OUTPUT BREAKDOWN VOLTAGE	6V

HIGH VOLTAGE HEX INTERFACE DRIVER

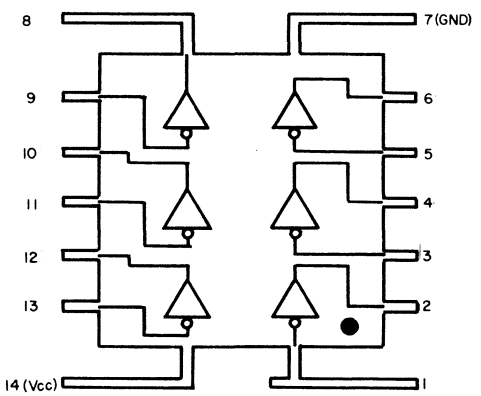
PROPAGATION DELAY	35ns
POWER DISSIPATION	10mW
OUTPUT BREAKDOWN VOLTAGE	35V

HIGH VOLTAGE HEX INDICATOR DRIVER

TURN-ON OR TURN-OFF DELAY	0.8 s
PROPAGATION DELAY	35ns
POWER DISSIPATION	12mW
OUTPUT BREAKDOWN VOLTAGE	55V



BASIC CIRCUIT SCHEMATIC
(one element)



LOGIC DIAGRAM
(top view)

SELECTION GUIDE

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts
Output Voltage : +6 Volts
V_{cc} : +8 Volts
Output Current : ±50mA
Operating Temp. : −55°C to +125°C
Storage Temp. : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	DRIVEN INPUT	OUTPUT	NOTES See Page 3
"1" OUTPUT VOLTAGE									
node Input	4.0	4.5		V	−55°C	4.5V	2.2V	SEE	3
node Input	4.0	4.5		V	+25°C	4.5V	1.8V	NOTE	3
node Input	3.7	4.4		V	+125°C	4.5V	1.2V	2a	3
"0" OUTPUT VOLTAGE									
node Input		.25	.45	V	−55°C	4.5V		16.7mA	3
node Input		.25	.40	V	+25°C	5.0V		20.5mA	3
node Input		.25	.45	V	+125°C	5.5V		20.5mA	3
"0" INPUT CURRENT									
node Input		2.55	3.45	mA	−55°C	5.5V	.35V		3
node Input	1.80	2.70	3.45	mA	+25°C	5.5V	.35V		3
node Input		2.30	3.45	mA	+125°C	5.5V	.35V		3
"1" OUTPUT CURRENT									
			100	nA	+25°C	4.5V	GND	4.5V	3
			50	μA	+125°C	4.5V	GND	4.5V	3
POWER DISSIPATION									
		12	17.5	mW	+25°C	5.0V	GND		
		8	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE									
		2.0		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	TEST CIRCUIT	FAN-OUT
Turn On Delay		20	35	ns	−55°C	4.5V		8
t_{on}		13	20	ns	+25°C	4.5V	Circuit No. 1	8
		15	22	ns	+125°C	4.5V	$R_L = 220\Omega$	8
Turn Off Delay		10	25	ns	−55°C	5.5V	2	1
t_{off}		5	15	ns	+25°C	5.5V	2	1
		8	25	ns	+125°C	5.5V	2	1
Propagation Delay t_{pd}		8	12	ns	+25°C	5.0V	3	1

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts
Output Voltage : +35 Volts
V_{cc} : +8 Volts
Output Current : ±35mA
Operating Temp. : −55°C to +125°C
Storage Temp. : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	DRIVEN INPUT	OUTPUT	NOTES See Page 3
"1" OUTPUT VOLTAGE									
node Input	29			V	−55°C	4.5V	2.2V	SEE	3
node Input	29			V	+25°C	4.5V	1.8V	NOTE	3
node Input	28			V	+125°C	4.5V	1.2V	2b	3
"0" OUTPUT VOLTAGE									
node Input			1.0	V	−55°C	4.5V		5mA	3
node Input		.55	1.0	V	+25°C	5.0V		10mA	3
node Input			1.0	V	+125°C	5.5V		10mA	3
"0" INPUT CURRENT									
node Input		2.55	3.45	mA	−55°C	5.5V	.35V		3
node Input	1.80	2.70	3.45	mA	+25°C	5.5V	.35V		3
node Input		2.30	3.45	mA	+125°C	5.5V	.35V		3
"1" OUTPUT CURRENT									
		.025	1.0	μA	+25°C	4.5V	GND	30V	3
		1	50	μA	+125°C	4.5V	GND	30V	3
POWER DISSIPATION									
		12	17.5	mW	+25°C	5.0V	GND		
		8	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE									
		5.0		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	TEST CIRCUIT
Propagation Delay			80	ns	−55°C	5.0V	
t_{pd}		35	70	ns	+25°C	5.0V	3
			80	ns	+125°C	5.0V	

NOTES:

1. This specification is written for one gate element. With multiple element packages, all elements within the package must qualify for the package to obtain "type" classification.

2a. The output is to be returned to V_{cc} through 5.6KΩ for these tests.

2b. The output is to be returned to +30V through 5.6KΩ for these tests.

3. "NAND" Logic Definitions: "UP" Level = "1" "DOWN" Level = "0".

4. All measurements made with Pin 7 at zero volts. All voltage and capacitance measurements are referenced to pin 7. Terminals not specifically mentioned are left electrically open.

5. These measurements must be made using current forcing, voltage measuring techniques.

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts
Output Voltage : +6 Volts
V_{cc} : +8 Volts
Output Current : ±50mA
Operating Temp. : 0°C to +75°C
Storage Temp. : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	DRIVEN INPUT	OUTPUT	NOTES See Page 3
"1" OUTPUT VOLTAGE									
node Input	3.0	3.8		V	0°C	4.5V	1.6V	SEE	3
node Input	3.0	3.8		V	+25°C	4.5V	1.6V	NOTE	3
node Input	3.0	3.8		V	+75°C	4.5V	1.3V	2a	3
"0" OUTPUT VOLTAGE									
node Input		.30	.45	V	0°C	4.5V		12.0mA	3
node Input		.30	.45	V	+25°C	5.0V		13.3mA	3
node Input		.30	.45	V	+75°C	5.5V		14.4mA	3
"0" INPUT CURRENT									
node Input		2.70	3.45	mA	0°C	5.5V	.45V		3
node Input	1.80	2.70	3.45	mA	+25°C	5.5V	.45V		3
node Input		2.70	3.45	mA	+75°C	5.5V	.45V		3
"1" OUTPUT CURRENT									
		.05	1	μA	+25°C	4.5V	GND	4.5V	3
		.1	5	μA	+75°C	4.5V	GND	4.5V	3
POWER DISSIPATION									
		14.8	17.5	mW	+25°C	5.0V	GND		
		10.0	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE		2.0		pF	+25°C	5.0V		0.5VDC 25mVrms @ 1 MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	TEST CIRCUIT
Propagation Delay t_{pd}		18	25	ns	+25°C	5.0V	3

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts Output Current : ±35mA
Output Voltage : +35 Volts Operating Temp. : −0°C to +75°C
V_{cc} : +8 Volts Storage Temp. : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS				TEST CONDITIONS				
	MIN.	TYP.	MAX.	UNIT	TEMP.	V_{cc}	DRIVEN INPUT	OUTPUT	NOTES See Page 3
"1" OUTPUT VOLTAGE									
node Input	29			V	0°C	4.5V	1.6V	SEE	3
node Input	29			V	+25°C	4.5V	1.6V	NOTE	3
node Input	28			V	+75°C	4.5V	1.3V	2b	3
"0" OUTPUT VOLTAGE									
node Input			1.0	V	0°C	4.5V		8.0mA	3
node Input		.65	1.0	V	+25°C	5.0V		8.0mA	3
node Input			1.0	V	+75°C	5.5V		8.0mA	3
"0" INPUT CURRENT									
node Input		2.95	3.45	mA	0°C	5.5V	.45V		3
node Input	1.80	2.95	3.45	mA	+25°C	5.5V	.45V		3
node Input		2.95	3.45	mA	+75°C	5.5V	.45V		3
"1" OUTPUT CURRENT									
		.1	1	μA	+25°C	4.5V	GND	30V	3
		1	50	μA	+75°C	4.5V	GND	30V	3
POWER DISSIPATION									
		14.8	17.5	mW	+25°C	5.0V	GND		
		10.0	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE		5.0		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1 MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

CHARACTERISTIC	LIMITS				TEST CONDITIONS		
	MIN.	TYP.	MAX.	UNIT	TEMP.	V_{cc}	TEST CIRCUIT
Propagation Delay t_{pd}		35	70	ns	+25°C	5.0V	3

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Input Voltage : +6 Volts Output Current : ±25mA
Output Voltage : +55 Volts Operating Temp. : −0°C to +75°C
V_{cc} : +8 Volts Storage Temp. : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

STATIC ELECTRICAL CHARACTERISTICS (Notes 1, 4)

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	DRIVEN INPUT	OUTPUT	NOTES See Page 3
"1" OUTPUT VOLTAGE									
node Input	3.0	3.5		V	0°C	4.5V	1.6V	SEE	3
node Input	3.0	3.5		V	+25°C	4.5V	1.6V	NOTE	3
node Input	3.0	3.5		V	+75°C	4.5V	1.3V	2a	3
"0" OUTPUT VOLTAGE									
node Input			1.0	V	0°C	4.5V		8.0mA	3
node Input		.75	1.0	V	+25°C	5.0V		8.0mA	3
node Input			1.0	V	+75°C	5.5V		8.0mA	3
"0" INPUT CURRENT									
node Input		2.95	3.45	mA	0°C	5.5V	.45V		3
node Input	1.80	2.95	3.45	mA	+25°C	5.5V	.45V		3
node Input		2.95	3.45	mA	+75°C	5.5V	.45V		3
OUTPUT BREAKDOWN VOLTAGE	55	65		V	+25°C	4.5V	GND	100μA	3, 5
	55			V	+75°C	4.5V	GND	100μA	3, 5
POWER DISSIPATION		14.8	17.5	mW	+25°C	5.0V	GND		
		10.0	11.0	mW	+25°C	5.0V	OPEN		
OUTPUT CAPACITANCE		8		pF	+25°C	5.0V	GND	0.5VDC 25mVrms @ 1MHz	

SWITCHING (DYNAMIC) CHARACTERISTICS

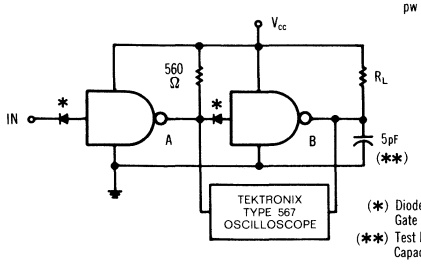
CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS TEMP.	V_{cc}	TEST CIRCUIT
Turn On Delay t_{on}		.80	2.0	μs	+25°C	5.0V	4
Turn Off Delay t_{off}		1.0	2.0	μs	+25°C	5.0V	4

DIGITAL DATA

TEST CIRCUITS

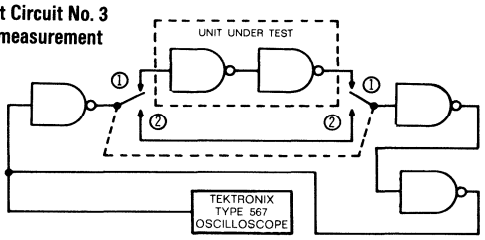
Test Circuit No. 1
t_{on} and t_{off} — measurements

INPUT PULSE
$t_r = t_f = 5ns$
$f = 1MH_z$
$pw = 100ns$



(*) Diodes from Expander Gate RD-211
(**) Test Fixture and Probe Capacity

Test Circuit No. 3
t_{pd} measurement



Propagation delay for one element based on pair delay measurement

$t_{pd} = \frac{T_5 - T_3}{4}$ Where

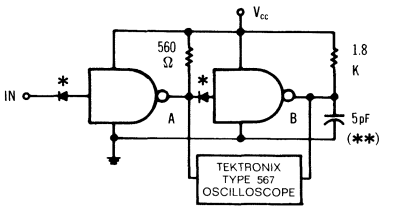
T_5 = Measured time for one cycle of oscillation with switch in position ① (5 elements)

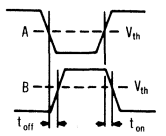
And

T_3 = Measured time for one cycle of oscillation with switch in position ② (3 elements standard)

Test Circuit No. 2
t_{on} and t_{off} — measurements

(*) Diodes from Expander Gate RD-211
(**) Test Fixture and Probe Capacity

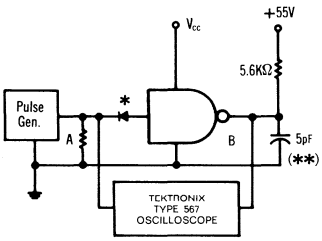


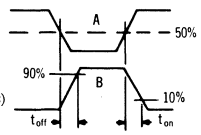


V_{TH}	−55°C	+25°C	+125°C
	1.9V	1.5V	1.2V

Test Circuit No. 4
t_{on} and t_{off} — measurements

INPUT PULSE
$t_r = t_f = 5ns$
$f = 100KH_z$
$pw = 5.0\mu s$
$Amp. = +3.5V$



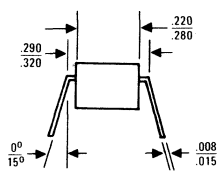


(*) Diodes from Expander Gate RD-211
(**) Test Fixture and Probe Capacity

DIGITAL DATA

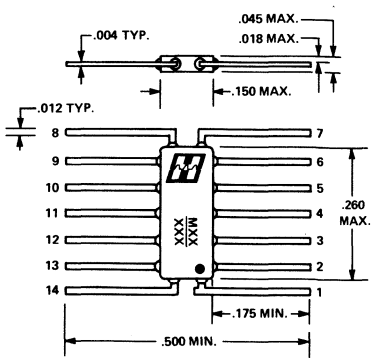
PACKAGING

Package outline drawings for Harris Integrated Circuits products are illustrated at right. For each package, a particular Harris protective carrier is used in production, testing, and handling. If desired, this protective carrier may be specified for shipping purposes. Harris can also furnish custom designed packages from its in-house facility. The package Carriers and their releationship to corresponding test contactors are shown.



14-PIN TO-84 PACKAGE OUTLINE (KOVAR)

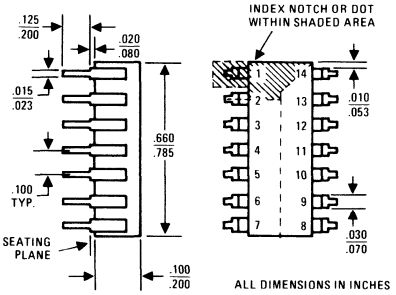
CONTACTOR 029-001
CARRIER 029-040
Barnes Development Company



LEADS SPACED .050 ON CENTER. TOLERANCES NON-CUMULATIVE.

14-PIN DUAL INLINE (PLUG-IN) PACKAGE (CERAMIC, WITH KOVAR BASE)

CONTACTOR 029-271-01
CARRIER 029-240-01
Barnes Development Company



ALL DIMENSIONS IN INCHES

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS

HD-4000

Dual 3-Input 'NOR' Gate Plus Inverter

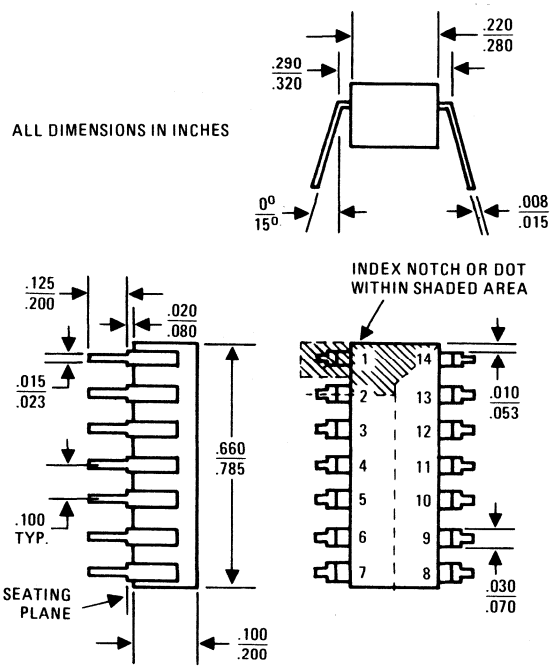
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 1nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- ONLY ONE POWER SUPPLY REQUIRED
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

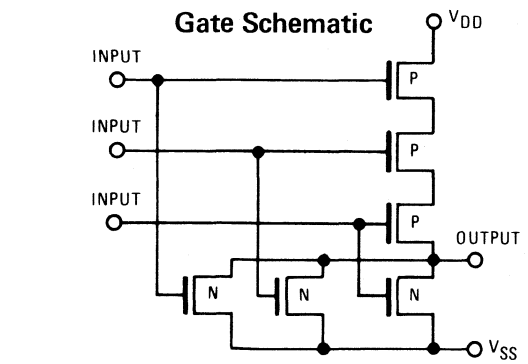
DESCRIPTION

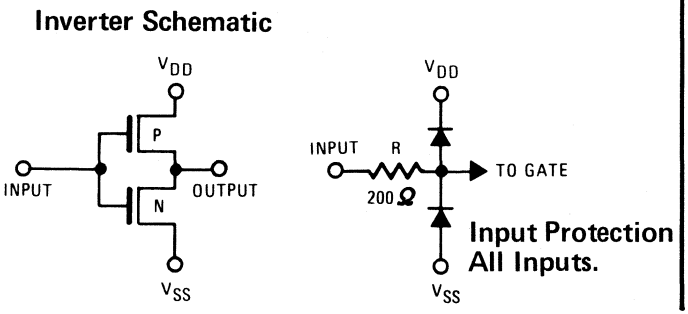
The HD-4000 Dual 3-Input NOR Gate with Inverter is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris low capacitance Dielectric Isolation process. The HD-4000 is designed for high speed applications which require extremely low power dissipation and good noise immunity. The wide supply voltage range provides considerable power supply flexibility. Pin equivalent to CD-4000A.

PACKAGE

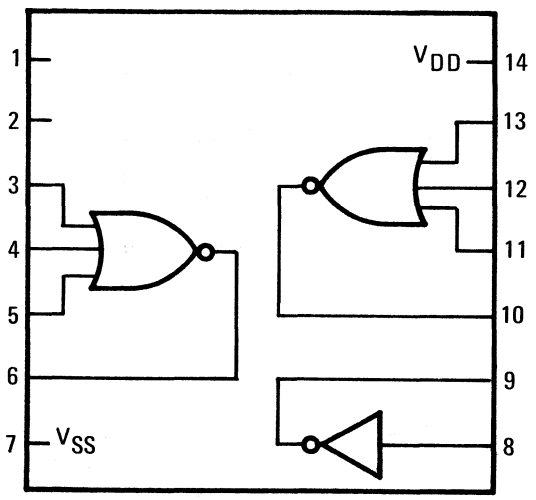


CIRCUIT DIAGRAMS





LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} -V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	.31 .62			.25 .50	.5 1.0		.175 .35			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.31 -.75			-.25 -.60	-.5 -1.2		-.175 -.40			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		.05 .10			.05 .10	50 100			300 600	nA nA	5 10	
Input Capacitance						7					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	25 10	40 20	40 20	80 50	ns ns	5 10	T_A = 25°C
	t_{PHL}	25 10	40 20	40 20	80 50	ns ns	5 10	Ref. To Switching Time Definitions
Transition Time	t_{TLH}	35 20	70 40	100 35	150 70	ns ns	5 10	
	t_{THL}	30 15	60 30	100 35	150 70	ns ns	5 10	

NOTE: 1 V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level that the circuit will withstand before producing an output state change.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} -V_{SS}	-0.5VDC to +15VDC
Input Voltage Range, (All Inputs) V_{IN}	V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} =+3VDC to +15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	-40°C MIN.	-40°C TYP.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	.145 .3			.12 .25	.5 1.0		.175 .35			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.175 -.40			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		5 5			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						7					pF		

A.C.

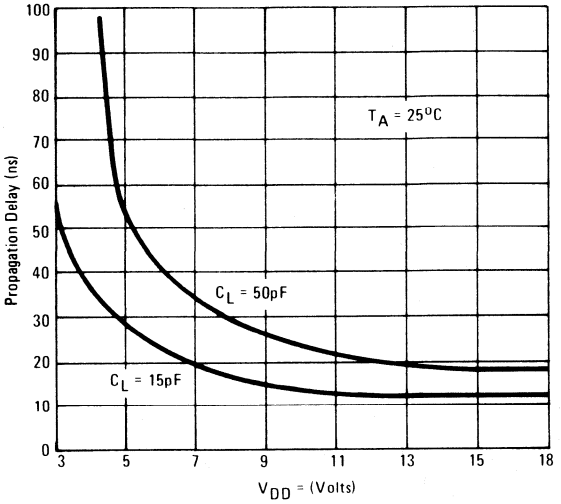
PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	30 12	50 25	45 25	150 75	ns ns	5 10	T_A = 25°C
	t_{PHL}	30 12	50 25	45 25	150 75	ns ns	5 10	Ref. To Switching Time Definitions
Transition Time	t_{TLH}	40 25	85 50	120 40	250 150	ns ns	5 10	
	t_{THL}	35 18	75 40	120 40	225 120	ns ns	5 10	

NOTE: 1 V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level that the circuit will withstand before producing an output state change.

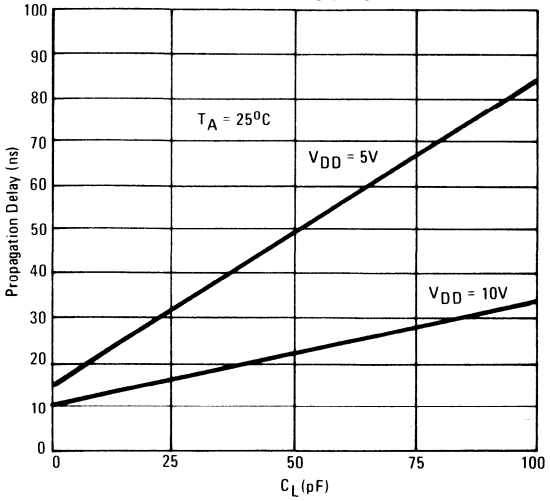
DIGITAL DATA

TYPICAL CHARACTERISTICS

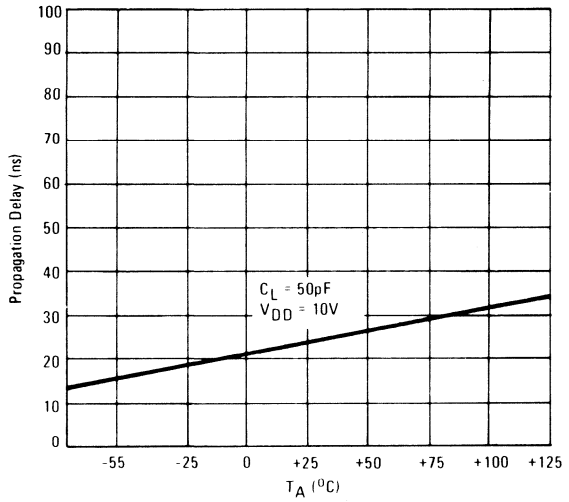
TYPICAL PROPAGATION DELAY
vs. SUPPLY VOLTAGE



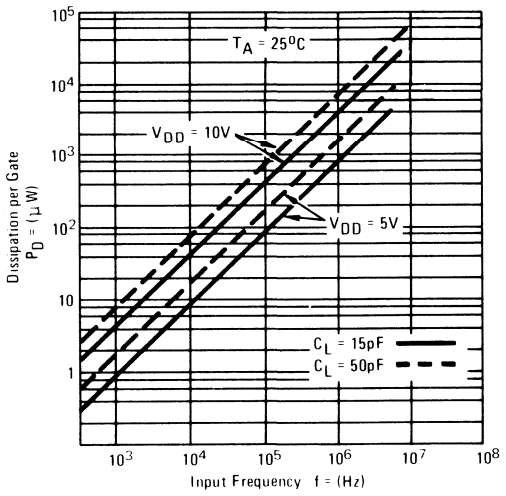
TYPICAL PROPAGATION DELAY
vs. LOAD CAPACITANCE



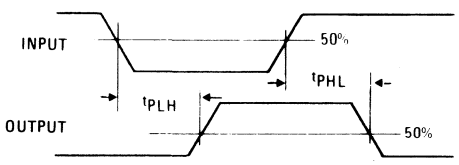
TYPICAL PROPAGATION DELAY
vs. AMBIENT TEMPERATURE

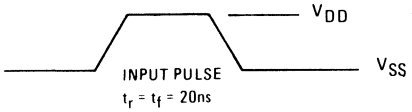


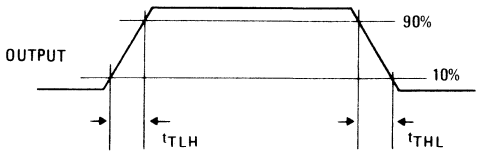
TYPICAL POWER DISSIPATION
vs. INPUT FREQUENCY

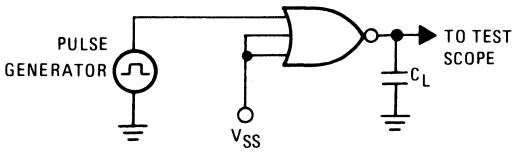


SWITCHING TIME DEFINITION AND CONDITIONS









HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS
HD-4001
Quad 2-Input 'NOR' Gate

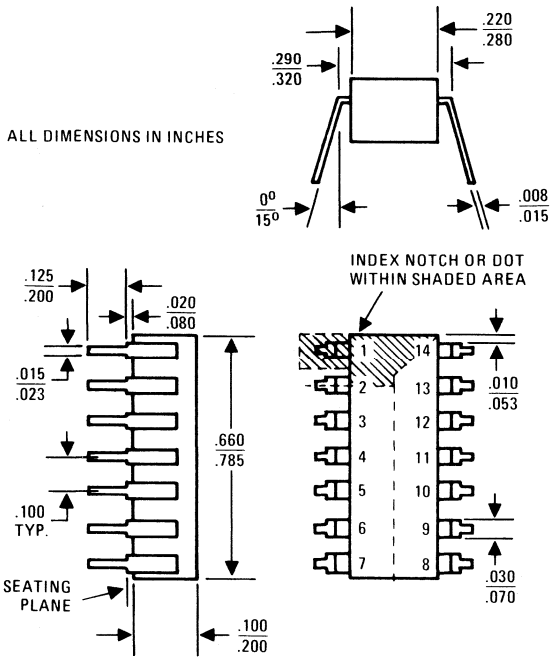
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 1nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- ONLY ONE POWER SUPPLY REQUIRED
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

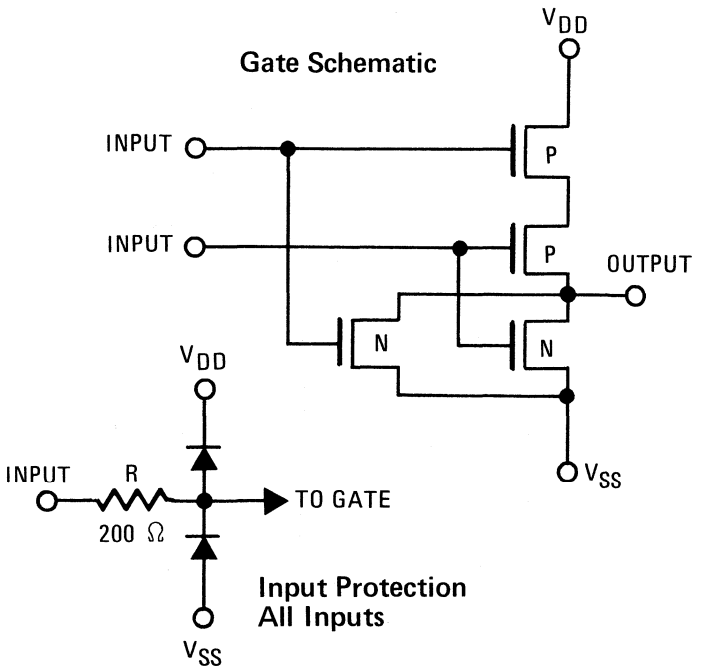
DESCRIPTION

The HD-4001 Quad 2-Input NOR Gate is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris low capacitance Dielectric Isolation process. The HD-4001 is designed for high speed applications which require extremely low power dissipation and good noise immunity. The wide supply voltage range provides considerable power supply flexibility. Pin equivalent to CD-4001A

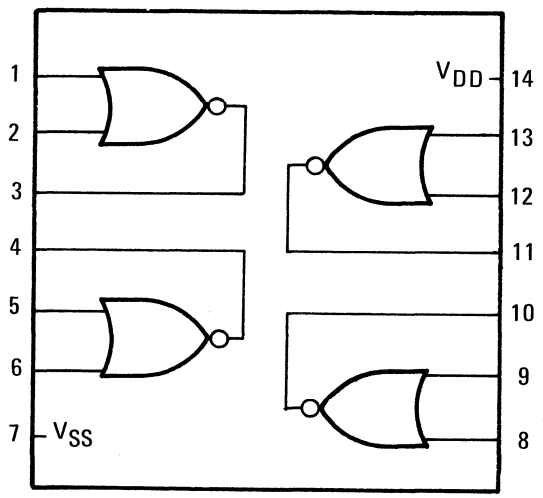
PACKAGE



CIRCUIT DIAGRAMS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATING

Power Supply Voltage Range, V_{DD} -V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	.31 .62			.25 .50	.5 1.0		.175 .35			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.31 -.75			-.25 -.60	-.5 -1.2		-.175 -.40			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		.05 .10			.05 .10	50 100			300 600	nA nA	5 10	
Input Capacitance						7					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	25 10	40 20	40 20	80 50	ns ns	5 10	Ref. To Switching Time Definitions T_A = 25°C
	t_{PHL}	25 10	40 20	40 20	80 50	ns ns	5 10	
Transition Time	t_{TLH}	35 20	70 40	100 35	150 70	ns ns	5 10	
	t_{THL}	30 15	60 30	100 35	150 70	ns ns	5 10	

NOTE: 1 V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level that the circuit will withstand before producing an output state change.

DIGITAL DATA

ABSOLUTE MAXIMUM RATING

Power Supply Voltage Range, V_{DD} -V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	-40°C MIN.	-40°C TYP.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
Input Leakage	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq 3.5VDC$ $V_{OH} \geq 7.0VDC$
Noise Immunity (Note 1)	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq 1.5VDC$ $V_{OL} \leq 3.0VDC$
Output Drive Current	I_{OL}	.145 .3			.12 .25	.5 1.0		.095 .2			mA mA	5 10	$V_{OL} = .5VDC$ $V_{OL} = .5VDC$
Output Drive Current	I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.095 -.25			mA mA	5 10	$V_{OH} = 4.5VDC$ $V_{OH} = 9.5VDC$
Quiescent Power Supply Current	I_{DD}		5 5			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						7					pF		

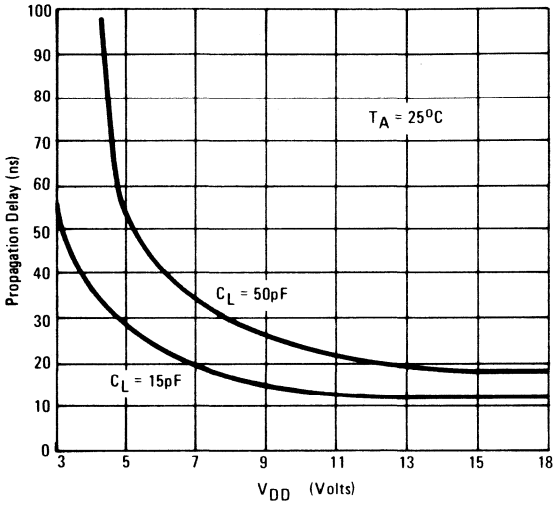
A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	30 12	50 25	45 25	150 75	ns ns	5 10	Ref. To Switching Time Definitions $T_A = 25°C$
Propagation Delay	t_{PHL}	30 12	50 25	45 25	150 75	ns ns	5 10	
Transition Time	t_{TLH}	40 25	85 50	120 40	250 150	ns ns	5 10	
Transition Time	t_{THL}	35 18	75 40	120 40	225 120	ns ns	5 10	

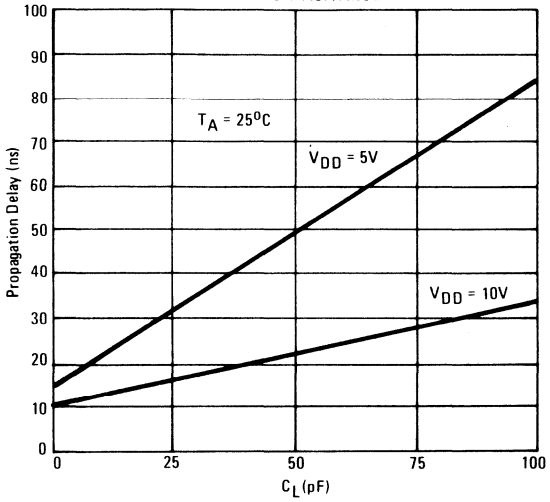
NOTE: 1 V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level that the circuit will withstand before producing an output state change.

TYPICAL CHARACTERISTICS

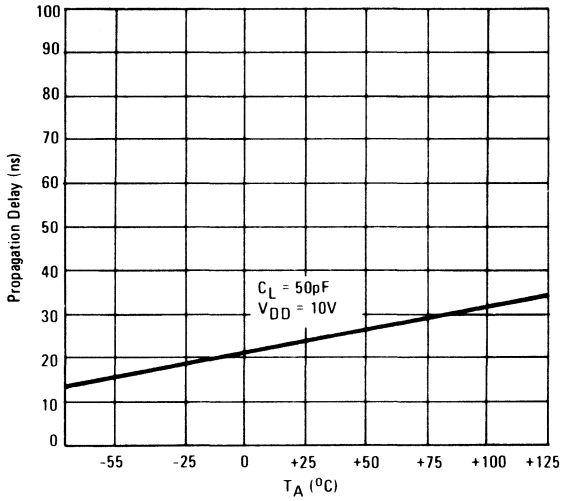
TYPICAL PROPAGATION DELAY
vs. SUPPLY VOLTAGE



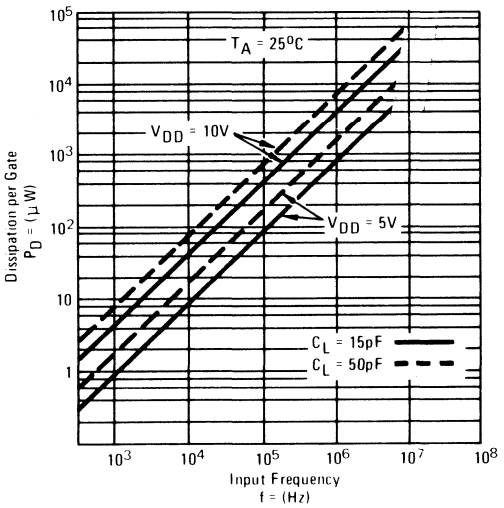
TYPICAL PROPAGATION DELAY
vs. LOAD CAPACITANCE



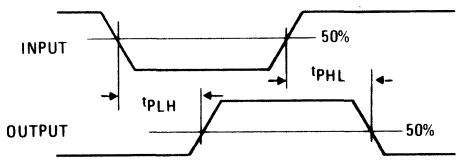
TYPICAL PROPAGATION DELAY
vs. AMBIENT TEMPERATURE

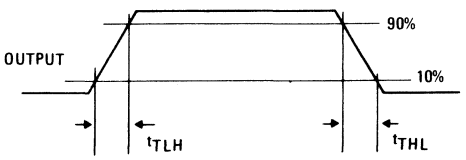


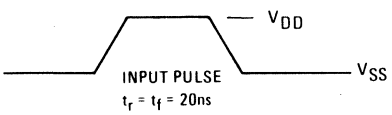
TYPICAL POWER DISSIPATION
vs. INPUT FREQUENCY

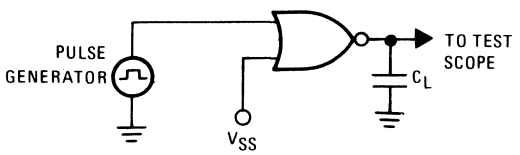


SWITCHING TIME DEFINITIONS AND CONDITIONS









HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS

HD-4009

Hex Inverter/Buffer

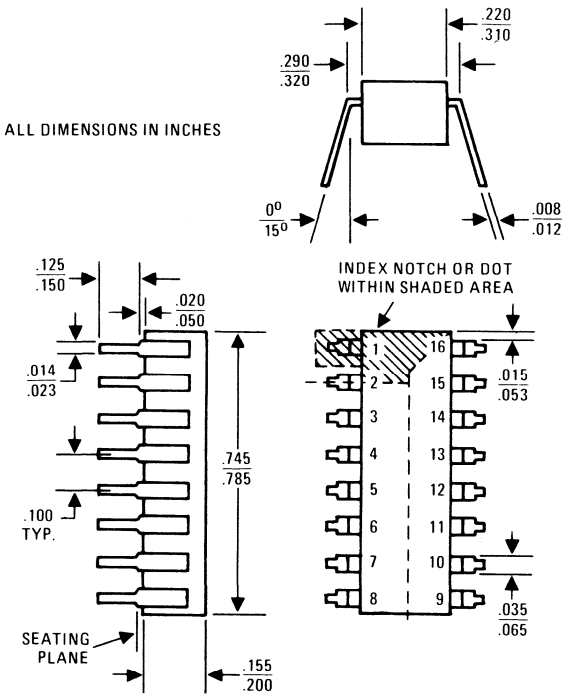
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 50nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

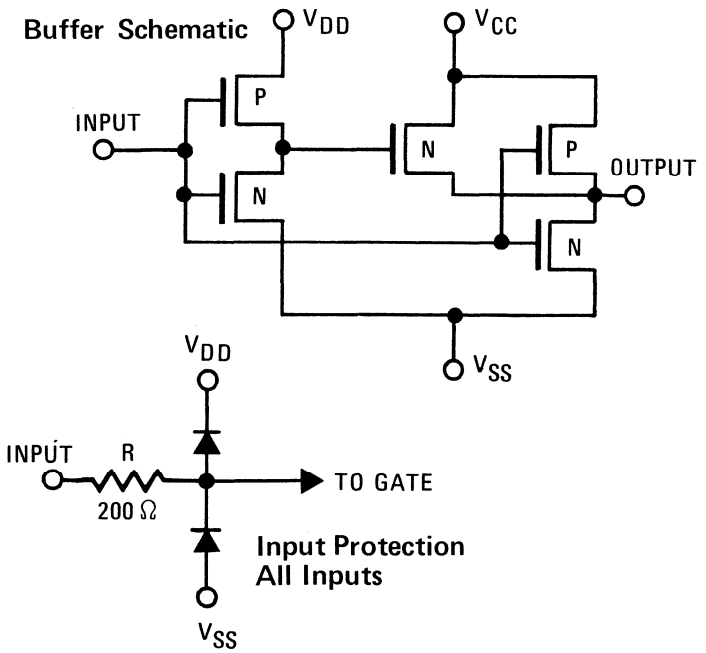
DESCRIPTION

The HD-4009 Hex Inverter/Buffer is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris low capacitance Dielectric Isolation process. The HD-4009 is designed as a Hex Inverting Buffer and can be used as drivers for CMOS to CMOS or CMOS to TTL/DTL Logic. Pin equivalent to CD-4009A

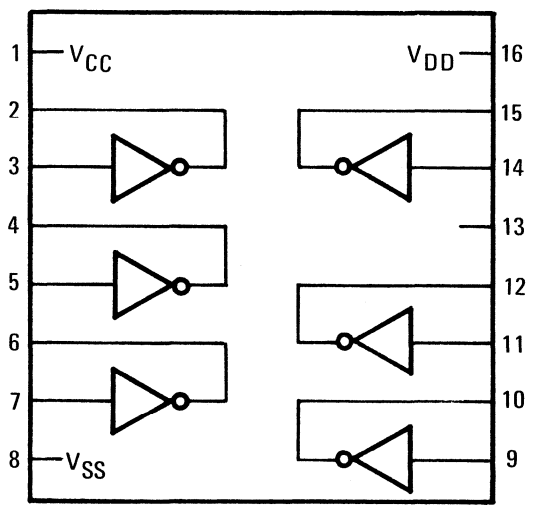
PACKAGE



CIRCUIT DIAGRAMS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS} & V_{CC} - V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC To V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{CC} = +3VDC to V_{DD}, V_{DD} = +3VDC to + 18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} UNLESS OTHERWISE SPECIFIED)

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	V_{IL} = V_{SS},
	I_{IH}		10			10			20		pA	10	V_{IH} = V_{DD},
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	3.75 10			3.0 8.0	4 10		2.1 5.6			mA mA	5 10	V_{OL} = .4 VDC V_{OL} = .5VDC
	I_{OH}	-1.85 - .9			-1.25 -.60	-2.0 -1.0		-.9 -.40			mA mA	5 10	V_{OH} = 2.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{SS}		10 15			10 15	100 150			600 900	nA nA	5 10	
Input Capacitance						7					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES	
Propagation Delay	t_{PLH}	20 15	40 25	45 25	80 50	ns ns	5 10	V_{CC} = V_{DD}	T_A = 25°C
		10	20	20	35	ns	10	V_{CC} = 5VDC	
	t_{PHL}	15 10	25 15	25 10	50 30	ns ns	5 10	V_{CC} = V_{DD}	
		10	15	15	25	ns	10	V_{CC} = 5VDC	
Transition Time	t_{THL}	15 10	25 20	30 15	45 35	ns ns	5 10	V_{CC} = V_{DD}	
	t_{TLH}	40 25	65 50	70 55	125 100	ns ns	5 10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD}-V_{SS} & V_{CC} - V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC To V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{CC} = +3VDC to V_{DD}, V_{DD} = +3VDC to + 15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} UNLESS OTHERWISE SPECIFIED)

D.C.

PARAMETER	SYM.	40°C MIN.	40°C TYP.	40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	V_{IL} = V_{SS}
	I_{IH}		10			10			20		pA	10	V_{IH} = V_{DD}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	3.6 9.6			3 8	4 10		2.4 6.4			mA mA	5 10	V_{OL} = .4VDC V_{OL} = .5VDC
	I_{OH}	-1.85 - .9			-1.25 -.6	-1.75 -.8		-1 -.48			mA mA	5 10	V_{OH} = 2.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{SS}		10 15			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						7					pF		

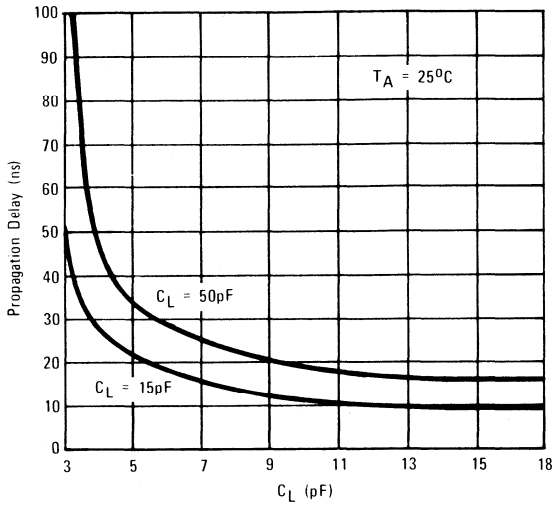
A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES	
Propagation Delay	t_{PLH}	25 20	50 30	75 60	150 90	ns ns	5 10	V_{CC} = V_{DD}	T_A = 25°C
		15	25	40	75	ns	10	V_{CC} = 5VDC	
	t_{PHL}	20 15	30 20	60 45	90 60	ns ns	5 10	V_{CC} = V_{DD}	
		15	20	30	60	ns	10	V_{CC} = 5VDC	
Transition Time	t_{THL}	20 15	30 25	60 45	90 75	ns ns	5 10	V_{CC} = V_{DD}	
	t_{TLH}	40 30	80 60	120 85	245 180	ns ns	5 10		

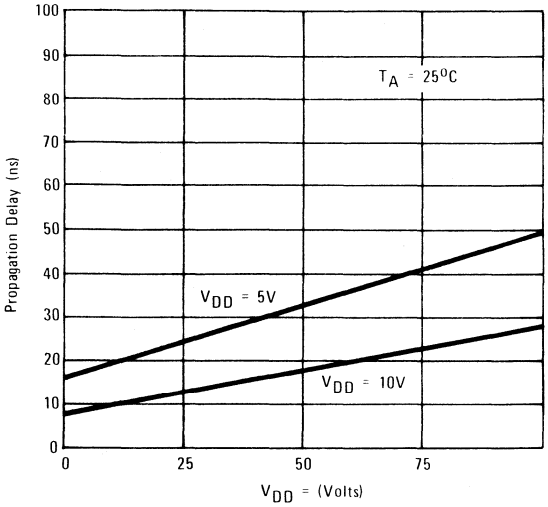
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

TYPICAL CHARACTERISTICS

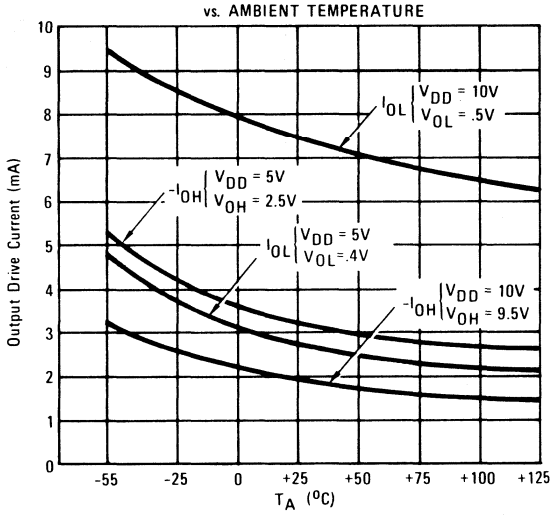
TYPICAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



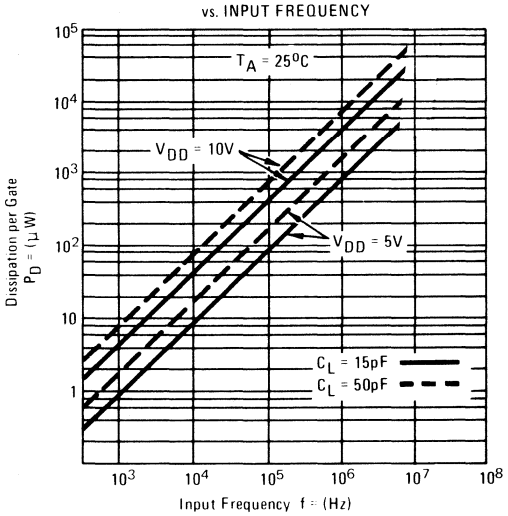
TYPICAL PROPAGATION DELAY vs. LOAD CAPACITANCE



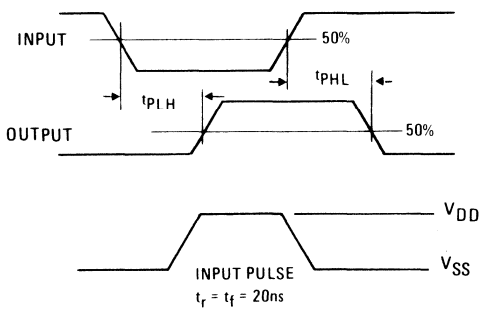
TYPICAL OUTPUT DRIVE CURRENT vs. AMBIENT TEMPERATURE

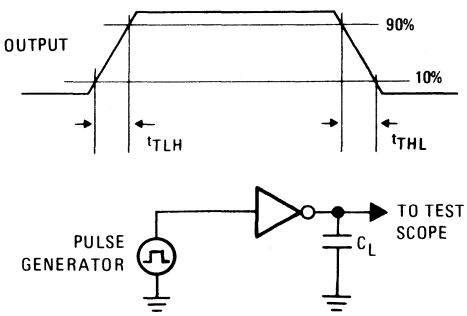


TYPICAL POWER DISSIPATION vs. INPUT FREQUENCY



SWITCHING TIME DEFINITIONS AND CONDITIONS





HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS
HD-4010
Hex Buffer

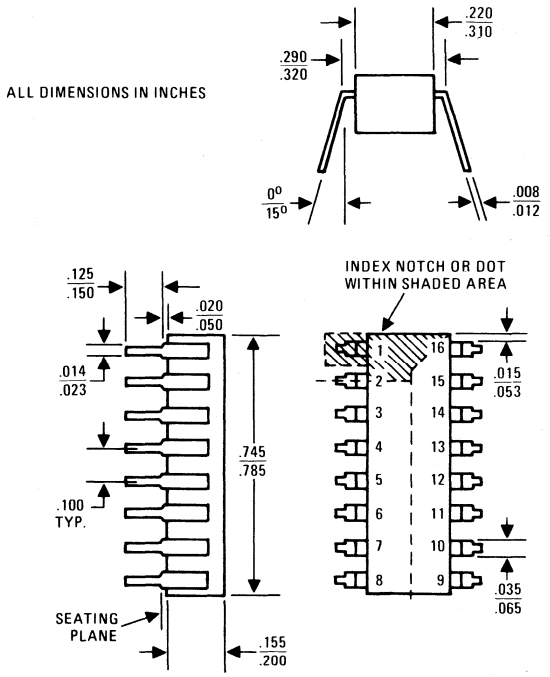
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 50nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTGE
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

DESCRIPTION

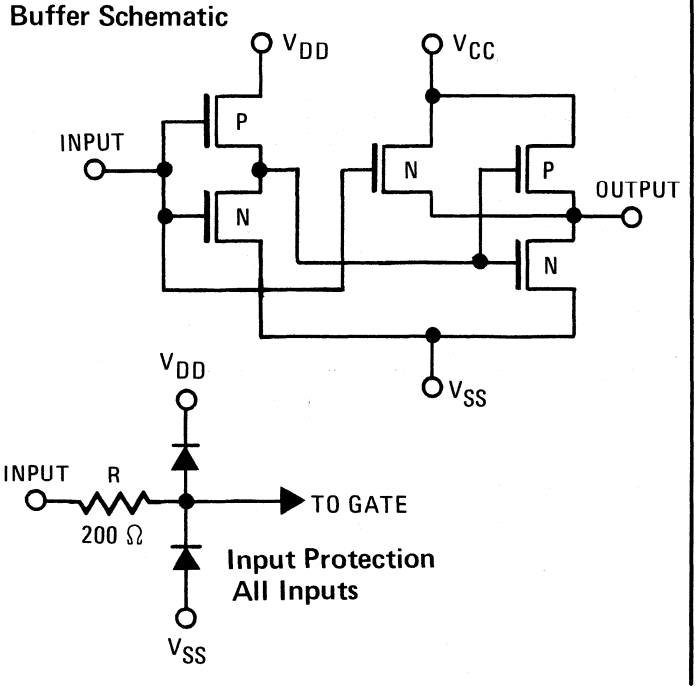
The HD-4010 Hex Buffer is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris low capacitance Dielectric Isolation process. The HD-4010 is designed as a Hex Buffer and can be used as drivers for CMOS to CMOS or CMOS to TTL/DTL Logic. Pin equivalent to CD-4010A.

PACKAGE

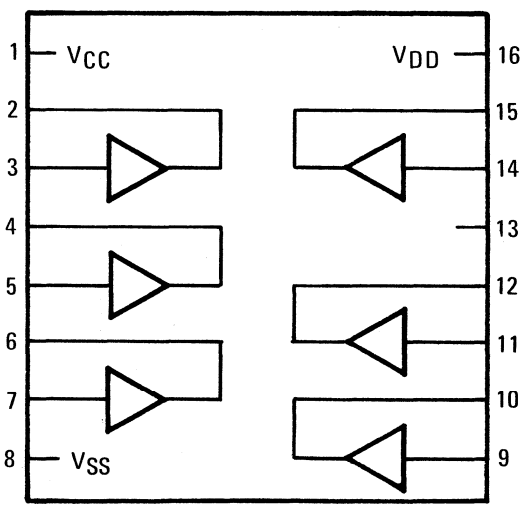


CIRCUIT DIAGRAMS

Buffer Schematic



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS} & V_{CC} - V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{CC} = +3VDC to V_{DD}, V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} UNLESS OTHERWISE SPECIFIED)

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	V_{IL} = V_{SS}
	I_{IH}		10			10			20		pA	10	V_{IH} = V_{DD}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	3.75 10			3.0 8.0	4 10		2.1 5.6			mA mA	5 10	V_{OL} = .4VDC V_{OL} = .5VDC
	I_{OH}	-1.85 - .9			-1.25 -.60	-2.0 -1.0		-.9 -.40			mA mA	5 10	V_{OH} = 2.5 VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{SS}		10 15			10 15	100 150			600 900	nA nA	5 10	
Input Capacitance						7					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES	
Propagation Delay	t_{PLH}	20 15	40 25	45 25	80 50	ns ns	5 10	V_{CC} = V_{DD}	T_A = 25°C
		10	20	20	35	ns	10	V_{CC} = 5VDC	
	t_{PHL}	15 10	25 15	25 10	50 30	ns ns	5 10	V_{CC} = V_{DD}	
		10	15	15	25	ns	10	V_{CC} = 5VDC	
Transition Time	t_{THL}	25	65 50	70 55	125 100	ns ns	5 10	V_{CC} = V_{DD}	
	t_{TLH}	15 10	25 20	30 15	45 35	ns ns	5 10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} -V_{SS} & V_{CC} -V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{CC} = +3VDC to V_{DD}, V_{DD} = +3VDC to +15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{DD}$ UNLESS OTHERWISE SPECIFIED)

D.C.

PARAMETER	SYM.	−40°C MIN.	−40°C TYP.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq 3.5$VDC $V_{OH} \geq 7.0$VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq 1.5$VDC $V_{OL} \leq 3.0$VDC
Output Drive Current	I_{OL}	3.6 9.6			3.0 8.0	4 10		2.4 6.4			mA mA	5 10	$V_{OL} = .4$VDC $V_{OL} = .5$VDC
	I_{OH}	-1.5 -.72			-1.25 -.60	-1.75 -.80		-1.0 -.48			mA mA	5 10	$V_{OH} = 2.5$VDC $V_{OH} = 9.5$VDC
Quiescent Power Supply Current	I_{SS}		10 15			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						7					pF		

A.C.

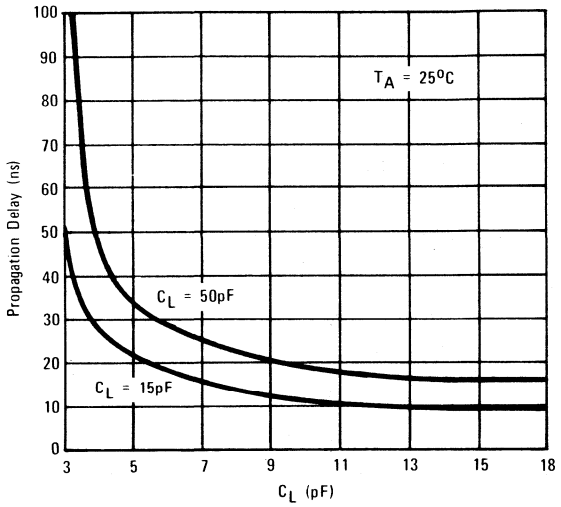
PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES	
Propagation Delay	t_{PLH}	25 20	50 30	75 60	150 90	ns ns	5 10	$V_{CC} = V_{DD}$	$T_A = 25°C$
		15	25	40	75	ns	10	V_{CC} = 5VDC	
	t_{PHL}	20 15	30 20	60 45	90 60	ns ns	5 10	$V_{CC} = V_{DD}$	
		15	20	30	60	ns	10	V_{CC} = 5VDC	
Transition Time	t_{THL}	40 30	80 60	120 85	245 180	ns ns	5 10	$V_{CC} = V_{DD}$	
	t_{TLH}	20 15	30 25	60 45	90 75	ns ns	5 10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

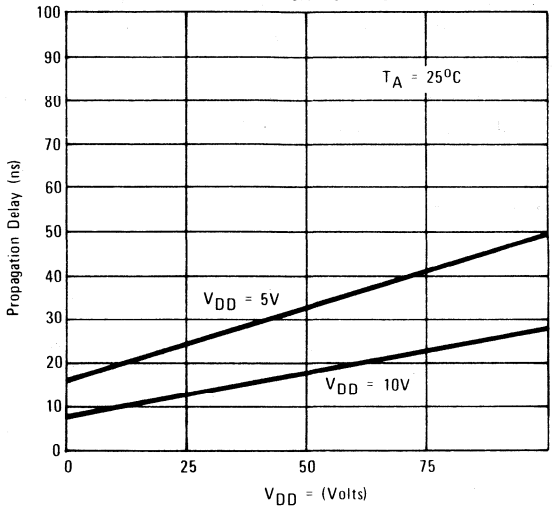
DIGITAL DATA

TYPICAL CHARACTERTISTICS

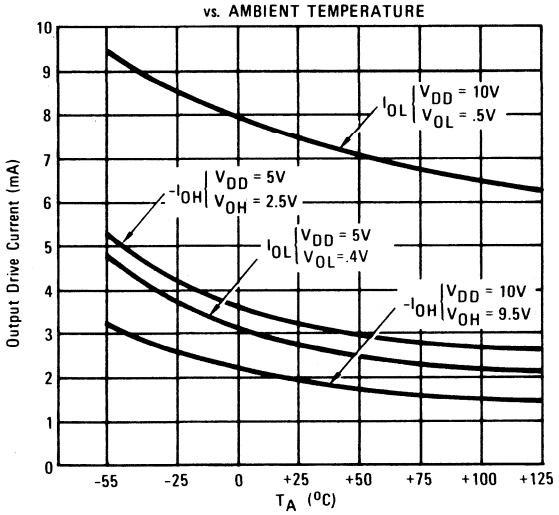
TYPICAL PROPAGATION DELAY
vs. SUPPLY VOLTAGE



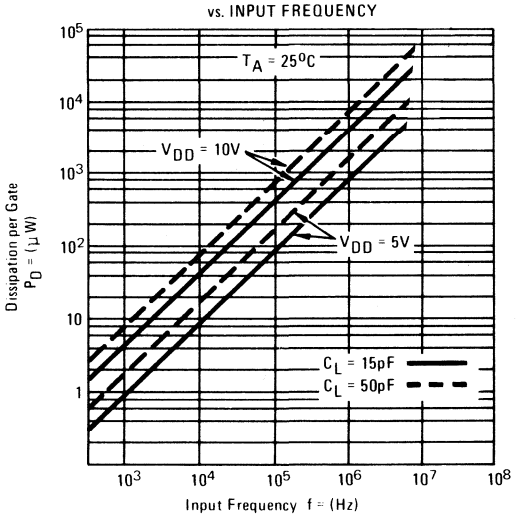
TYPICAL PROPAGATION DELAY
vs. LOAD CAPACITANCE



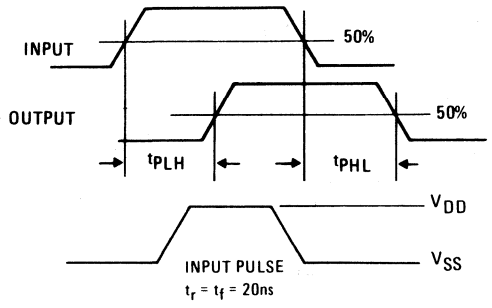
TYPICAL OUTPUT DRIVE CURRENT
vs. AMBIENT TEMPERATURE

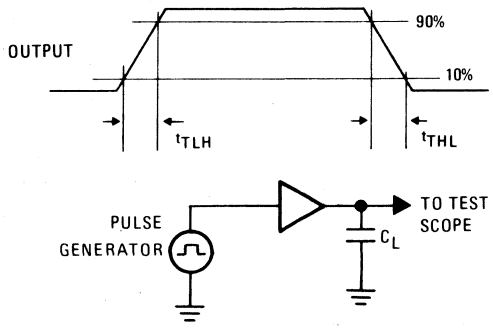


TYPICAL POWER DISSIPATION
vs. INPUT FREQUENCY



SWITCHING TIME DEFINITIONS AND CONDITIONS





HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS

HD-4011

Quad 2-Input 'NAND' Gate

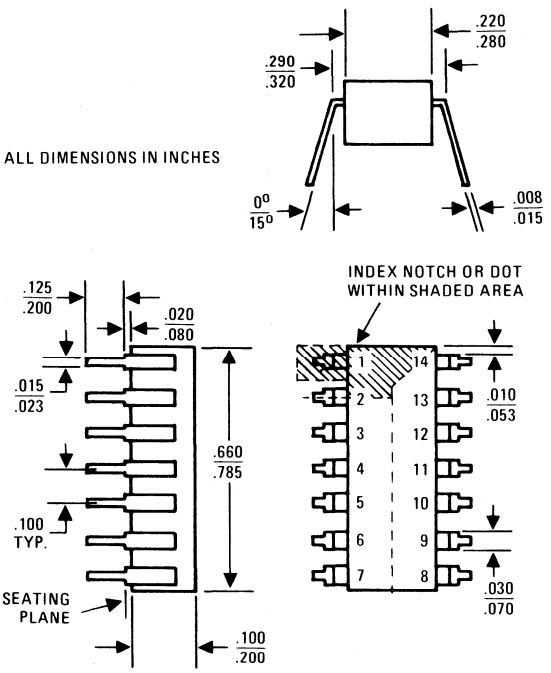
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 1nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- ONLY ONE POWER SUPPLY REQUIRED
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

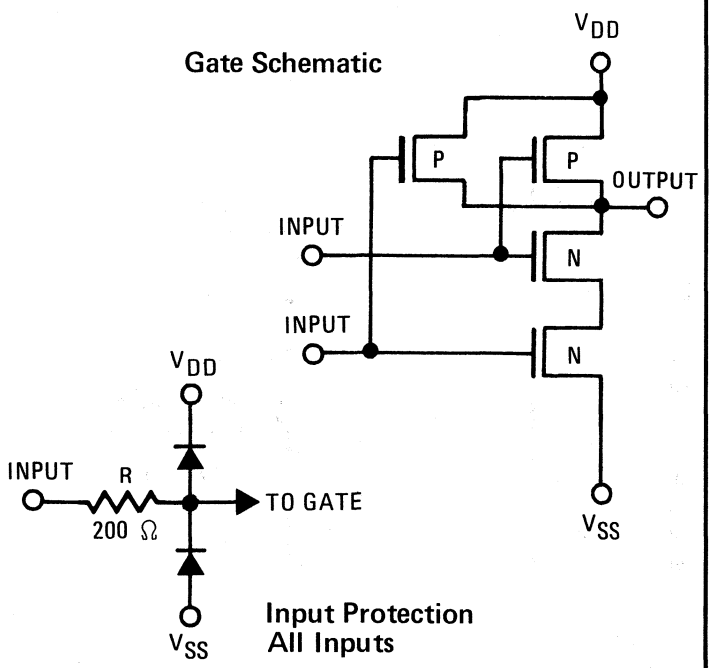
DESCRIPTION

The HD-4011 Quad 2-Input NAND Gate is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris low capacitance Dielectric Isolation process. The HD-4011 is designed for high speed applications which require extremely low power dissipation and good noise immunity. The wide supply voltage range provides considerable power supply flexibility. Pin equivalent to CD-4011A.

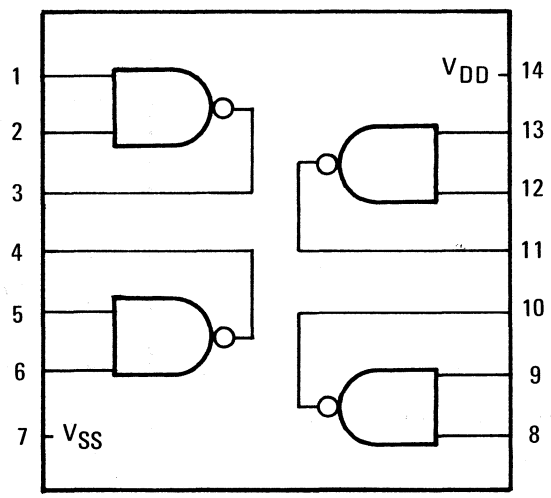
PACKAGE



CIRCUIT DIAGRAMS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}	-0.5VDC to +18VDC
Input Voltage Range, (All Inputs) V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	.31 .62			.25 .50	.5 1.0		.175 .35			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.31 -.75			-.25 -.60	-.5 -1.2		-.175 -.40			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		.05 .10			.05 .10	50 100			300 600	nA nA	5 10	
Input Capacitance						7					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	25 10	40 20	40 20	80 50	ns ns	5 10	Ref. To Switching Time Definitions T_A = 25°C
	t_{PHL}	25 10	40 20	40 20	80 50	ns ns	5 10	
Transition Time	t_{TLH}	35 20	70 40	100 35	150 70	ns ns	5 10	
	t_{THL}	30 15	60 30	100 35	150 70	ns ns	5 10	

NOTE: 1 V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level that the circuit will withstand before producing an output state change.

DIGITAL DATA

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	-40°C MIN.	-40°C TYP.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	.145 .3			.12 .25	.5 1.0		.095 .2			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.095 -.25			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		5 5			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						7					pF		

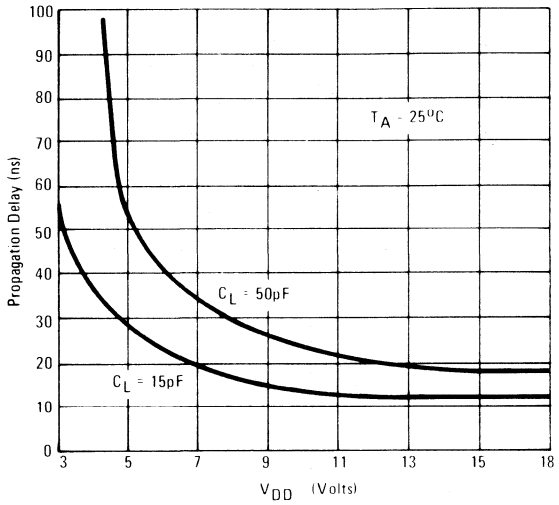
A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	30 12	50 25	45 25	150 75	ns ns	5 10	Ref. To Switching Time Definitions T_A = 25°C
	t_{PHL}	30 12	50 25	45 25	150 75	ns ns	5 10	
Transition Time	t_{TLH}	40 25	85 50	120 40	250 150	ns ns	5 10	
	t_{THL}	35 18	75 40	120 40	225 120	ns ns	5 10	

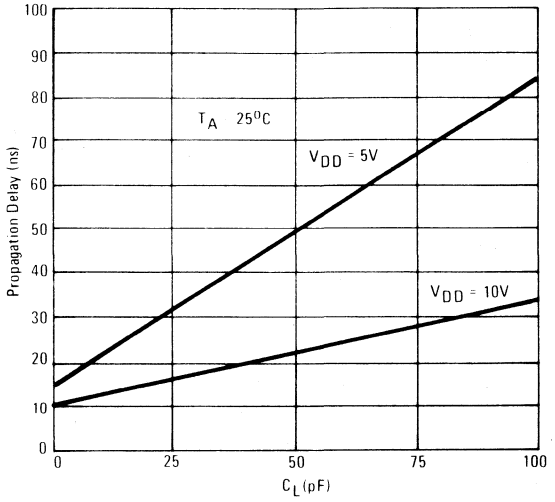
NOTE: 1 V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal '1' or '0' input level that the circuit will withstand before producing an output state change.

TYPICAL CHARACTERISTICS

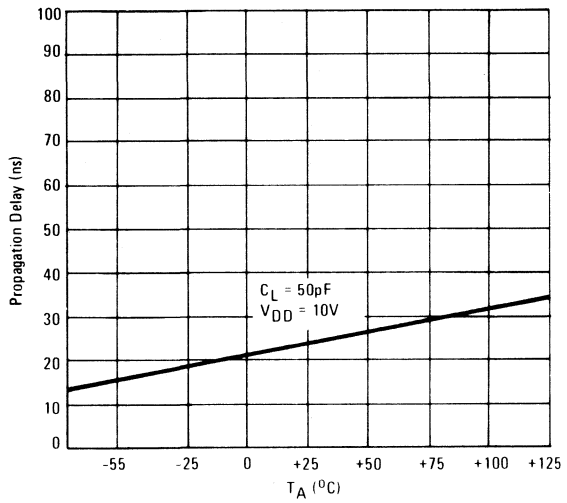
TYPICAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



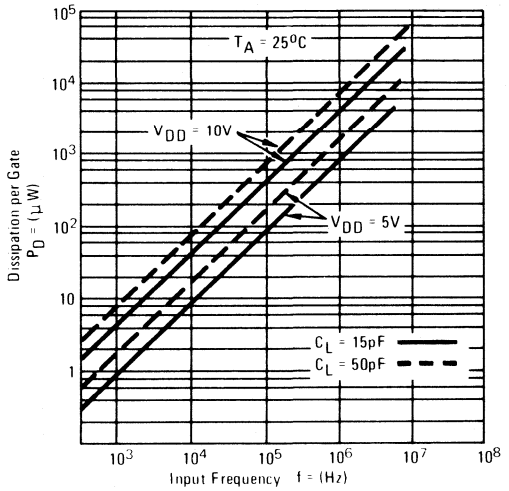
TYPICAL PROPAGATION DELAY vs. LOAD CAPACITANCE



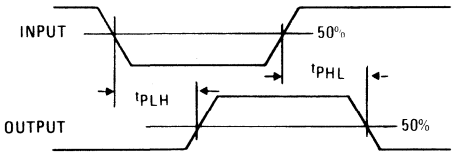
TYPICAL PROPAGATION DELAY vs. AMBIENT TEMPERATURE

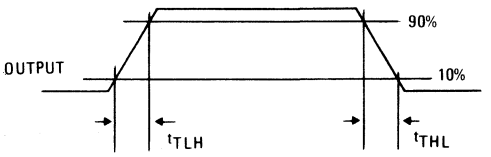


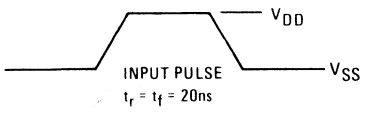
TYPICAL POWER DISSIPATION vs. INPUT FREQUENCY

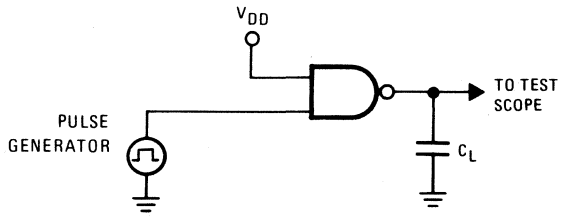


SWITCHING TIME DEFINITIONS AND CONDITIONS









HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS
HD-4012
Dual 4-Input 'NAND' Gate

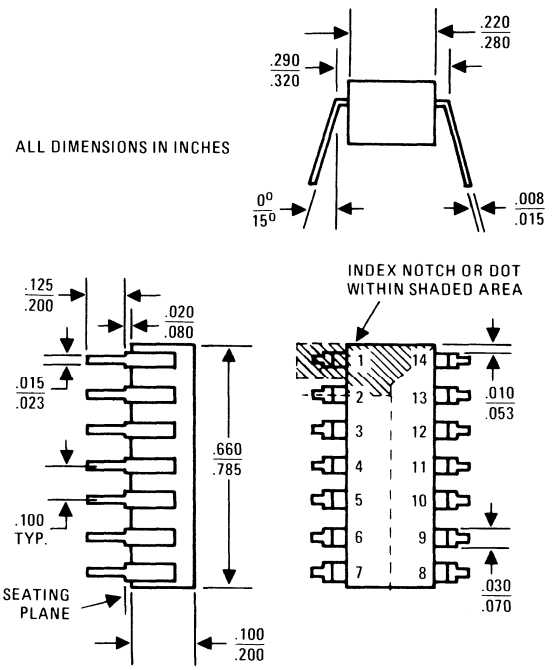
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 1nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- ONLY ONE POWER SUPPLY REQUIRED
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

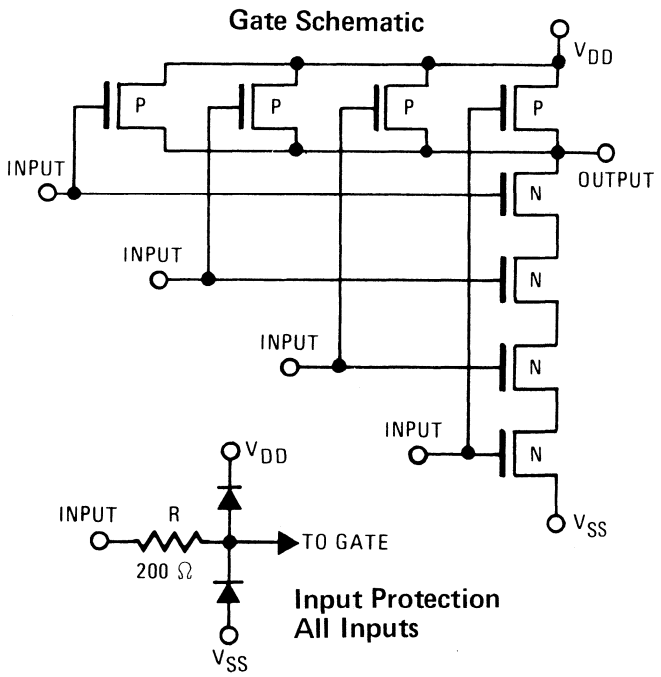
DESCRIPTION

The HD-4012 Quad 4-Input 'NAND' Gate is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris low capacitance Dielectric Isolation process. The HD-4012 is designed for high speed applications which require extremely low power dissipation and good noise immunity. The wide supply voltage range provides considerable power supply flexibility. Pin equivalent to CD-4012A

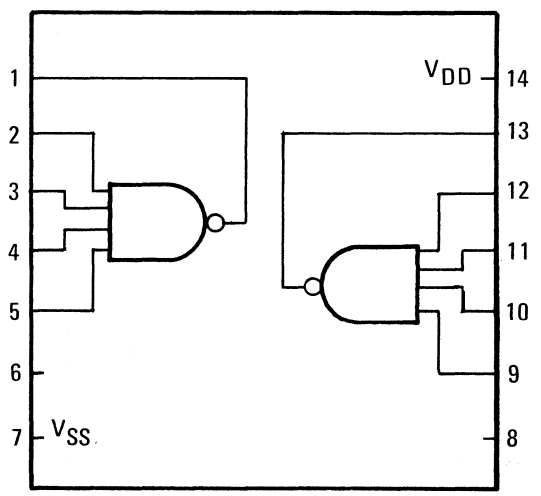
PACKAGE



CIRCUIT DIAGRAMS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} -V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq 3.5$VDC $V_{OH} \geq 7.0$VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq 1.5$VDC $V_{OL} \leq 3.0$VDC
Output Drive Current	I_{OL}	.31 .62			.25 .50	.5 1.0		.175 .35			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.31 -.75			-.25 -.60	-.5 -1.2		-.175 -.40			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		.05 .10			.05 .10	50 100			300 600	nA nA	5 10	
Input Capacitance						7					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	25 10	40 20	40 20	80 50	ns ns	5 10	Ref. To Switching Time Definitions T_A = 25°C
	t_{PHL}	25 10	40 20	40 20	80 50	ns ns	5 10	
Transition Time	t_{TLH}	35 20	70 40	100 35	150 70	ns ns	5 10	
	t_{THL}	30 15	60 30	100 35	150 70	ns ns	5 10	

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} -V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} +0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

D.C.

PARAMETER	SYM.	-40°C MIN.	-40°C TYP.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$, All other inputs = V_{DD}
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$, All other inputs = V_{SS}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V	5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V	5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	.145 .3			.12 .25	.5 1.0		.095 .2			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.145 -.35			-.12 -.3	-.5 -1.2		-.095 -.25			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{DD}		5 5			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						7					pF		

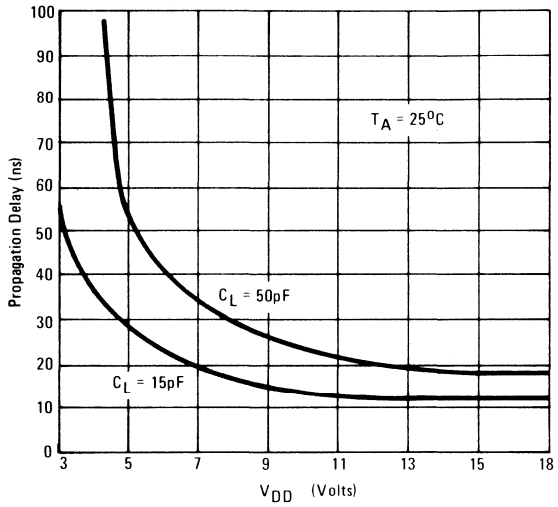
A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES
Propagation Delay	t_{PLH}	30 12	50 25	45 25	150 75	ns ns	5 10	Ref. To Switching Time Definitions T_A = 25°C
	t_{PHL}	30 12	50 25	45 25	150 75	ns ns	5 10	
Transition Time	t_{TLH}	40 25	85 50	120 40	250 150	ns ns	5 10	
	t_{THL}	35 18	75 40	120 40	225 120	ns ns	5 10	

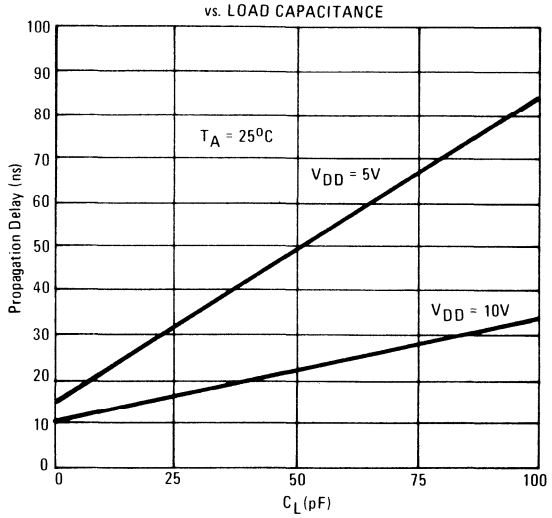
NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

TYPICAL CHARACTERISTICS

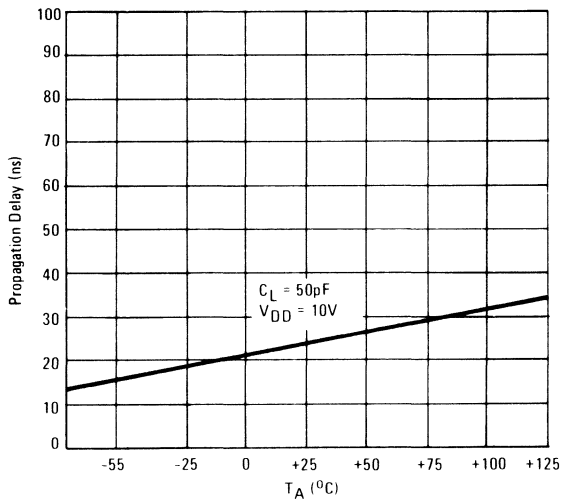
TYPICAL PROPAGATION DELAY
vs. SUPPLY VOLTAGE



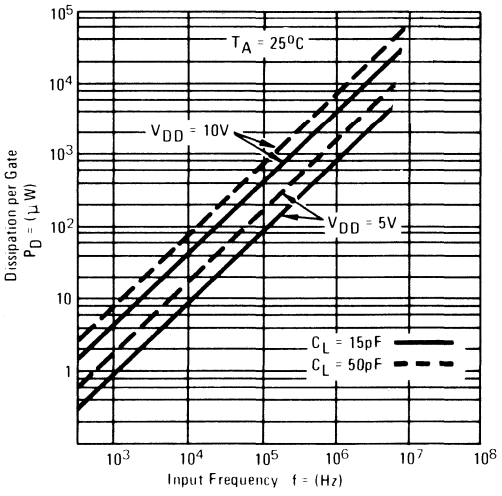
TYPICAL PROPAGATION DELAY
vs. LOAD CAPACITANCE



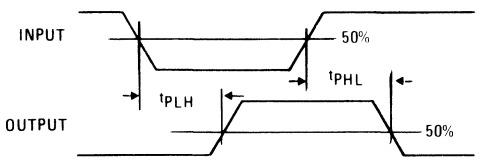
TYPICAL PROPAGATION DELAY
vs. AMBIENT TEMPERATURE

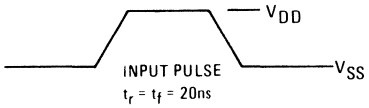


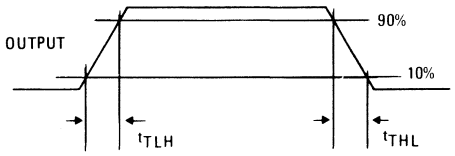
TYPICAL POWER DISSIPATION
vs. INPUT FREQUENCY

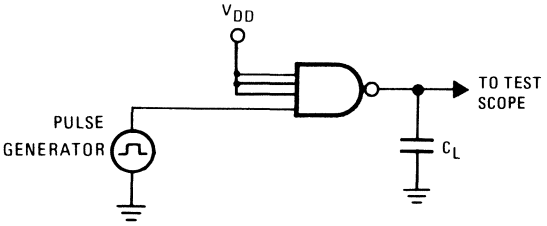


SWITCHING TIME DEFINITIONS AND CONDITIONS









HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS
HD-4013
Dual 'D' Flip Flop

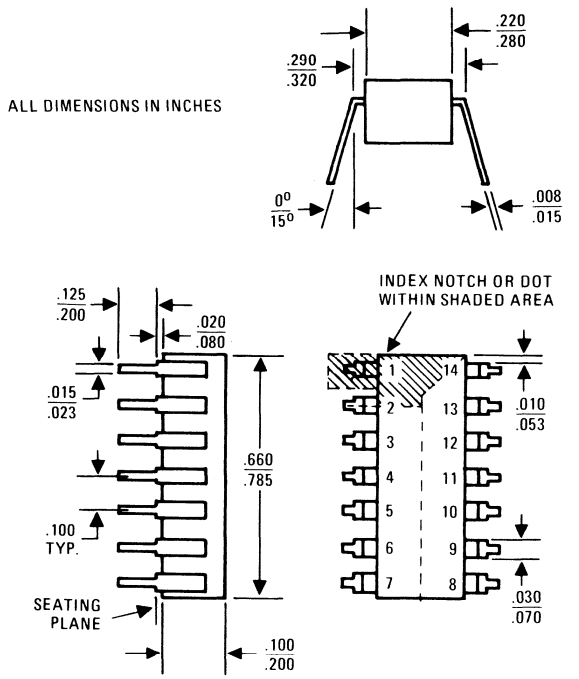
FEATURES

- HIGH SPEED 18MHz TYPICAL TOGGLE RATE
- VERY LOW POWER 50nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- ONLY ONE POWER SUPPLY REQUIRED
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

DESCRIPTION

The HD-4013 Dual D Flip Flop is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris Low Capacitance Dielectric Isolation process. The HD-4013 is designed as a Static Master Slave Flip Flop that is triggered only on the positive transition of the clock pulse. Pin equivalent to CD-4013A.

PACKAGE

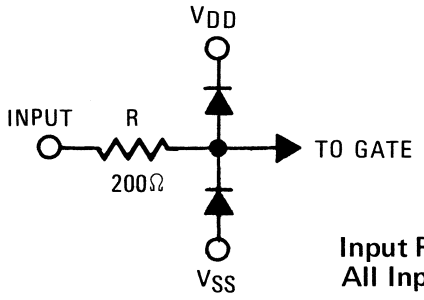


CIRCUIT DIAGRAM & TRUTH TABLE

Truth Table

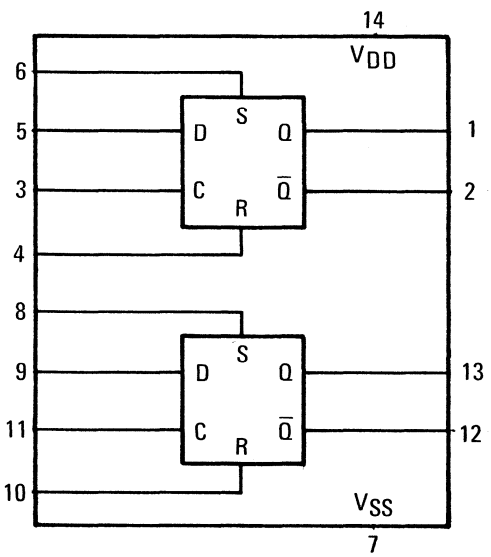
X = Don't Care
Z = Invalid

D	S	R	Qn	Qn+1
0	0	0	0	0
0	0	0	1	0
1	0	0	0	1
1	0	0	1	1
X	1	0	1	1
X	0	1	0	0
X	1	1	Z	Z



Input Protection
All Inputs

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

DC

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$
Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5			1.5	2.25		1.4			V	5	$V_{OH} \geq 3.5VDC$
		3.0			3.0	4.5		2.9			V	10	$V_{OH} \geq 7.0VDC$
	V_{NH}	1.4			1.5	2.25		1.5			V	5	$V_{OL} \leq 1.5VDC$
		2.9			3.0	4.5		3.0			V	10	$V_{OL} \leq 3.0VDC$
Noise Immunity Set, Reset Inputs See Note 1	V_{NL}	1.2			1.2			1.1			V	5	$V_{OH} \geq 3.5VDC$
		1.2			1.2			1.1			V	10	$V_{OH} \geq 7.0VDC$
	V_{NH}	1.5			1.5			1.5			V	5	$V_{OL} \leq 1.5VDC$
		3.0			3.0			3.0			V	10	$V_{OL} \leq 3.0VDC$
Quiescent Power Supply Current	I_{DD}		10			10	100			600	nA	5	S = R = C =
			15			15	150			900	nA	10	D = V_{SS}
Output Drive Current	I_{OL}	.65			.5	1.0		.35			mA	5	V_{OL} = .5VDC
		1.25			1.0	2.0		.75			mA	10	V_{OL} = .5VDC
	I_{OH}	-.31			-.25	- .5		-.175			mA	5	V_{OH} = 4.5VDC
		-.8			-.65	-1.3		-.45			mA	10	V_{OH} = 9.5VDC
Input Capacitance						6					pF		

AC

PARAMETER	SYMBOL	C_L = 15pF MIN.	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF MIN.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES	
Propagation Delay Clock to Q	$t_{PLH} = t_{PHL}$		90	150		175	300	ns	5	S = R = V_{SS}	T_A = 25°C
			30	55		60	110	ns	10		
Transition Time	$t_{TLH} = t_{THL}$		50	70		95	125	ns	5		
			25	40		50	75	ns	10		
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		55	100		70	150	ns	5		
			25	35		30	50	ns	10		
Maximum Clock Rise, Fall Time	$t_{TLH} = t_{THL}$	15			15			μs	5		
		5			5			μs	10		
Set Up Time	$t_{SLH} = t_{SHL}$		10	20		10	20	ns	5		
			0	10		0	10	ns	10		
Maximum Clock Frequency	f_{CL}	5	9		3	7		MHz	5		
		14	18		10	15		MHz	10		
Propagation Delay Set, Reset	$t_{PHL} = t_{PLH}$		60	150		100	300	ns	5	D = C = V_{SS}	
			25	55		40	110	ns	10		
Minimum Set, Reset Pulse Width	$t_{WH(S)} =$ $t_{WH(R)}$		50	100		50	100	ns	5		
			25	35		25	35	ns	10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{DD} = +3VDC to +15VDC, V_{SS} = 0VDC

ELECTRICAL CHARACTERISTICS

DC

PARAMETER	SYM.	−40°C MIN.	−40°C TYP.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	$V_{IL} = V_{SS}$
	I_{IH}		10			10			20		pA	10	$V_{IH} = V_{DD}$
Noise Immunity Clock, Data Inputs See Note 1	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V	5 10	$V_{OH} \geq 3.5$VDC $V_{OH} \geq 7.0$VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V	5 10	$V_{OL} \leq 1.5$VDC $V_{OL} \leq 3.0$VDC
Noise Immunity Set, Reset Inputs See Note 1	V_{NL}	1.2 1.2			1.2 1.2			1.1 1.1			V V	5 10	$V_{OH} \geq 3.5$VDC $V_{OH} \geq 7.0$VDC
	V_{NH}	1.5 3.0			1.5 3.0			1.5 3.0			V V	5 10	$V_{OL} \leq 1.5$VDC $V_{OL} \leq 3.0$VDC
Quiescent Power Supply Current	I_{DD}		25 50			25 50	500 1000		100 200		nA nA	5 10	S = R = C= D = V_{SS}
Output Drive Current	I_{OL}	.35 .72			.30 .60	.90 2.4		.24 .50			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-.17 -.40			-.14 -.33	-.42 -1.0		-.065 -.27			mA mA	5 10	V_{OH} = 4.5VDC V_{OH} = 9.5VDC
Input Capacitance						6					pF		

AC

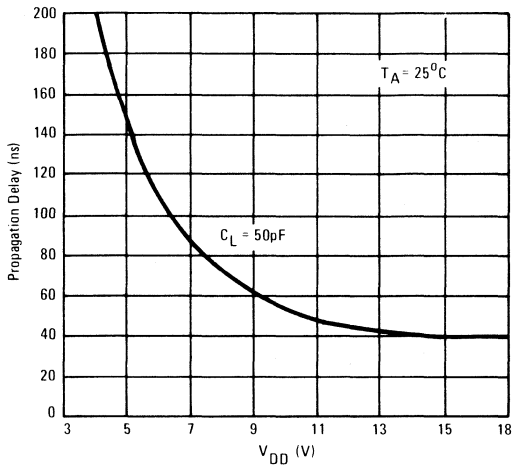
PARAMETER	SYMBOL	C_L = 15pF MIN.	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF MIN.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES	
Propagation Delay Clock to Q	$t_{PLH} = t_{PHL}$		110	180		225	400	ns	5	S = R = V_{SS}	T_A = 25°C
			40	70		80	145	ns	10		
Transition Time	$t_{TLH} = t_{THL}$		60	85		125	165	ns	5		
			30	50		65	100	ns	10		
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		100	200		165	330	ns	5		
			55	70		70	100	ns	10		
Maximum Clock Rise, Fall Time	$t_{TLH}=t_{THL}$	15			15			µs	5		
		5			5			µs	10		
Set Up Time	$t_{SLH} = t_{SHL}$		20	40		20	40	ns	5		
			10	20		10	20	ns	10		
Maximum Clock Frequency	f_{CL}	2.5	5		1.5	3		MHz	5		
		7	9		5	7		MHz	10		
Propagation Delay Set, Reset	$t_{PHL} = t_{PLH}$		80	180		125	400	ns	5	D = C = V_{SS}	
			30	70		65	145	ns	10		
Minimum Set, Reset Pulse Width	$t_{WH(S)}$ =			100			120	ns	5		
	$t_{WH(R)}$			45			45	ns	10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

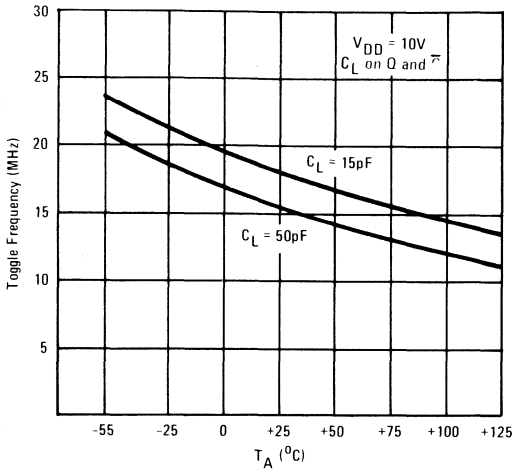
DIGITAL DATA

TYPICAL CHARACTISTICS

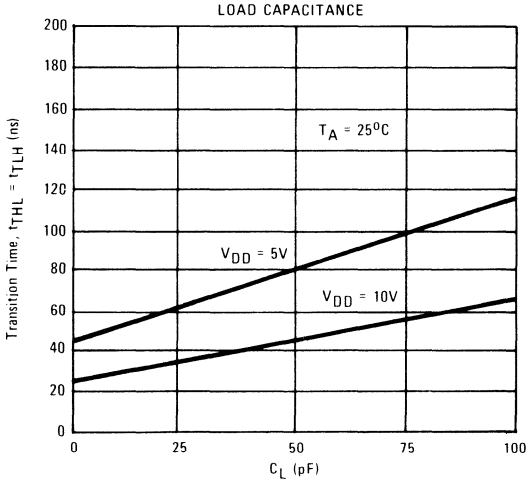
TYPICAL PROPAGATION DELAY
CLOCK TO OUTPUT vs. SUPPLY VOLTAGE



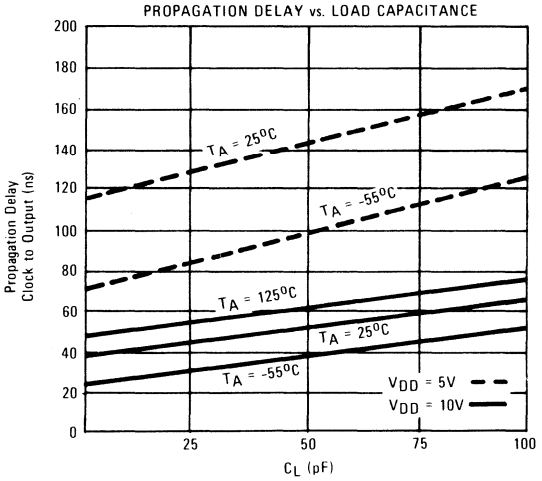
TYPICAL
TOGGLE FREQUENCY vs. AMBIENT TEMPERATURE



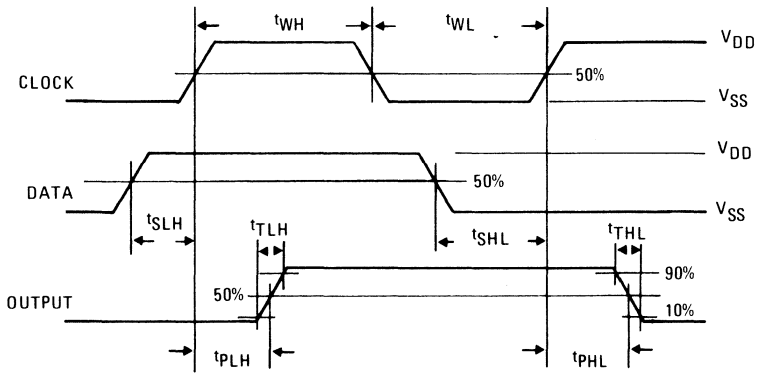
TYPICAL TRANSITION TIMES vs.
LOAD CAPACITANCE

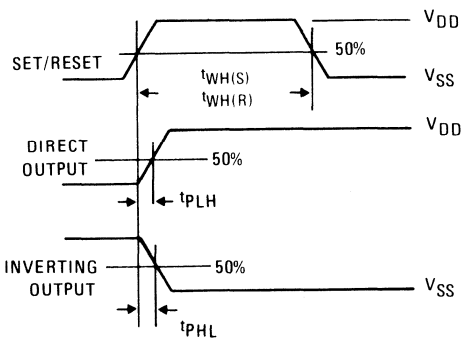


TYPICAL
PROPAGATION DELAY vs. LOAD CAPACITANCE



SWITCHING TIME DEFINITIONS AND CONDITIONS





HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DI/CMOS

HD-4809

Triple True/Complement Buffer

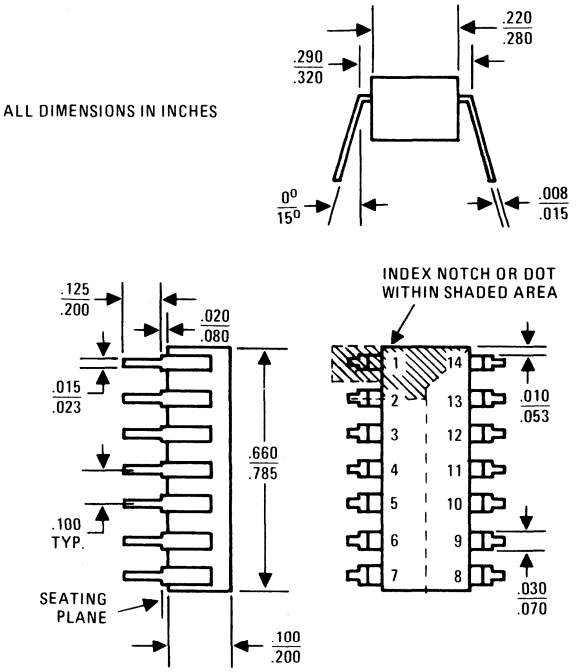
FEATURES

- HIGH SPEED 10ns TYPICAL PROPAGATION DELAY
- VERY LOW POWER 50nW TYPICAL
- WIDE POWER SUPPLY VOLTAGE RANGE 3VDC TO 18VDC
- LARGE NOISE IMMUNITY TYPICALLY 45% OF SUPPLY VOLTAGE
- INPUT DIODE PROTECTION AGAINST STATIC CHARGE
- DIELECTRICALLY ISOLATED COMPLEMENTARY MOS

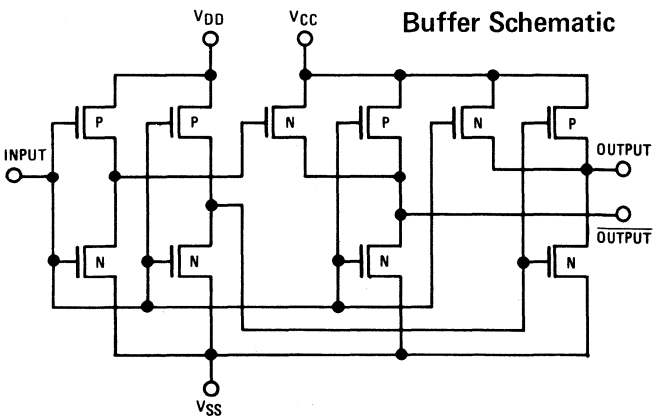
DESCRIPTION

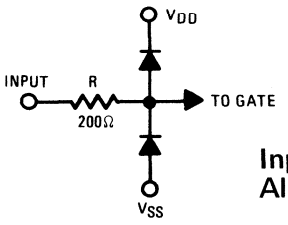
The HD-4809 Triple True/Complement Buffer is constructed with the Harris Dielectric Isolation, complementary MOS process. The very high speeds are obtained by using complementary P-channel and N-channel devices with the Harris Low Capacitance Dielectric Isolation process. The HD-4809 is designed as a triple buffer with true and complement outputs and can be used as drivers for CMOS to CMOS or CMOS to TTL/DTL logic.

PACKAGE



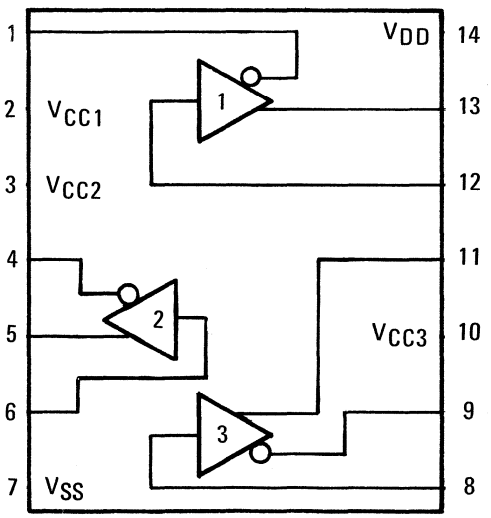
CIRCUIT DIAGRAMS





Input Protection
All Inputs

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS} & V_{CC} - V_{SS}	-0.5VDC to +18VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{CC} = +3VDC to V_{DD}, V_{DD} = +3VDC to +18VDC, V_{SS} = 0VDC (Note 2)

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} UNLESS OTHERWISE SPECIFIED)

D.C.

PARAMETER	SYM.	−55°C MIN.	−55°C TYP.	−55°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	125°C MIN.	125°C TYP.	125°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	V_{IL} = V_{SS}
	I_{IH}		10			10			20		pA	10	V_{IH} = V_{DD}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	3.75 10			3.0 8.0	4 10		2.1 5.6			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-1.85 - .9			-1.25 -.60	-2.0 -1.0		-.9 -.40			mA mA	5 10	V_{OH} = 2.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{SS}		10 15			10 15	100 150			600 900	nA nA	5 10	
Input Capacitance						11					pF		

A.C.

PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES	
Propagation Delay	t_{PLH}	20 15	40 25	45 25	80 50	ns ns	5 10	V_{CC} = V_{DD}	T_A = 25°C
		10	20	20	35	ns	10	V_{CC} = 5VDC	
	t_{PHL}	15 10	25 15	25 10	50 30	ns ns	5 10	V_{CC} = V_{DD}	
		10	15	15	25	ns	10	V_{CC} = 5VDC	
Transition Time	t_{THL}	15 10	25 20	30 15	45 35	ns ns	5 10	OUTPUT 1,4,9 V_{CC} = V_{DD}	
	t_{TLH}	40 25	65 50	70 55	125 100	ns ns	5 10		
	t_{THL}	40 25	65 50	70 55	125 100	ns ns	5 10	OUTPUT 5,11,13 V_{CC} = V_{DD}	
	t_{TLH}	15 10	25 20	30 15	45 35	ns ns	5 10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.
2. V_{CC1}, V_{CC2}, V_{CC3} Need not be equal to each other.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_{DD} - V_{SS} & V_{CC} - V_{SS}	-0.5VDC to +15VDC
Input Voltage Range (All Inputs), V_{IN}	V_{SS} -0.5VDC to V_{DD} + 0.5VDC
Storage Temp. Range	-65°C to +150°C

RECOMMENDED OPERATING VOLTAGE RANGE

V_{CC} = +3VDC to V_{DD}, V_{DD} = +3VDC to +15VDC, V_{SS} = 0VDC (Note 2)

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} UNLESS OTHERWISE SPECIFIED)

D.C.

PARAMETER	SYM.	−40°C MIN.	−40°C TYP.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C TYP.	85°C MAX.	UNITS	CONDITIONS V_{DD}	CONDITIONS NOTES
Input Leakage	I_{IL}		10			10			20		pA	10	V_{IL} = V_{SS}
	I_{IH}		10			10			20		pA	10	V_{IH} = V_{DD}
Noise Immunity (Note 1)	V_{NL}	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9				5 10	$V_{OH} \geq$ 3.5VDC $V_{OH} \geq$ 7.0VDC
	V_{NH}	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0				5 10	$V_{OL} \leq$ 1.5VDC $V_{OL} \leq$ 3.0VDC
Output Drive Current	I_{OL}	3.6 9.6			3.0 8.0	4 10		2.4 6.4			mA mA	5 10	V_{OL} = .5VDC V_{OL} = .5VDC
	I_{OH}	-1.5 -.72			-1.25 -.60	-1.75 -.80		-1.0 -.48			mA mA	5 10	V_{OH} = 2.5VDC V_{OH} = 9.5VDC
Quiescent Power Supply Current	I_{SS}		10 15			25 50	500 1000		100 200		nA nA	5 10	
Input Capacitance						11					pF		

A.C.

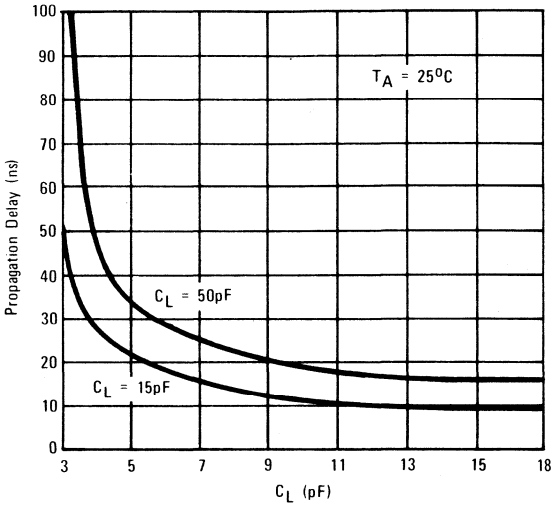
PARAMETER	SYMBOL	C_L = 15pF TYP.	C_L = 15pF MAX.	C_L = 50pF TYP.	C_L = 50pF MAX.	UNITS	V_{DD}	NOTES	
Propagation Delay	t_{PLH}	25 20	50 30	75 60	150 90	ns ns	5 10	V_{CC} = V_{DD}	T_A = 25°C
		15	25	40	75	ns	10	V_{CC} = 5VDC	
	t_{PHL}	20 15	30 20	60 45	90 60	ns ns	5 10	V_{CC} = V_{DD}	
		15	20	30	60	ns	10	V_{CC} = 5VDC	
Transition Time	t_{THL}	20 15	30 25	60 45	90 75	ns ns	5 10	OUTPUT 1,4,9 V_{CC} = V_{DD}	
	t_{TLH}	40 30	80 60	120 85	245 180	ns ns	5 10		
	t_{THL}	40 30	80 60	120 85	245 180	ns ns	5 10	OUTPUT 5,11,13 V_{CC} = V_{DD}	
	t_{TLH}	20 15	30 25	60 45	90 75	ns ns	5 10		

NOTE: 1. V_{NH}, V_{NL} is defined as the maximum voltage change from an ideal "1" or "0" input level that the circuit will withstand before producing an output state change.

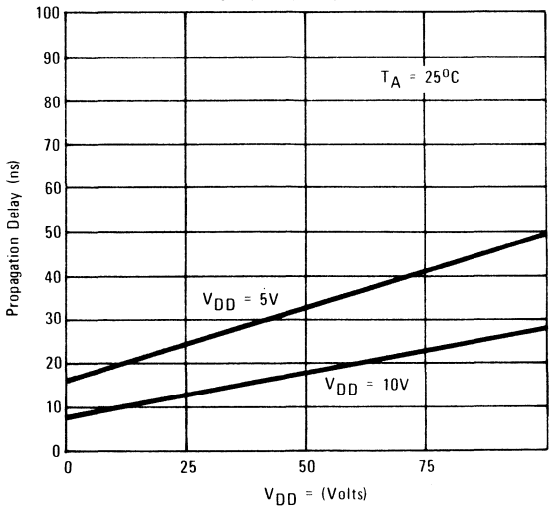
2. V_{CC1}, V_{CC2}, V_{CC3} Need not be equal to each other.

TYPICAL CHARACTERISTICS

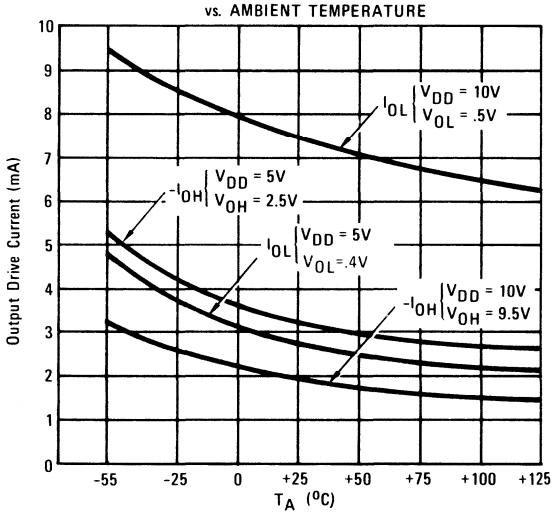
TYPICAL PROPAGATION DELAY
vs. SUPPLY VOLTAGE



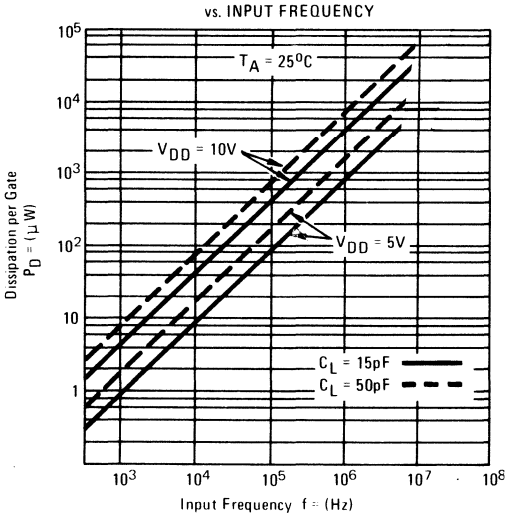
TYPICAL PROPAGATION DELAY
vs. LOAD CAPACITANCE



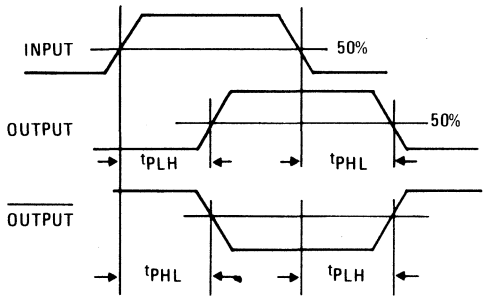
TYPICAL OUTPUT DRIVE CURRENT
vs. AMBIENT TEMPERATURE

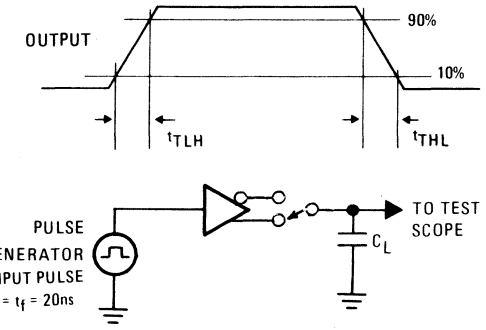


TYPICAL POWER DISSIPATION
vs. INPUT FREQUENCY



SWITCH TIME DEFINITIONS AND CONDITIONS





HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 207

RECEIVER/TRANSMITTER NOISE IMMUNITY

BY DON JONES &
GEORGE MILER, JR.

INTRODUCTION

This paper is intended to answer many questions which have arisen about the noise immunity of Harris Semiconductor's HD-245 family digital line transmitter/receiver system relative to other systems.

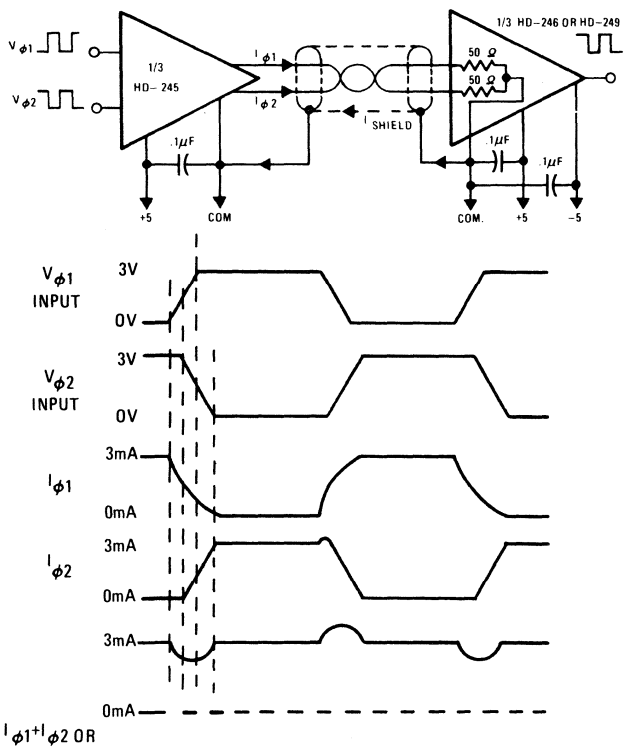


Figure 1- Harris Current Mode System

Shown in Figure 1 is the operation of the HD-245/249 system. First, line $\phi 1$ conducts a current of about 3mA which travels down the line through one of the 50Ω terminating resistors in the receiver and returns through the transmission line shield to the transmitter power supply common. Then, the current on line $\phi 1$ shuts off and line $\phi 2$ conducts current which is also returned through the shield. The shield essentially carries the same DC current since lines $\phi 1$ and $\phi 2$ alternate in conduction. There may be small variations in the transmission line current if both transmitter inputs are high or low simultaneously during the data transition times. The important fact concerning noise immunity is that this is essentially a three conductor transmission system, and in most instances, externally generated noise affects all three conductors.

The noise which can affect a digital line transmission system includes several types:

1. Magnetic and capacitive pickup from other electrical conductors in the near proximity to the transmission line.
2. Magnetic and capacitive crosstalk between transmission lines sharing a common shield.
3. Ground line noise between the transmitter and receiver.

All of these types of noise will be considered in this discussion.

EXTERNAL MAGNETIC EFFECTS

Changing magnetic lines of force from an adjacent AC power line which intersect the digital transmission line will induce a voltage difference between the transmitter and receiver. The induced voltage will be equal and of the same polarity on the two signal lines and return line at any point. Even though large excursions can be measured between the transmitter and receiver ground points, this has no effect on the digital transmission quality. To the transmitter and to the re-

ceiver, their respective ends of the transmission line appear normal since they have not shifted with respect to ground at that end of the line.

This has been verified experimentally by winding a transmission line around a ferrite core to form a pulse transformer secondary. When a primary winding was connected to a pulse generator (0 to 20MHz, 20V Peak) no adverse effects could be noted on a receiver output (Figure 2).

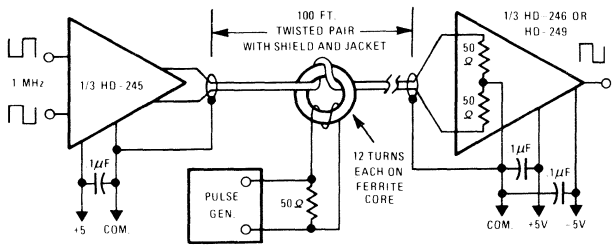


Figure 2- External Magnetic Field

The effect of a ground loop outside the magnetic circuit is only to reduce the coupled noise. For maximum immunity, the power supplies should be filtered by 0.1μF or larger capacitors to the common lines at the transmitter and receiver pins.

EXTERNAL CAPACITIVE EFFECT

The effect of capacitive coupling of AC signals from adjacent conductors is to tend to produce noise with respect to ground on both signal lines which is uniform along the length of the line. Here, a shield on the transmission line is highly effective in preventing adverse effects. The foil type shields, in addition to being less expensive, give more perfect protection than braided wire types.

The ability to reject capacitively coupled noise has also been verified experimentally as shown in Figure 3. Power supply filtering is again essential. No erroneous receiver output was noted.

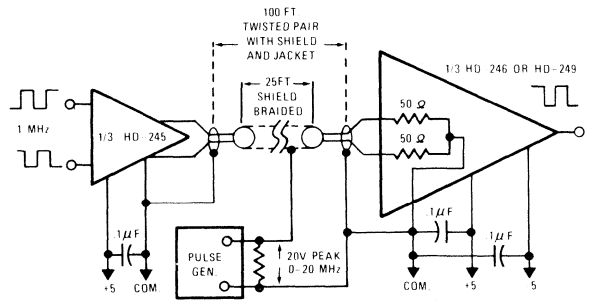


Figure 3- External Capacitive Field

CROSSTALK

It is possible to contain a number of individual twisted-pair transmission lines within a single overall shield. Perfectly balanced signals on a twisted pair will produce an unchanging magnetic and electric field which will not couple to other lines. The delay between the complementary inputs to the transmitter must be small compared with the transition times of the transmitter inputs to minimize the small current pulses during switching. The HD-245 transmitter worstcase current unbalance is guaranteed so that it is possible to enclose more than 15 twisted pairs without exceeding the common mode range of a receiver even if 14 of the pairs should switch at the same instant. Power lines, single ended signal lines, or high level twisted pair signal lines should not be enclosed in the same shield.

GROUND LINE NOISE

In systems where transmission line shields are the only connections between the transmitter and receiver power supplies, interference from noise currents on the shield will be negligible, since the only current on the shield will be signal return current and the system can withstand noise up to 2V peak. If severe ground loop currents are present, for example, if both transmitter and receiver power supply commons are connected to different points on a noisy AC power line ground, interference can be encountered. The best solution is to remove the ground loop and use DC power supplies which are well isolated from the AC line.

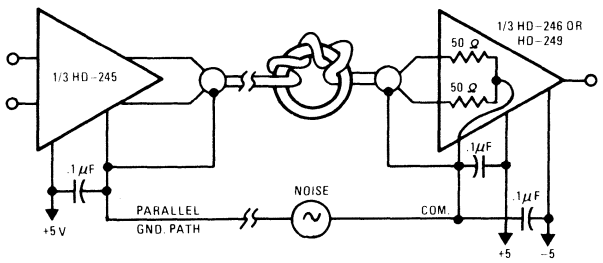


Figure 4 - Ground Line Noise

Another effective solution is to wind a portion of each transmission line around a magnetic core to form a balun transformer as shown in Figure 4. Flux produced by the signal currents and the shield return cancel one another, so the signal remains unaffected. Ground loop current produces a flux in the core so that the current is reduced by the inductance and by core losses. Thus, the coils form a low impedance to signals but a high impedance to noise.

This transmitter/receiver system is unaffected by ground differentials as long as the receiver ground is between 3V positive and 25V negative with respect to the transmitter V_{CC}. Therefore, large low frequency ground noises can be tolerated as well as large ground error signals.

Precautions should be taken to minimize ground differentials between the line termination and the HD-248 party line receiver. For best performance, the inputs of the party line receiver should remain within ±0.5V of the HD-248 ground.

OTHER TRANSMISSION SYSTEMS

A popular low speed transmission system which conforms with EIA Standard No. RS-232C is shown in Figure 5. This standard was established for low speed local digital communications.

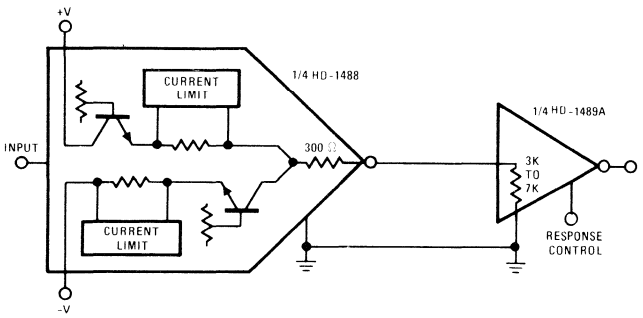


Figure 5- EIA STD. RS-232C Data System

RS-232C specifies that the output of the transmitter swings between +6V and −6V while the receiver thresholds are between +0.8V and +2V. This is a simple system to implement, requiring only one signal line and a common ground return. Shielded or twisted transmission lines are generally not used with this system and several communications circuits can share the same ground return. A terminated transmission line is not practical with this system because it is designed to operate with an impedance of between 3KΩ and 7KΩ.

Since the Harris HD-1488 transmitter and the HD-1489A receiver system is designed for the low data rates implied in RS-232C, the transmitter can be filtered to minimize the noise and oscillations which are normally generated by a voltage mode transmitter. Due to the short circuit current limiting in the HD-1488, it is possible to limit the slew rate of the transmitter to approximately 30V per microsecond by placing a 330pF capacitor from the output to ground.

The noise pickup is minimized by the moderate receiver input impedance. The HD-1489A receiver is able to reject several volts of noise because of the large hysteresis and the large voltage difference between the transmitter output and the receiver thresholds.

Another popular high speed transmission system is the differential voltage switching type shown below in Figure 6.

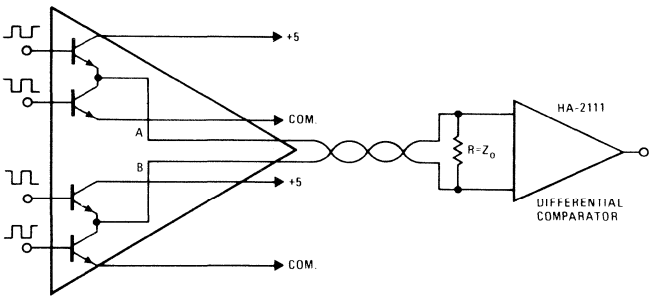


Figure 6- Differential Voltage Switching

First, line A is connected to +5V and current flows through the terminating resistor to line B which is connected to common. Then, the current is reversed for the next half cycle.

In the absence of noise, no ground return or shield is required; however, shielding is definitely necessary in any practical system.

In an unshielded environment, the receiver must have a high common mode noise rejection, and some systems boast the ability to reject common mode noise up to ±15V. Common mode currents cannot return to ground through the terminating resistor, but must travel through the high impedance receiver input. Therefore, very little induced noise power is required to exceed the common mode voltage range of the receiver, and an unshielded line could not be used in the vicinity of AC power lines, teletypewriter lines, etc., carrying signals over 15V peak.

Also, the voltage switching type transmitter is often a source of noise. Ringing resulting from high speed low impedance switching will be present on the lines. Most transmitters have diode clamps to reduce ringing, but it still may exceed 1VRMS which would make an unshielded line a strong source of radiated RF interference.

The "totem pole" transmitter output will draw sharp current spikes from the power supply, since at the instant of switching, the formerly saturated transistor will turn off slower than the other transistor turns on, creating a power supply short circuit for a few nanoseconds. This requires very drastic power

supply decoupling at the transmitter to prevent interference with other circuitry, and the transmitter will dissipate increasing amounts of power at high signal frequencies. The current spikes also often couple to the signal line creating additional differential and common mode noise. Obviously, the use of shielded transmission lines is usually a necessity in this type of system.

CONCLUSION

A comparison of noise rejection of the three types of systems, Harris' current switching type (HD-245), RS-232C voltage mode (HD-1488) and the differential voltage switching types, are given below for various noise sources:

1. Externally generated magnetic and capacitive coupled noise: Using shielded line, which is generally necessary for other reasons, the three system types should reject noise equally well.

2. Crosstalk between lines: In Harris' current switching system, parameters which can cause crosstalk (current unbalance) are well defined. Spikes and ringing on the lines are negligible. Operation of more than 15 twisted pair lines in a single shield without mutual interference is assured.

   Crosstalk between a few lines can be eliminated in the RS-232C system by filtering the transmitter. However, this severely limits the maximum data rate.

   In differential voltage switching type systems, caution should be taken when using more than one line pair in a single shield, because spikes and ringing will be significant and are not easily predicted.

3. Ground line noise: The current switching type and the RS-232C type systems are not as good as the differential voltage type in this respect, but the problem can be avoided by eliminating noisy ground loops as dictated by standard system design practices.

4. Self-generated noise: The current switching type system is far superior in generating lower levels of conducted and radiated RF interference. The signal swings on the line are 20 times smaller. The non-saturating current switching transmitter generates smooth ramps without overshoot or ringing. Power supply lines are free of current spikes and power drain is constant with signal frequency.

   The noise generated by the differential and the RS-232C voltage mode types can be greatly reduced by filtering if high data rates are not required.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 205

HIGH SPEED DIGITAL COMMUNICATIONS

BY G. G. MILER

INTRODUCTION

The use of high speed digital communications is rapidly increasing. This is partially due to the FCC decision to allow competition in data communications as well as the great increase in the use of computers with data communications capability. The use of management information systems is expected to continue to grow at a rapid rate. This will result in increased usage of sophisticated data collection systems , as well as the increased usage of remote data entry terminals and display systems.

There are several general classes of digital communications systems discussed in this application note. Low and moderate speed local digital systems are defined by EIA Standard RS-232. This type of system is intended for local (less than 100 feet) communications between the computer system and the long distance communications system interface (modem). Modems are generally required for long distance (greater than 10 miles) digital communications systems. Coaxial lines and microwave links are generally required for high speed, long distance data communications systems. Another general class of digital communications which is rapidly growing is that used for communications within a company. Distances of up to several thousand feet are generally required for high speed communications between a data acquisition, system, or process control system and the central computer system.

VOLTAGE MODE TRANSMISSION

Data rates of up to 10 million bits per second can be obtained with standard TTL logic; however, the transmission distance must be very short. For example, a typical 50 foot low capacitance cable will have a capacitance of approximately 750pF which requires a current of greater than 50mA to drive 5V into this cable at 10MHz; therefore, voltage mode transmitters are undesirable for long transmission lines at high data rates due to the large current required to charge the transmission line capacitance.

CURRENT MODE TRANSMISSION

An alternate method of driving high data rates down long transmission lines is to use a current mode transmitter. Current mode logic changes the current in a low impedance transmission line and requires very little change in voltage. For example, a 2mA change in transmitter current will produce a 100mV change in receiver voltage independent of the series transmission line resistance. The rise time at the receiver for a typical 50 foot cable (750pF) is approximately 30ns for a 2mA pulse.

An emitter coupled logic gate is frequently used for a current mode transmitter. However, ECL gates are not compatible with TTL and DTL logic and they require considerable power. The Harris Semiconductor HD-245/545 is a TTL/DTL compatible current mode transmitter designed for high data rates on long transmission lines. Data rates of 15 megabits per second can be obtained with 50 feet of transmission line when using the companion HD-246/546 or HD-249/549 receiver. Data rates of 2 megabits per second are easily obtained on transmission lines as

long as 1,000 feet. The Harris transmitter and receivers feature very low power, typically 25mW for the transmitter and 15mW for the receiver.

HARRIS TRANSMITTER/RECEIVERS

The Harris transmitter/receiver family consists of a triple line transmitter, two triple line receivers with internal terminations and a triple party-line receiver. The general characteristics of the transmitter and receivers are outlined in Table I.

Triple Line Transmitter

PARAMETER	HD-245	HD-545	UNITS	COMMENTS
Operating Temp. Range	-55 to +125	0 to +75	^{o}C	
"ON" Output Current	2.0 MIN	1.8 MIN	mA	Over full temp. range
Power Supply Current	6.2 MAX	8.0 MAX	mA	Per transmitter section
Standby Current	33 MAX	33 MAX	µA	Per transmitter section
Propagation Delay	10 MAX	10 MAX	ns	25^{o}C

Triple Line Receiver

PARAMETER	RECEIVER TYPE	LIMITS	UNITS	COMMENTS
Operating Temp Range	HD-246/248/249	-55 to+125	^{o}C	
Power Supply I_{CC} (V_{CC}=+5.0V)	HD-246/248/249	2.2	mA	Per receiver section
	HD-546/548/549	2.5	mA	With Output High
Propagation Delay	All Receivers	30	ns	25^{o}C
Input Impedance and Output Circuit	HD-246/546	$\frac{\text{Input}}{100}$	Ohm	$\frac{\text{Output}}{\text{Open Collector}}$
	HD-248/548	Hi-Z		6K Pull-up Resistor
	HD-249/549	100	Ohm	6K Pull-up Resistor

Table I. General Transmitter/Receiver Characteristics

TRANSMITTER

The HD-245/545 transmitters have two inputs per transmitter, either of which is low while the other is open during normal operation and both inputs are open during stand-by. For optimum transmitter performance, the "off" input should be open circuit rather than being pulled towards +5V, because this will reduce the "on" output data current. On the other hand, the "on" and "off" output data current will be increased if the "off" input is held below its open circuit voltage. Open collector gates such as the 7401 and 7403 or 7405 Hex-Inverter are suitable for driving the HD-245/545 transmitter inputs. By using 2-input gates as shown in Figure 1, an enable line can be provided so that more than one transmitter may be connected to a line for time sharing. When the enable line is low the transmitter will be disabled and will present a high impedance to the transmission line as well as requiring very little power supply current.

Complementary input signals may be derived from high speed inverter gates as shown, or by using the complementary outputs of a flip-flop. When the transmitter is connected near the midpoint of a long transmission line or to a line with terminations at both ends, two transmitter sections should be paralleled with respective inputs and outputs connected together in order to drive the reduced impedance. This parallel transmitter technique can also be used to increase the data rate on long transmission lines.

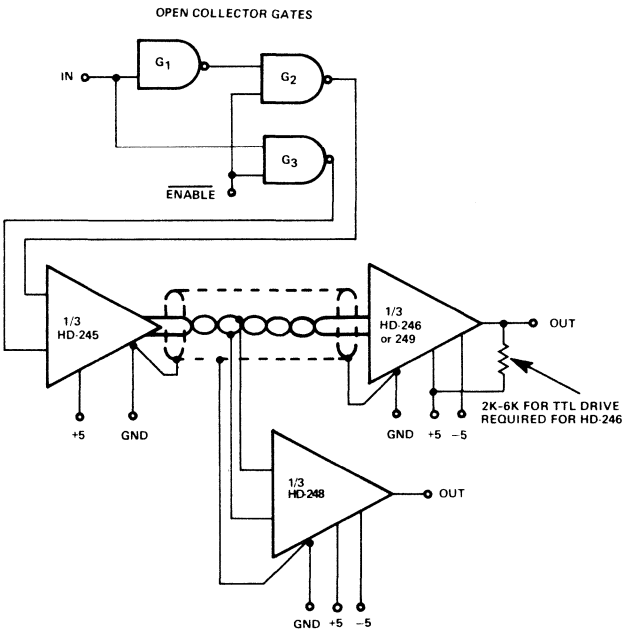


Figure I. Typical Data Transmission System

TRANSMITTER OPERATION

The transmitter alternately applies the current to each of the two conductors in the twisted pair line such that the total current in the twisted pair is constant and always in the same direction. This current flows through either of the two 50 ohm terminating resistors at the receiver and returns to the transmitter as a steady D.C. current on the transmission line shield. The D.C. power supply return for the transmitter is through the receiver terminating resistors (the transmitter

ground pin is only a substrate ground). Therefore, it is essential that the shield be connected to the power supply common at both the transmitter and receiver, preferably at the integrated circuit "ground" pin. More than fifteen twisted pair lines can share the the same shield without crosstalk.

RECEIVERS

The HD-248/548 "party-line" receiver presents a high impedance load to the transmission line allowing as many as ten HD-248/548 receivers to be distributed along a line without excessive loading. Figure 1 shows a typical system of a transmitter, a terminating receiver and a party-line receiver. The transmission line is terminated in its characteristics impedance by an HD-246/546, HD-249/549, or by a pair of 50 ohm resistors connecting each line to the ground return shield.

TRANSMISSION LINES

The maximum frequency (or minimum pulse width) which can be carried by a certain length of a given transmission line is dependent on the loss characteristics of the particular line. At low frequencies, there will be virtually no loss in pulse amplitude, but there will be a degradation of rise and fall-time which is roughly proportional to the square of the line length. This is shown in Figure 2. If the pulse width is less than the rise-time at the receiver end, the pulse amplitude will be diminished, approaching the point where it cannot be detected by the receiver.

The transmission line used with the Harris HD-245/545 series transmitter and receivers can be any ordinary shielded, twisted pair line with a characteristic impedance of 100 ohms. Twisted pair lines consisting of number 20 or 22 guage wire will generally have this characteristic impedance. Special high quality transmission lines are not necessary and standard audio, shielded-twisted pair, cable is generally suitable.

Since the necessary characteristics for various twisted pair lines are not readily available, it may be necessary to take some measurements on a length of the proposed line. To do this, connect an HD-245/545 transmitter to one end of the line (100 feet or more) and an HD-246/546 or an HD-249/549 receiver to the other end. The rise and fall-times can be measured on the line at both ends and the constant "K", for that line can be computed as shown in Figure 2 so that the minimum pulse width can be determined for any length of line.

Data rates of 2MHz have been obtained using 1,000 feet of standard shielded, twisted pair, audio cable. Data rates of 15MHz are possible on shorter lengths of transmission line (50 feet).

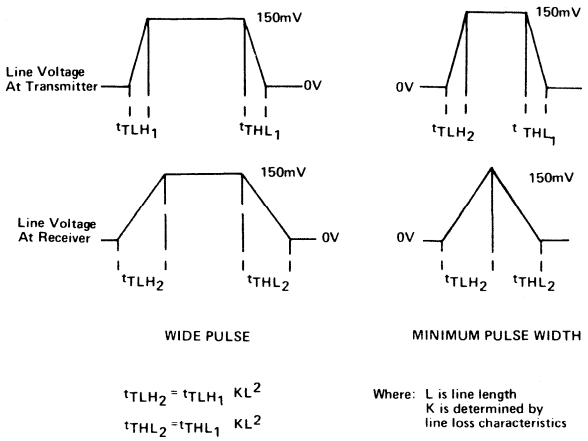


Figure 2. Transmission Line Wave-Shaping

ELECTROMAGNETIC INTERFERENCE

Very little electromagnetic interference is generated by the Harris current mode system because the total current through the twisted pair is constant, while the current through the shield is also constant and in the opposite direction. This can be verified by observing, with a current probe, the total current through the twisted pair, through the shield and through the complete shielded, twisted pair cable. In each case a constant current will be observed with only small variations. Small pulses may be observed if the complementary inputs to the transmitter do not switch at the same time. The current will decrease during the time both inputs are high, and will increase during the time both inputs are low. These switching pulses may be observed when using the circuit shown in Figure

1. The amplitude and shape of these pulses will depend on the propagation delay of G_1, and transition times of G_2 and G_3. These pulses are generally of no concern because of their small amplitude and width, but they may be reduced by increasing the similarity of the waveforms and timing synchronization of the complementary signals applied to the transmitter.

In addition to generating very little noise, the system is also highly immune to outside noise since it is difficult to capacitively couple a differential signal into the low impedance twisted pair cable and it is even more difficult in induce a differential current into the line due to the very high impedance of the constant current transmitter. Therefore, differential mode interference is generally not a problem with the Harris current mode system. Large common mode voltages can also be tolerated because the output current of the transmitter is constant as long as the receiver termination ground is less than 2V positive with respect to the grounded input of the transmitter, and is less than 25V negative with respect to the transmitter V_{CC}. The current mode system is totally unaffected by ground differential noise of $\pm 2V$ at frequencies as high as 1 MHz.

PROPAGATION DELAY

CHARACTERISTICS	-55°C to +125°C HD-245/246/248/249			0°C to +75°C HD-545/546/548/549			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay T_{PLH}		18	40		18	40	ns
Propagation Delay T_{PHL}		18	40		18	40	ns
Duty Cycle Distortion $T_{PLH} - T_{PHL}$		2	15		4	20	ns

V_{CC}=+5V, V_{EE}= −5V

Table II. Overall Transmitter/Receiver Switching Characteristics

The worst case propagation delay of a transmitter and receiver, connected as shown in Figure 1, can be determined by adding the maximum delay shown on the data sheet for the transmitter and receiver. These overall switching characteristics are shown in Table II.

For the entire system, however, the propagation delay of the transmission line must also be considered. This delay, of course, depends on the length of the line and the characteristics of the line, but in general, delays of between 1.5ns and 3.0ns per foot can be expected.

SUMMARY

The optimum data communications system for very high speed data transfer over long transmission lines is the current mode system. The Harris current mode transmitter/receiver system provides a combination of: the high speed required, excellent noise immunity, low power consumption and very low levels of RFI.

Complex digital communications systems design can be simplified by fully utilizing the unique features of the Harris HD-245 family current mode system.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 204

DESIGNING WITH THE HD-0165 KEYBOARD ENCODER

BY D. F. JONES

The Harris Semiconductor type HD-0165 Keyboard Encoder integrated circuit provides an ideal low cost means of transforming signals from any manual keyboard into a TTL compatible parallel binary code.

CODE IMPLEMENTATION

The organization and truth table for the HD-0165 are shown in Figure 1 and Table 1. Basically, there are sixteen input lines, only one of which is normally connected at a time through the keyboard to the +5V supply. There are four output lines which produce a parallel binary code which is determined by the actuated input lines. The outputs will drive any DTL or TTL circuits with a fanout of six normal loads. The function of the two auxiliary outputs will be explained later.

To produce a certain output code by actuating a particular key, simply look down the output columns (1–4) of the truth table until the desired four-bit code is found; then look across to see which input is high (H) and connect that input pin to the key.

One fact which should be obvious is that since all sixteen possible combinations of four bits are available on the output lines, the numbering system for the input and output lines is arbitrary. The ordering of the truth table arbitrarily shows an ascending negative logic (H=0, L=1) output in binary code with output line 4 the most significant bit. But we do not need to be governed by this. If we want the "zero" key to produce LLLL, we do not need to tie input 1 to that key and put inverter gates in series with the outputs; we can simply tie input 16 to the "zero" key. Similarly, we could wire up a ten button keyboard to yield a 1–2–4–8 BCD code, a 1–2–4–2 BCD code, a 1–2–2–5 code, a Gray code, or any other code up to four bits simply by using the truth table and wiring the inputs to the appropriate keys. Redundant codes can be generated, if desired, by wiring one input line to more than one key.

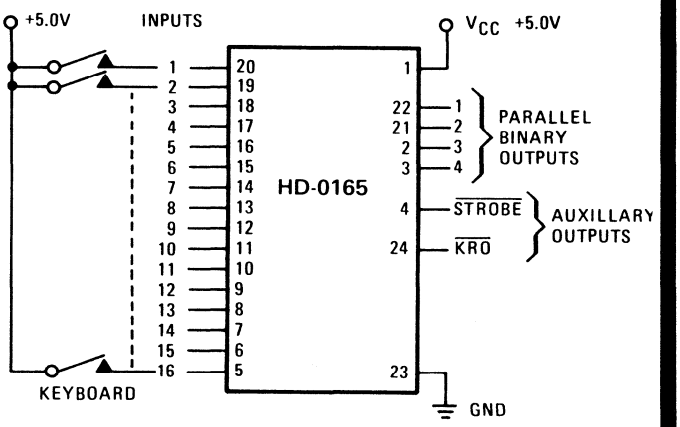


Figure 1. Keyboard Encoder Organization

ENCODING MORE THAN SIXTEEN KEYS

Two keyboard encoder circuits may be used to encode up to 256 keys, represented by eight bits.

The general scheme is to let the outputs from one device represent the four most significant bits and the output from the other device represent the four least significant bits of the output word. Each key is wired to one input on each of the two devices to produce the desired output code.

It is necessary to isolate the two wires from each key, since each device input usually is connected to more than one key. This is accomplished either by using double-pole key switches, or by using two diodes per key in series with the device input lines. The general scheme for cascading two encoders is shown in Figure 2.

APP NOTES

TABLE I
TRUTH TABLE, HD-0165

INPUTS																OUTPUTS					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	St.	K_{RO}
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = > +0.4V H = > +2.4V X = Erroneous Data

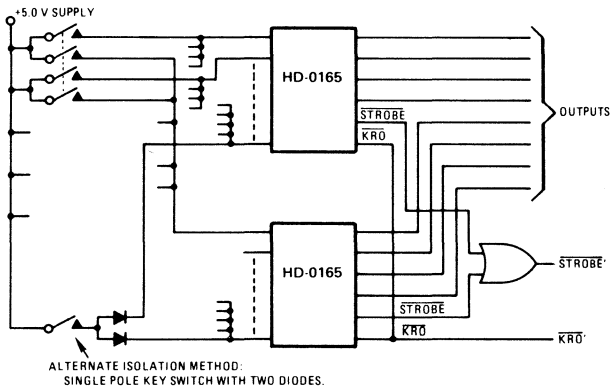


Figure 2

An important fact — when diode input isolation is used the diode forward voltage drop decreases the input current available to the encoder, and the result is that the encoder output fanout should be reduced to two TTL loads. The fanout capability could be restored by returning the keys to a higher voltage (+5.7V to +6.0V). This voltage could be generated by placing a high-current diode between the normal supply regulator output and its sense line, as shown in Figure 3.

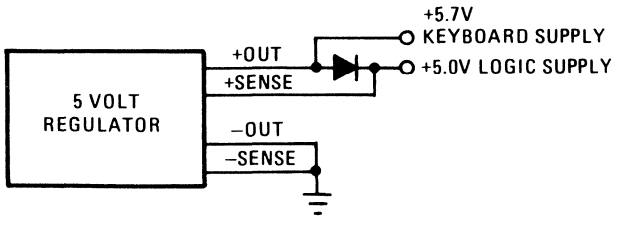


Figure 3

AUXILIARY OUTPUTS

As shown in the truth table, the STROBE output is high if no keys are actuated, and becomes low when any key is actuated. This signal is normally used to gate the encoded signal into other circuitry, and may be conditioned to eliminate any effects of switch bounce or skew in output propagation delays.

The KEY ROLLOVER (K_{RO}) output is normally high, and goes low only when two or more keys are actuated simultaneously. This signals that the output data word is not valid during that time.

Figure 4 illustrates one method of switch bounce surpression which also gives correct data input under key rollover conditions. One dual retriggerable monostable multivibrator device is required per keyboard to suppress multiple strobe pulses resulting from key bounce or arcing on either "make" or "break". With this scheme, there is no necessity for the use of mercury-wetted or other exotic key switches to prevent bounce effects.

The strobe and K_{RO} outputs from one or more encoders are combined at point A; so that the signal at point A is high when any one key is depressed, and low when no key or two or more keys are depressed.

The time delay, T_1, generated by the first monostable must be longer than the worst expected interval between switching spikes —

about 3 to 10 milliseconds is usually sufficient.

The time delay, T_2, generated by the second monostable depends on system requirements – about 0.5 microseconds will result from the values shown.

The waveforms shown at A, B, and C show a typical situation. At interval I, a key is depressed and the first monostable generates a delay, T_1, sufficiently long to allow any switch bounce spikes to die out. At the trailing edge of T_1, the second monostable generates a strobe pulse, T_2, for entering the data into the system. The delayed strobe also assures that the parallel data are stabilized when strobed into the system.

At interval II, a second key is depressed while the first key is not released until interval III. The first monostable might be triggered at this time, but this will not cause an output at C, because the clear (C_D) terminal of the second monostable will be held low. At interval III, when the first key is released, the two monostables will again be triggered, entering the data from the second key into the system.

If noise occurs at interval IV, when the second key is released, no signal will appear at C since C_D will again be low before the trailing edge at B is generated.

For data entry, it is necessary that a key be held down for longer than T_1, but since this interval is only a few milliseconds, it is highly unlikely that any deliberate key depression would be for a shorter interval.

The delayed strobe pulse, S_t, is used to signal the presence of new data to the system. The pulse can be used to gate a latch circuit or, if a serial data format is required, the pulse can be used to enable the parallel loading of a shift register.

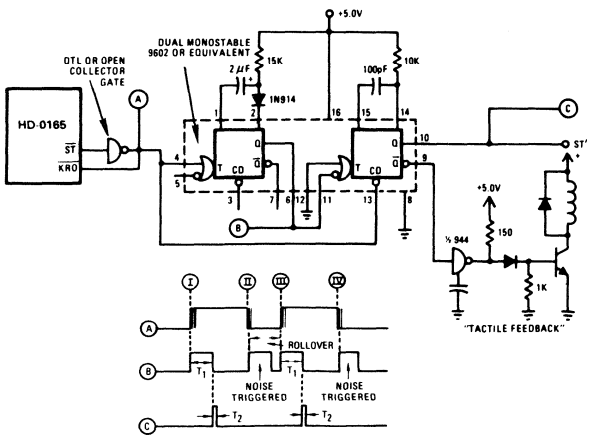


Figure 4. Switch Bounce Elimination

An optional "tactile feedback" circuit is also shown in Figure 4, which for a small increase in cost will greatly increase operator accuracy at high entry speeds. The transistor load is either a small solenoid hammer which taps the keyboard area, or a small loudspeaker which produces an audible "tick" each time data is entered. Since the "tick" only occurs when data entry actually occurs in the system, this scheme will give more accuracy (probably at lower cost) than special "tactile feel" key switches. Actual circuitry will depend on the type of load used. A capacitor is shown at the gate expander terminal to stretch the pulse at this point.

BATTERY OPERATED KEYBOARD

The circuit shown in Figure 5 will help conserve battery life in a portable keyboard. When no key is depressed, the PNP transistor is turned off, and there is no battery drain. When any key is pressed, the input current causes the transistor to turn on, supplying power to the encoder and to any other digital circuitry. The transistor should be capable of switching the necessary current and should have low $V_{CE(Sat)}$ for low power dissipation.

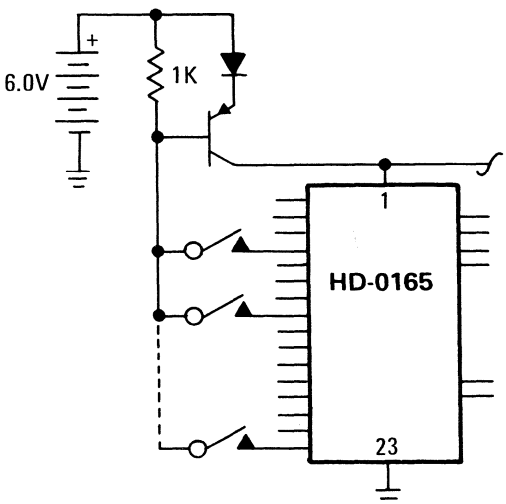


Figure 5. Battery Operated Keyboard

DESIGN EXAMPLE: TELETYPEWRITER KEYBOARD ENCODER

Each keyboard encoding design task must start with an analysis of the code to be produced and the arrangement of the keyboard. A minor complication arises when a single key must produce more than one code; for example when SHIFT and CONTROL keys are used.

As an example we will design a keyboard encoder for a teletypewriter or CRT terminal using the standard ASCII code for capital letters only, plus symbols and control functions.

First, for convenience, using the encoder truth table, we will assign a hexidecimal character to each device input line. The conventions for the output will be: positive logic (L=0, H=1); output line 1 will be the L.S.B., and output line 4 will be the M.S.B. This results in Table II.

Now, we tabulate the desired output words as a two digit hex code (Table III) with the first digit representing the four most significant bits and the second digit representing the four least significant bits. This now gives us the wiring list to correct each key in the normal (unshifted) mode to the two encoder circuits as in Figure 2. Since the hex code for "A" is CI, we can connect the two wires from the "A" key to the C input (Pin 17) of the top encoder and to the 1 input (Pin 6) of the bottom encoder of Figure 2. The rest of the keys are wired similarly for the specified output code in the unshifted state.

TABLE II
HEX CHARACTER ASSIGNMENT

HEX CHARACTER	INPUT LINE	PIN NUMBER
0	16	5
1	15	6
2	14	7
3	13	8
4	12	9
5	11	10
6	10	11
7	9	12
8	8	13
9	7	14
A	6	15
B	5	16
C	4	17
D	3	18
E	2	19
F	1	20

TABLE III
ASCII TELETYPEWRITER CODE

CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX
@	C0	Blank	A0	NULL	80	ACK	FC
A	C1	!	A1	SOH	81	ALT	FD
B	C2	"	A2	STX	82	ESC	FE
C	C3	#	A3	ETX	83	Rubout	FF
D	C4	$	A4	EOT	84		
E	C5	%	A5	WRU	85		
F	C6	&	A6	RU	86		
G	C7	'	A7	BELL	87		
H	C8	(	A8	FE	88		
I	C9	)	A9	HT	89		
J	CA	*	AA	LF	8A		
K	CB	+	AB	VT	8B		
L	CC	,	AC	FF	8C		
M	CD	–	AD	CR	8D		
N	CE	.	AE	SO	8E		
O	CF	/	AF	AI	8F		
P	D0	0	B0	DC0	90		
Q	D1	1	B1	X-ON	91		
R	D2	2	B2	Tape-ON	92		
S	D3	3	B3	X-OFF	93		
T	D4	4	B4	Tape-OFF	94		
U	D5	5	B5	ERR	95		
V	D6	6	B6	SYN	96		
W	D7	7	B7	LEM	97		
X	D8	8	B8	S_0	98		
Y	D9	9	B9	S_1	99		
Z	DA	:	BA	S_2	9A		
[	DB	;	BB	S_3	9B		
\	DC	<	BC	S_4	9C		
]	DD	=	BD	S_5	9D		
↑	DE	>	BE	S_6	9E		
←	DF	?	BF	S_7	9F		

TABLE IV

KEY			ENCODER INPUT	
NORMAL	SHIFT	CONTROL	MSB	LSB
A		SOH	C	1
B		STX	C	2
C		ETX	C	3
D		EOT	C	4
E		WRU	C	5
F		RU	C	6
G		BELL	C	7
H		FE	C	8
I		HT	C	9
J		LF	C	A
K	[	VT	C	B
L	\	FF	C	C
M	]	CR	C	D
N	↑	SO	C	E
O	←	SI	C	F
P	@	NUL	D	0
Q		X-ON	D	1
R		Tape-ON	D	2
S		X-OFF	D	3
T		Tape-OFF	D	4
U		ERR	D	5
V		SYN	D	6
W		LEM	D	7
X		S_0	D	8
Y		S_1	D	9
Z		S_2	D	A

KEY			ENCODER INPUT	
NORMAL	SHIFT	CONTROL	MSB	LSB
1	!		B	1
2	"		B	2
3	#		B	3
4	$		B	4
5	%		B	5
6	&		B	6
7	'		B	7
8	(		B	8
9	)		B	9
0			B	0
:	*		B	A
–	=		A	D
.	>		A	E
,	<		A	C
;	+		B	B
/	?		A	F
Line Feed			8	A
Return			8	D
Rubout			F	F
Space			A	0
ACK			F	C
ALT			F	D
ESC			F	E

For this example, we will design one of the more popular terminal keyboard arrangements as shown in Table IV.

Comparing Table IV with Table III, we note that the L.S.B.'s change in a particular pattern: A → B, B → A, C → D, D → C. Further investigation shows that this is simply an inversion of the fifth output bit. So, we could make the SHIFT key control a group of gates in series with the fifth output bit to pass this bit either inverted or not inverted.

Investigation of the control mode codes shows that bits 6 and 7 must always be "0" when the CONTROL key is depressed, the other bits remaining the same as in the normal mode for that key. This can easily be implemented by connecting DTL gates in "wired-OR" to these outputs. Control functions S_3 through S_7 can be generated by holding both the SHIFT and CONTROL keys down and pressing "L" through "P", respectively; or these could be implemented by additional wiring.

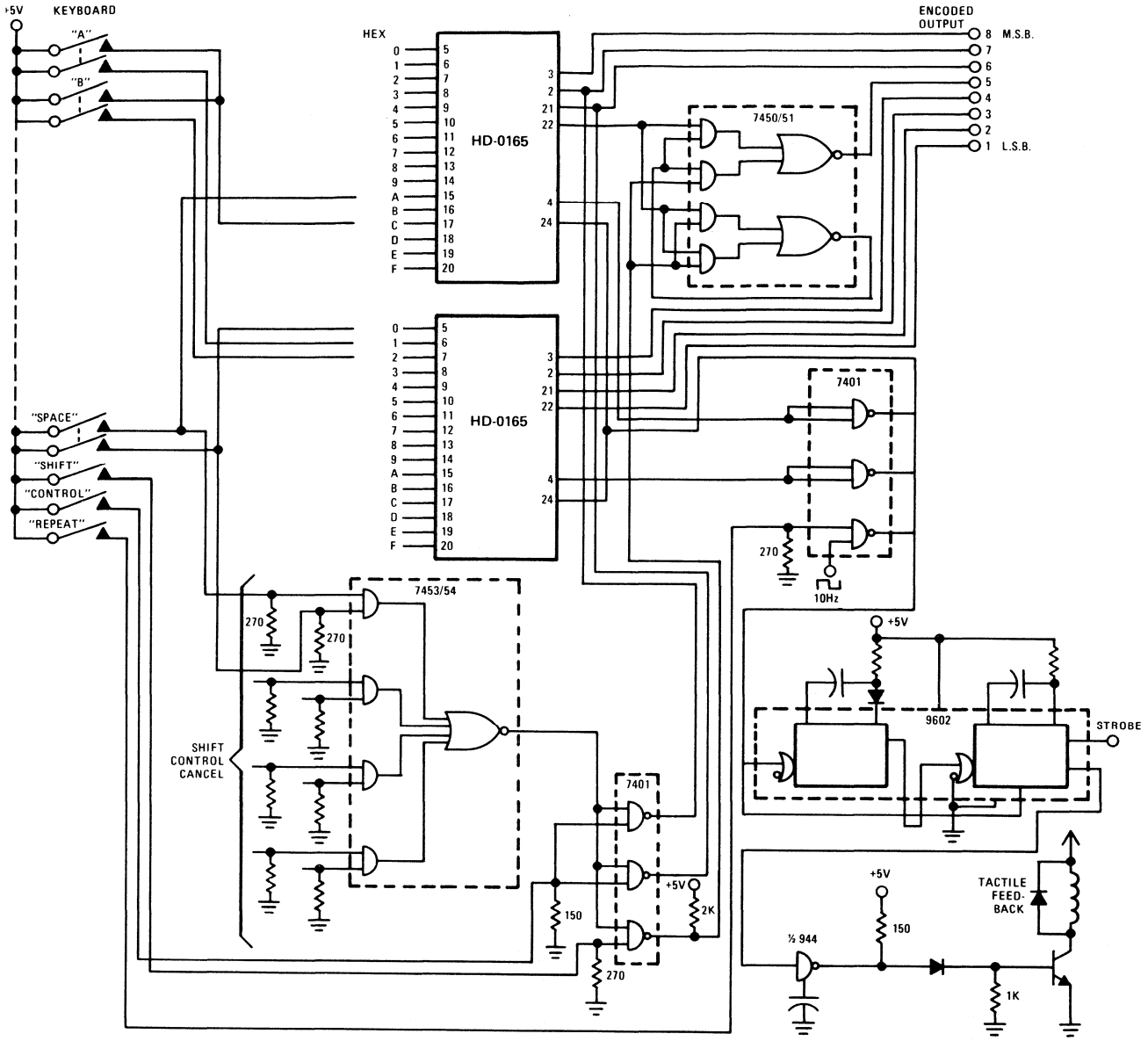


Figure 6. Teletypewriter (ASCII) Encoder

Figure 6 shows the finished design, with the wiring from keys to encoder input indicated in Table IV.

It may be desirable to have some keys, such as the SPACE bar, produce the same output in all three modes. If the "cancel" inputs shown in Figure 6, are wired to those keys, the effect of the SHIFT and CONTROL keys will be nullified for those particular keys.

An optional feature shown is the REPEAT key which pulses the strobe output at about 10cps as long as it and another key are held down.

A full typewriter ASCII keyboard with upper and lower case letters can be implemented in a similar fashion. The "shift" requires inversion of either bit 5 or bit 6 depending on the state of bit 7, so the logic at the output is somewhat more complex.

UNIVERSAL KEYBOARD ENCODER

Suppose we required a keyboard with a code in which there was no simple logical relationships between shifted and unshifted output words—or a keyboard which could produce several entirely different codes at the flip of a switch—or one which could be supplied with any desired code on very short notice. Any of these problems can be readily solved by using keyboard encoder circuits to generate a universal code—which can then be translated to the desired output code using programmable read-only memories.

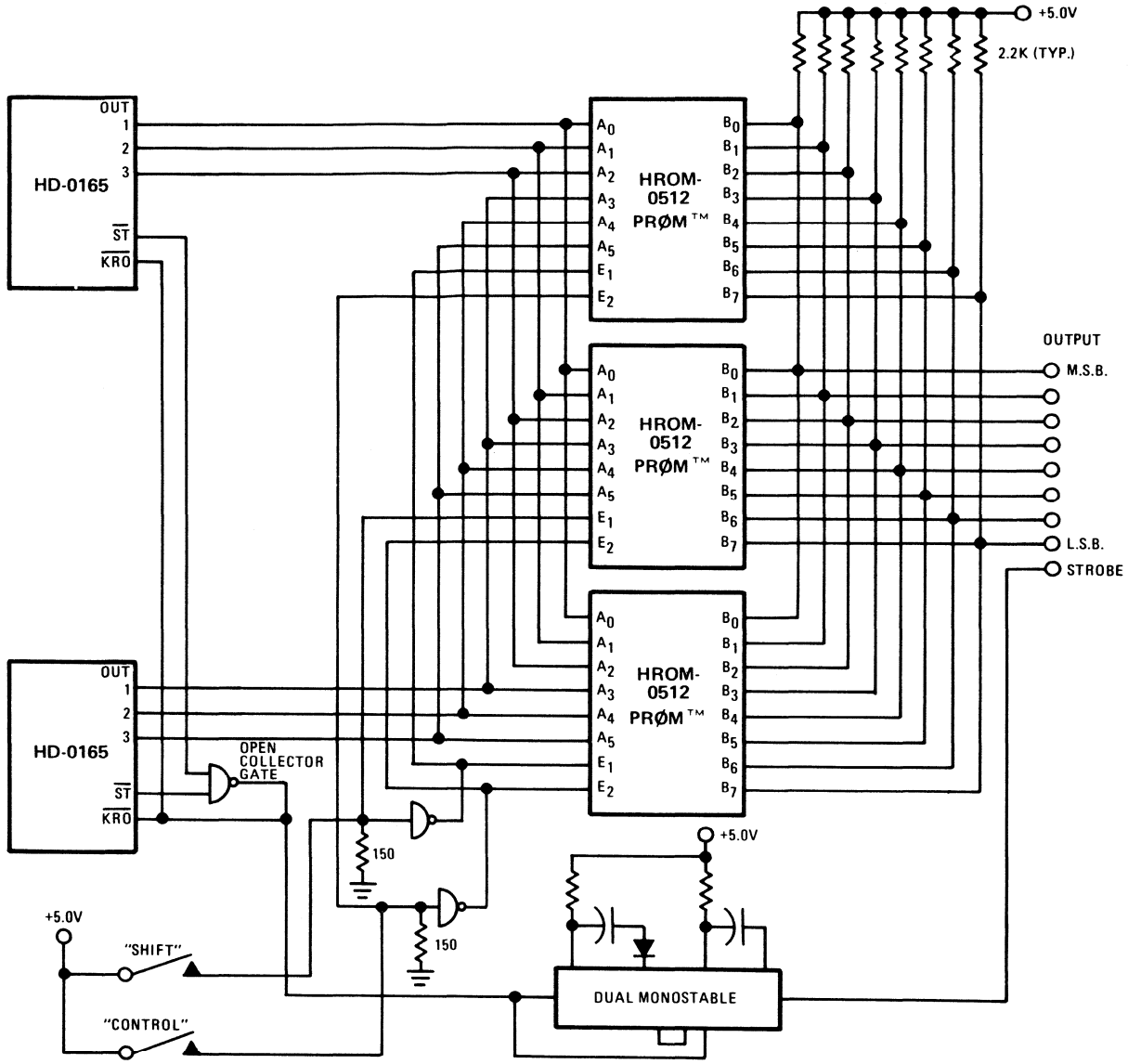


Figure 7. Universal Keyboard Encoder

Figure 7 shows the organization for a universal keyboard encoder. Up to 64 keys are wired to two encoder circuits which produce a six-bit output code (the fourth output bit of each encoder is not used). The key to encoder wiring is arbitrary as long as each key produces a unique six-bit output code from the encoders.

The six-bit code forms the address for one of three ROM's wired in parallel. Each HROM-0512 stores 64 eight-bit words, which can be programmed electrically by the user (contact Harris Semiconductor for data sheets and programming instructions).

Each ROM is initially programmed for the desired output word at the address location corresponding to a certain key. One ROM contains all 64 output words for the unshifted mode, the second contains all words for the shifted mode, and the third contains all words for the control mode. Selection of the particular ROM is accomplished through its enable inputs.

Obviously, there is no requirement for a logical relationship between corresponding words in the three ROM's, which greatly simplifies implementation of special codes. If it is desired that a particular word remain the same in all three modes, simply program the same word at the same address in the three ROM's.

A great advantage of this system is that any eight-bit code can be produced without any changes in wiring or P.C. board layout, simply by plugging in ROM's programmed to desired code. Additional ROM's could be wired in parallel with the enable inputs wired appropriately to produce multiple codes (both ASCII and EBCDIC codes, for example) either simultaneously or selectively.

Memory

Data Sheets

Application Notes

MEMORY DATA SHEETS

HM1-0110/0168/0104/0186	Commercial Diode Matrix
MONOLITHIC DIODE MATRICES	Monolithic Interface Circuits
HRAM-0064	High-Speed, 64-Bit Bipolar Random-Access Memory
HPROM-1256	256-Bit, Bipolar PROM
HPROM-8256	256-Bit, Bipolar PROM
HPROM-0512	512-Bit, Bipolar PROM
HPROM-1024/1024A	1024-Bit, Field Programmable Bipolar PROM
HPROM-2560/2561	2560-Bit, MOS Read-Only Memory for Horizontal, 5 x 7 Dot Matrix Character Generator

MEMORY APPLICATION NOTES

NOTE 201	Diode Matrices (4 x 10, 10 x 4)
NOTE 203	Programming the HPROM-0512 in an Expanded Configuration
NOTE 206	Monolithic Diode Matrices

HARRIS SEMICONDUCTOR
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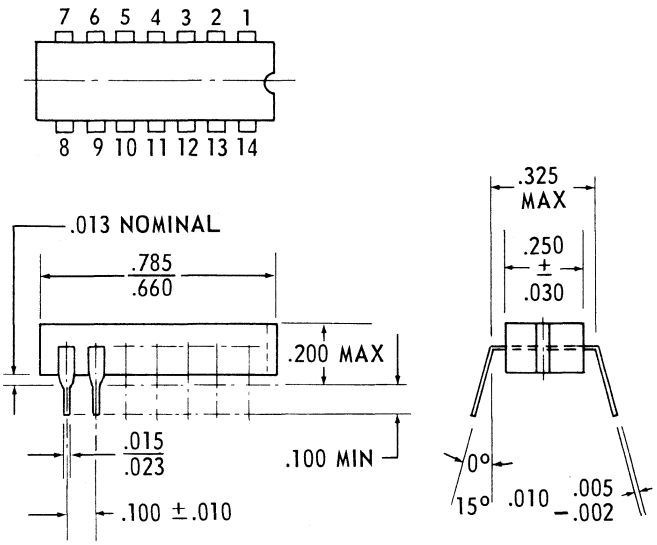
HM1-0110 (4x10)
HM1-0168 (6x 8)
HM1-0104 (10x 4)
HM1-0186 (8x 6)
Commercial Diode Matrix

DESCRIPTION

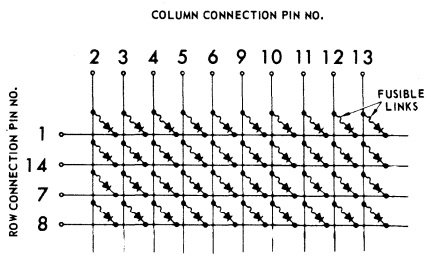
The commercial diode matrices are arrays of passivated silicon diodes, fabricated in dielectrically isolated moats. An epitaxial layer is used as the common cathode connection for all diodes in a row. Column connections to the anode side of the diodes are made through metal interconnect lines via fusible links. By selectively opening the links, diodes can be removed from the circuit to form any desired matrix pattern. This device is available in a 14-lead dual in-line CERDIP package.

PACKAGE

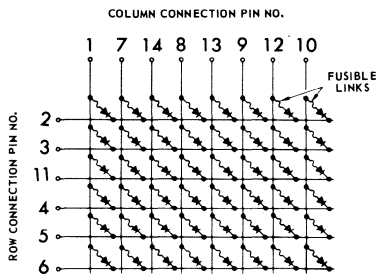


MATRIX PATTERNS

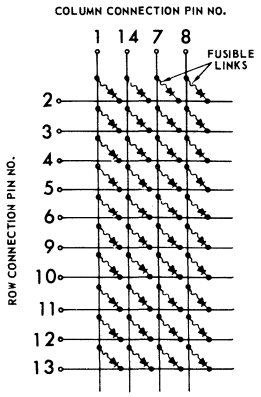
HM1-0110
(4 x 10)



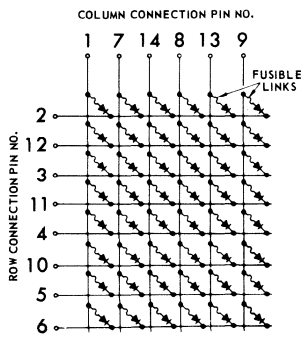
HM1-0168
(6 x 8)



HM1-0104
(10 x 4)



HM1-0186
(8 x 6)



MEMORY DATA

ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 µs Max.)	200mA
Total Circuit Dissipation (Still Air)	450mW
Operating Temperature (Ambient)	0°C to 70°C

ELECTRICAL CHARACTERISTICS AT 25°C

CHARACTERISTIC		HM1-0104 (10 x 4) HM1-0168 (6 x 8) HM1-0186 (8 x 6) LIMITS		HM1-0110 (4 x 10) LIMITS		CONDITIONS
		MIN.	MAX.	MIN.	MAX.	
Forward Drop	V_{F20}		1.5V		1.8V	I_F = 20mA
Forward Drop	V_{F1}		0.9V		1.0V	I_F = 1mA
Rev. Breakdown Volt.	BV_R	20V		20V		I_R = 100µA
Rev. Current	I_R		1µA		1µA	V_R = 15V
Rev. Rec. Time			100ns		100ns	I_F = 10mA I_R = 10mA to 1mA
Coupling Capacitance	C_{CP}		8pF		8pF	V_R = 5V f = 1MHz

NOTE: When ordering a matrix with a custom pattern either obtain copies of Harris patternizing forms from your local sales representative or contact headquarters, Marketing, Melbourne, Florida.

On all orders less than 100 units there will be a one time charge for each special pattern formed by Harris.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

MONOLITHIC DIODE MATRICES

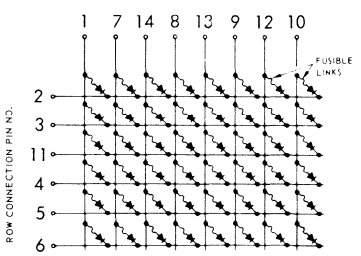
Monolithic Interface Circuits

Harris Monolithic Diode Matrices consist of arrays of passivated silicon diodes, fabricated in dielectrically isolated moats. Use of improved epitaxial techniques allow construction of arrays using the epitaxial layer as the common cathode connection for all diodes in a row. Column connection to the anode side of the diodes are made to metalized interconnect lines via fusible links. By selectively opening fuses, diodes are effectively removed from the circuit to form any desired matrix pattern. Harris automatic production test equipment provides instantaneous code pattern customizing from finished goods inventory.

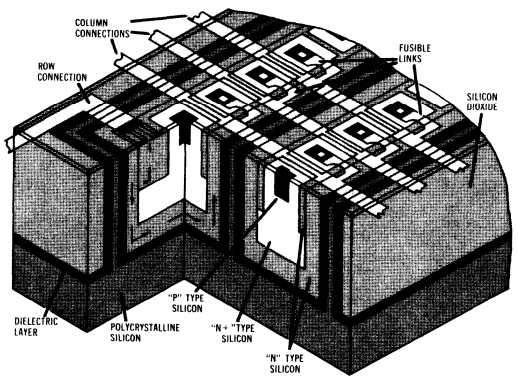
Combining the fusing technique with the availability of various matrix sizes and the possibility of assembling several matrices to form larger arrays, provides designers with the necessary flexibility in system design.

The matrices meet full military temperature range operation (-55°C to +125°C) and the circuits are designed to meet or exceed the mechanical and environmental requirements of MIL-STD-883.

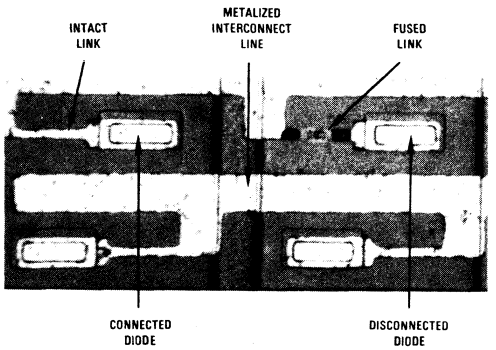
TYPICAL 6 x 8 CIRCUIT SCHEMATIC



Harris matrices are ideally suited for applications in logic generation, coding, decoding, and addressing type networks. For further information refer to Harris Diode Matrix Technical Information and Application Bulletin.



MONOLITHIC STRUCTURE



FUSIBLE LINK SYSTEM

MONOLITHIC INTERFACE CIRCUITS

When the Harris family of Monolithic Diode Matrices are used with Harris Monolithic Interface circuits, complex logic generation is possible with simple diode-inverter logic. A product selection guide for the monolithic interface circuits is given to help designers select the best interface circuit and matrix for his application. The interface circuits can be used for input to or output from any diode matrix.

MONOLITHIC DIODE MATRICES

PRODUCT SELECTION GUIDE

MILITARY

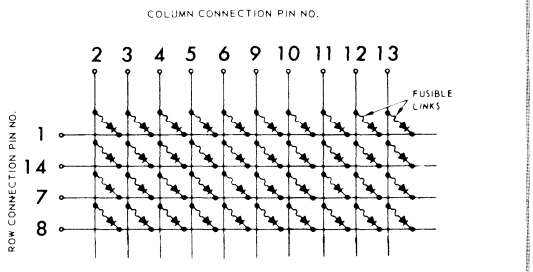
MATRIX SIZE	FAST RECOVERY	MEDIUM RECOVERY	GENERAL PURPOSE	PACKAGE OUTLINE
4 x 10	HM1-090	HM1-091	HM1-093	A
4 x 10	HM9-090	HM9-091	HM9-093	B
10 x 4	HM1-050	HM1-051	HM1-055	A
10 x 4	HM9-050	HM9-051	HM9-055	B
5 x 5	HM1-074	HM1-075	HM1-077	A
5 x 5	HM9-074	HM9-075	HM9-077	B
5 x 8	HM1-010	HM1-012	HM1-013	A
5 x 8	HM9-010	HM9-012	HM9-013	B
8 x 5	HM1-080	HM1-081	HM1-084	A
8 x 5	HM9-080	HM9-081	HM9-084	B
6 x 8	HM1-030	HM1-031	HM1-034	A
6 x 8	HM9-030	HM9-031	HM9-034	B
8 x 6	HM1-040	HM1-041	HM1-044	A
8 x 6	HM9-040	HM9-041	HM9-044	B

TYPICAL CHARACTERISTICS AT 25°C

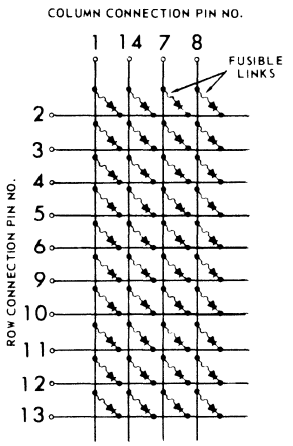
V_f $I_f = 1$ mA	V_f $I_f = 20$mA	BV_R $I_R = 100$uA	I_R $V_R = 25$V	t_{rr} *	C_{CP} $V_R = 5$V
FAST RECOVERY					
0.7V	1.0V	60V	25nA	7ns	1.9pF
MEDIUM RECOVERY					
0.75V	1.3V	60V	50nA	11ns	1.9pF
GENERAL PURPOSE					
0.7V	1.0V	50V	70nA	20ns	1.9pF

* 10 mA I_f to 10 mA I_R recover to 1 mA

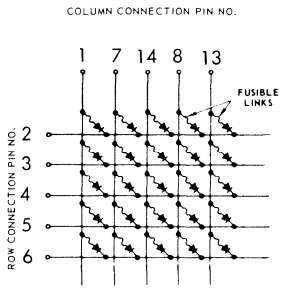
DIODE PIN OUT CONFIGURATION



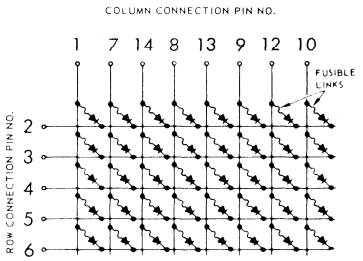
4 x 10



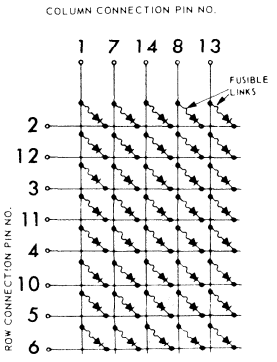
10 x 4



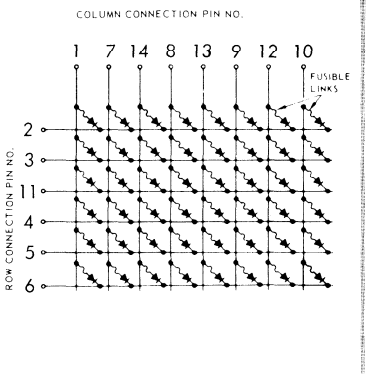
5 x 5



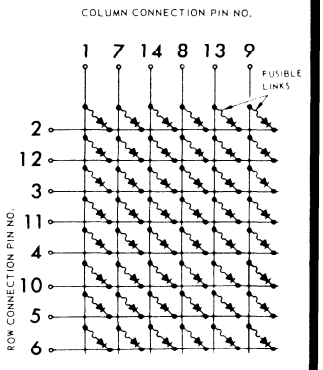
5 x 8



8 x 5



6 x 8



8 x 6

Harris now has available a family of Diode Matrices whose parameters and limits are designed for commercial applications. Contact your nearest sales office or headquarters marketing, Melbourne, Florida for detailed information.

MEMORY DATA

FAST RECOVERY MATRICES

HM-074	5 x 5	HM-050	10 x 4
HM-010	5 x 8	HM-080	8 x 5
HM-030	6 x 8	HM-090	4 x 10
HM-040	8 x 6		

ABSOLUTE MAXIMUM RATINGS

Forward Current : 100 mA
Surge Current (100 μ s max.) : 200 mA
Total Ckt. Dissipation (still air) : 450 mW
Operating Temp. (ambient) : −55°C to +125°C
Storage Temp. (ambient) : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

ELECTRICAL CHARACTERISTICS

HM-010 HM-050 HM-080
HM-030 HM-074 HM-090
HM-040

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS	
	MIN.	TYP.	MAX.		TEMP.	ELECTRICAL
FORWARD DROP						
$V_{F\,20}$			1.5	V	−55°C	I_F = 20 mA
		1.0	1.3	V	+25°C	I_F = 20 mA
$V_{F\,1}$			.95	V	−55°C	I_F = 1 mA
		0.7	.75	V	+25°C	I_F = 1 mA
REVERSE BREAKDOWN						
BV_R	40			V	−55°C	I_R = 100 μA
	45	60		V	+25°C	I_R = 100 μA
REVERSE CURRENT						
I_R		7	25	nA	+25°C	V_R = 25V
			10	μA	+125°C	V_R = 25V
REVERSE RECOVERY						
t_{rr}		7	10	ns	+25°C	I_F = 10 mA to I_R = 10 mA Recovery to 1 mA
CROSSPOINT CAPACITANCE						
C_{cp}		1.9	4.0	pF	+25°C	V_R = 5V, f = 1MHz
COUPLING COEFFICIENT						
I_{CL}		20	50	μA	+25°C	

PERFORMANCE CURVES (SEE PAGE 6 FOR PERFORMANCE CHARACTERISTIC CURVES.)

V_F	Figure 1	Figure 2
I_R	Figure 3	Figure 5
C_{cp}	Figure 6	

MEDIUM RECOVERY MATRICES

HM-075	5 x 5	HM-051	10 x 4
HM-012	5 x 8	HM-081	8 x 5
HM-031	6 x 8	HM-091	4 x 10
HM-041	8 x 6		

ABSOLUTE MAXIMUM RATINGS

Forward Current : 100 mA
Surge Current (100 μs max.) : 200 mA
Total Ckt. Dissipation (still air) : 450 mW
Operating Temp. (ambient) : −55°C to +125°C
Storage Temp. (ambient) : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

ELECTRICAL CHARACTERISTICS

HM-012 HM-051 HM-081
HM-031 HM-075 HM-091
HM-041

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS	
	MIN.	TYP.	MAX.		TEMP.	ELECTRICAL
FORWARD DROP						
$V_{F\,20}$			1.7	V	−55°C	I_F = 20 mA
		1.2	1.5	V	+25°C	I_F = 20 mA
$V_{F\,1}$			1.0	V	−55°C	I_F = 1 mA
		0.75	0.8	V	+25°C	I_F = 1 mA
REVERSE BREAKDOWN						
BV_R	35			V	−55°C	I_R = 100 μA
	40	60		V	+25°C	I_R = 100 μA
REVERSE CURRENT						
I_R		25	50	nA	+25°C	V_R = 25V
			25	μA	+125°C	V_R = 25V
REVERSE RECOVERY						
t_{rr}		11	25	ns	+25°C	I_F = 10 mA to I_R = 10 mA Recovery to 1 mA
CROSSPOINT CAPACITANCE						
C_{cp}		1.9	4.0	pF	+25°C	V_R = 5V, f = 1MHz
COUPLING COEFFICIENT						
I_{CL}		20	50	μA	+25°C	

PERFORMANCE CURVES (SEE PAGE 6 FOR PERFORMANCE CHARACTERISTIC CURVES.)

V_F	Figure 2	Figure 2
I_R	Figure 4	Figure 5
C_{cp}	Figure 6	

GENERAL PURPOSE MATRICES

HM-077	5 x 5	HM-055	10 x 4
HM-013	5 x 8	HM-084	8 x 5
HM-034	6 x 8	HM-093	4 x 10
HM-044	8 x 6		

ABSOLUTE MAXIMUM RATINGS

Forward Current : 100 mA
Surge Current (100 μs max.) : 200 mA
Total Ckt. Dissipation (still air) : 450 mW
Operating Temp. (ambient) : −55°C to +125°C
Storage Temp. (ambient) : −65°C to +150°C

Maximum ratings are limiting values above which permanent circuit damage may occur.

ELECTRICAL CHARACTERISTICS

HM-013 HM-055 HM-084
HM-034 HM-077 HM-093
HM-044

CHARACTERISTIC	LIMITS			UNIT	TEST CONDITIONS	
	MIN.	TYP.	MAX.		TEMP.	ELECTRICAL
FORWARD DROP						
$V_{F\,20}$			1.5	V	−55°C	I_F = 20 mA
		0.95	1.3	V	+25°C	I_F = 20 mA
$V_{F\,1}$			.95	V	−55°C	I_F = 1 mA
		0.7	.75	V	+25°C	I_F = 1 mA
REVERSE BREAKDOWN						
BV_R	30			V	−55°C	I_R = 100 μA
	35	50		V	+25°C	I_R = 100 μA
REVERSE CURRENT						
I_R		70	250	nA	+25°C	V_R = 25V
			50	μA	+125°C	V_R = 25V
REVERSE RECOVERY						
t_{rr}		20	50	ns	+25°C	I_F = 10 mA to I_R = 10 mA Recovery to 1 mA
CROSSPOINT CAPACITANCE						
C_{cp}		2.0	4.0	pF	+25°C	V_R = 5V, f = 1MHz
COUPLING COEFFICIENT						
I_{CL}		20	50	μA	+25°C	

PERFORMANCE CURVES (SEE PAGE 6 FOR PERFORMANCE CHARACTERISTIC CURVES.)

V_F	Figure 1	Figure 2
I_R	Figure 5	Figure 5
C_{cp}	Figure 6	

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 1

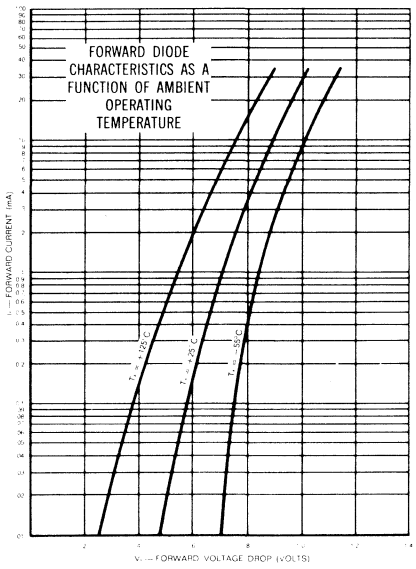


FIGURE 2

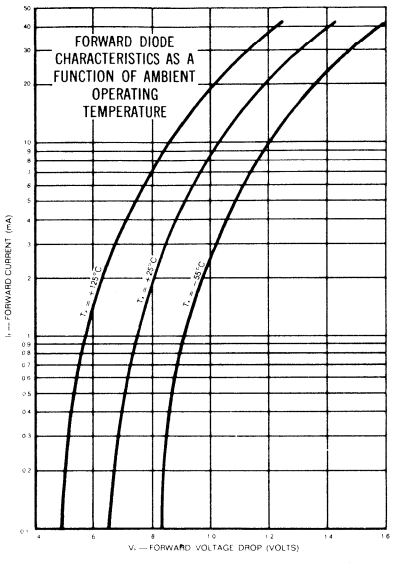


FIGURE 3

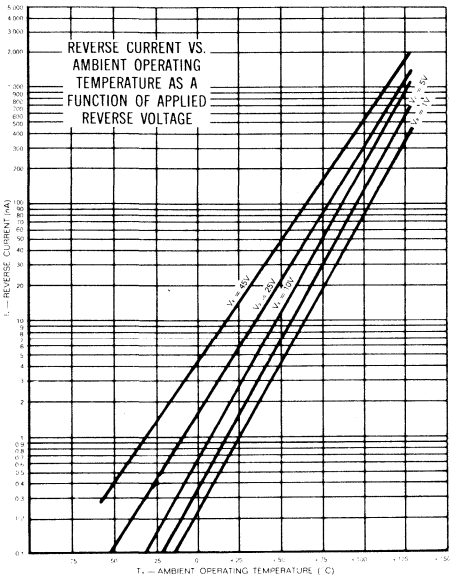


FIGURE 4

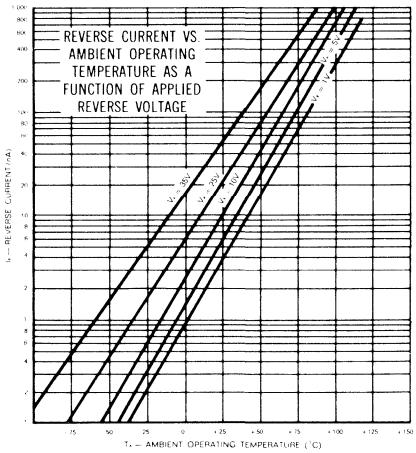


FIGURE 5

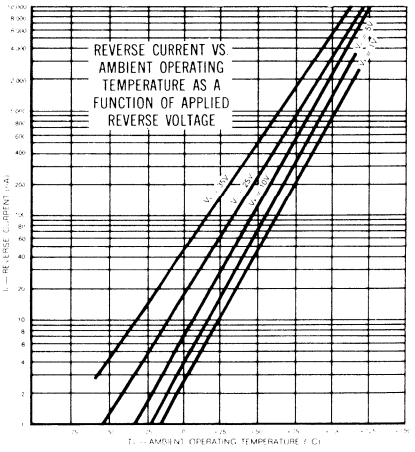
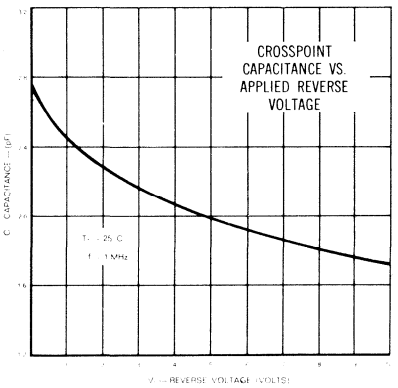
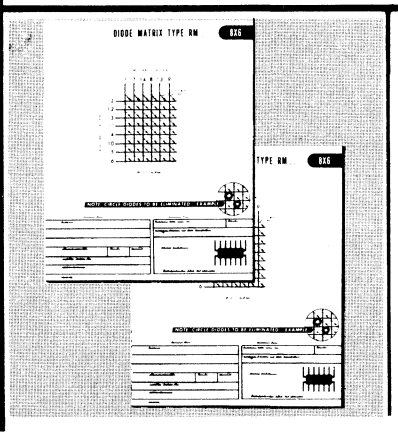


FIGURE 6

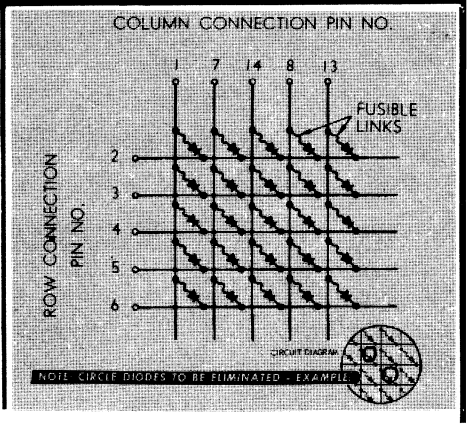


CUSTOM PATTERNS



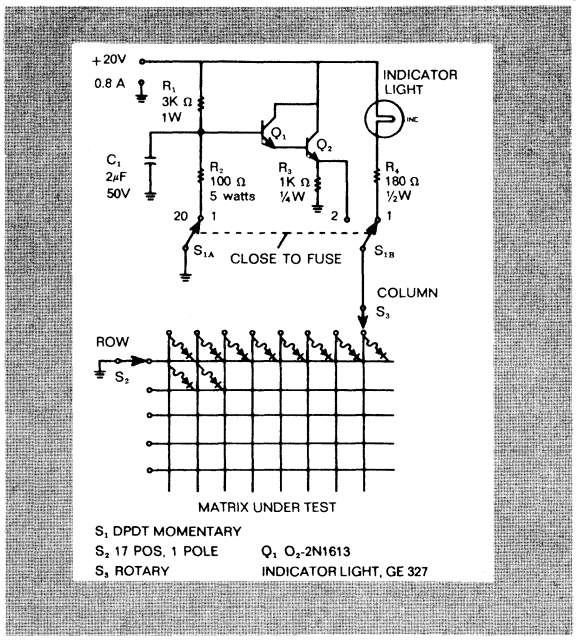
When ordering a matrix with a custom pattern either obtain copies of Harris patternizing forms from your local sales representative or take a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify pattern is to call out row and column pins for each diode to be removed.

On all orders less than 100 units there will be a one time charge for each special pattern formed by Harris.



DIODE MATRIX FUSING

A simple ramp current generator is used to provide the fusing current. With switch S_{1A} in the position shown the capacitor C_1 is discharged to ground through R_2. The diode to be eliminated is selected by setting the row and column switches S_2 and S_3 respectively as required. When switch S_{1A} is activated to position 2, capacitor C_1 charges up through R_1 forming a ramp voltage that drives the base of Q_1. The darlington transistor pair of Q_1 and Q_2 transforms the voltage ramp to a current ramp that provides current to the column contacts on the matrix. This current, through the fuse, opens the fusible link in series with the selected diode. The peak fusing current required to open a fusible link, is approximately 750 milliamperes. As the temperature of the fuse is raised, the aluminum begins to melt. This melting continues until the fuse link separates. The cohesive forces of the melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum at approximately 650°C will not affect the passivating layer of silicon dioxide whose melting temperature is about 1350°C. Test verification is obtained by an indicating device placed in series with the column and row switches through the contacts S_{1B} to give visual indication of the condition of each diode in the matrix before and after fusing.



MONOLITHIC INTERFACE CIRCUITS

Harris interface circuits and monolithic diode matrices form a compatible family of intergrated circuits to complement any logic design. These circuits in combination can perform AND, OR, INVERT, AND-OR, NAND/NOR logic functions. The versatility of these circuits is unsurpassed when control, coding and decoding logic functions are performed.

PRODUCT SELECTION GUIDE FOR INTERFACE CIRCUITS

200 / 300 SERIES MILITARY −55°C to +125°C

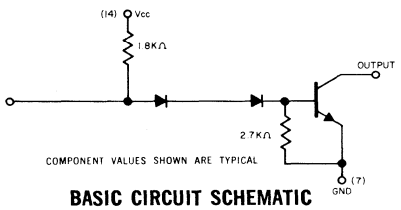
TYPICAL CHARACTERISTICS AT $V_{cc} = 5.0$ V AND $T_A = +25°C$

TYPE NUMBER	DESCRIPTION	Fan-Out	t_{pd} (ns)	Power Dissipation (mW)	Package Type	Notes
HD-234	Hex Interface Inverter	8	8	10	A	1
HD-1234	Hex Interface Inverter	8	8	10	B	1
HD-334	Hex Interface Inverter	5	8	10	A	1
HD-1334	Hex Interface Inverter	5	8	10	B	1
HD-235	Hex Interface Driver	35 V	35	10	A	2
HD-1235	Hex Interface Driver	35 V	35	10	B	2

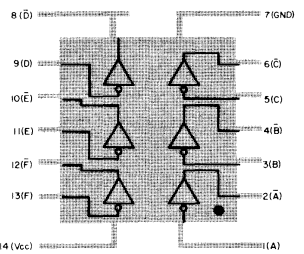
500 SERIES INDUSTRIAL 0°C to +75°C

TYPICAL CHARACTERISTICS AT $V_{cc} = 5.0$ V AND $T_A = +25°C$

TYPE NUMBER	DESCRIPTION	Fan-Out	t_{pd} (ns)	Power Dissipation (mW)	Package Type	Notes
HD-534	Hex Interface Inverter	5	18	12	A	1
HD-1534	Hex Interface Inverter	5	18	12	B	1
HD-535	Hex Interface Driver	35 V	35	12	A	2
HD-1535	Hex Interface Driver	35 V	35	12	B	2
HD-536	Hex Indicator Driver	55 V	—	12	A	2
HD-1536	Hex Indicator Driver	55 V	—	12	B	2



BASIC CIRCUIT SCHEMATIC (one element)



LOGIC DIAGRAM (top view)

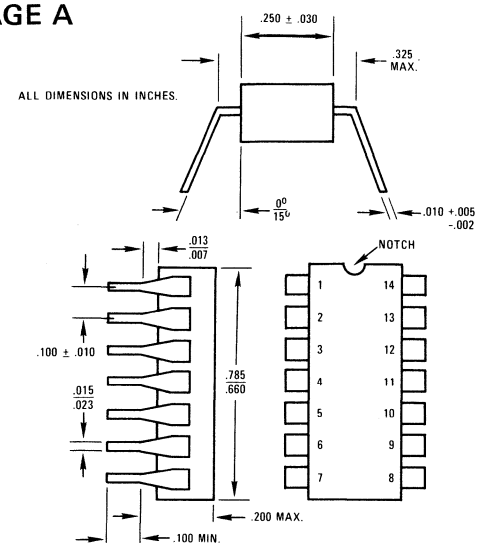
NOTES:

1.0 Fan-out is defined for Harris DTL logic of the same series number.

2.0 Voltage given in fan-out column is the minimum output breakdown voltage for this gate element.

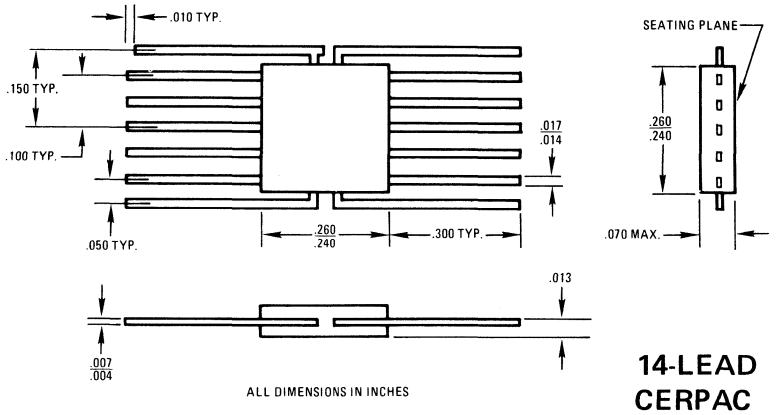
MEMORY DATA

PACKAGE A



14-LEAD CERDIP

PACKAGE B



14-LEAD CERPAC

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

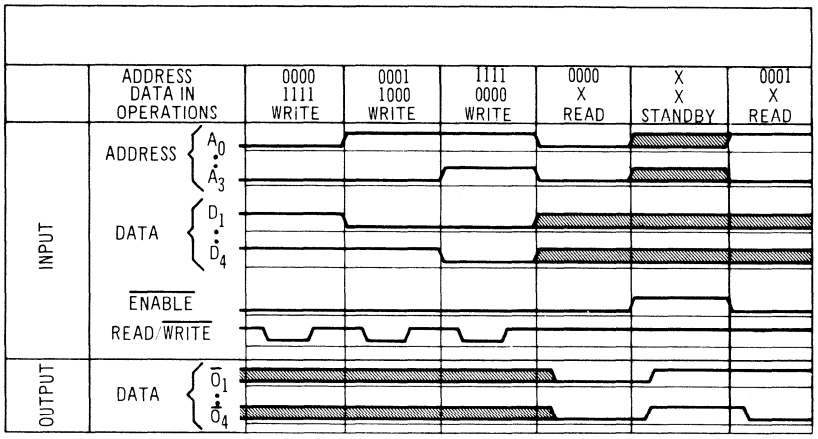
HRAM-0064

High-Speed, 64-Bit Bipolar Random-Access Memory

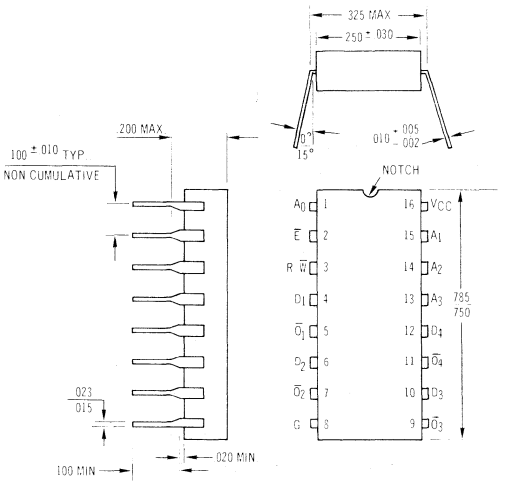
FEATURES

- 40 NS TYPICAL ACCESS TIME
- DTL/TTL COMPATIBLE – 5 VOLT SUPPLY
- FULLY DECODED – 16 WORDS/4 BITS PER WORD
- STATIC OUTPUTS – FANOUT OF TEN
- EXPANDABLE – "WIRED-OR" OUTPUTS/CHIP ENABLE INPUT
- AVAILABLE IN EITHER 0°C TO +75°C OR −55°C TO +125°C TEMPERATURE RANGES
- CERAMIC 16 PIN DUAL IN-LINE PACKAGE

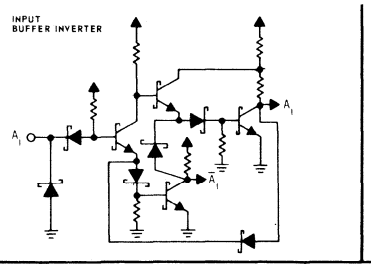
TYPICAL OPERATING SEQUENCE

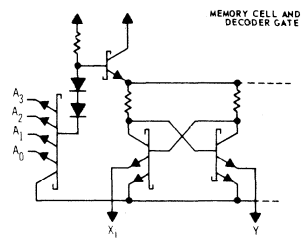


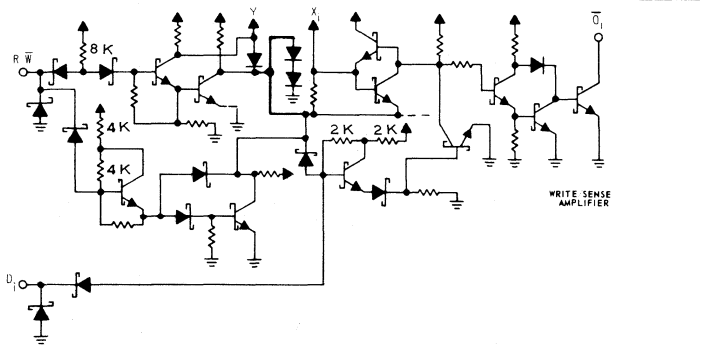
PACKAGE



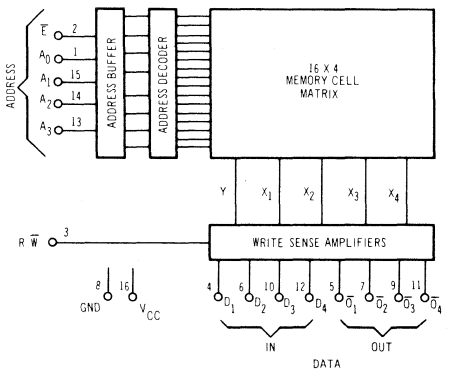
CIRCUITS







BLOCK DIAGRAM



MEMORY DATA

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{CC}	+7.0V	Output Sink Current, I_{OL}	100mA
Input Voltages (All)	+5.5V	Ambient Storage Temperature	−65°C to +150°C
Output Supply Voltage, V_{OS}	+5.5V	Case Operating Temperature*	−55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5.0V ± 5%, T_{CASE} = { −55°C to +125°C (HRAM-0064-2); 0°C to +75°C (HRAM-0064-5) } unless otherwise specified

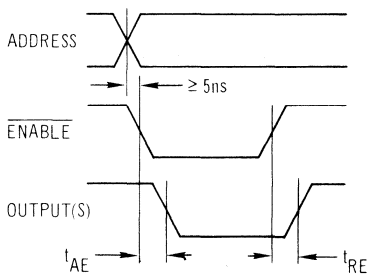
	PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
D.C.	Input Load Current	I_{FA}, I_{FE}, I_{FW}, I_{FD}			1.6	mA	V_{IN} = 0.4 Volts
	Input Leakage Current	I_{RA}, I_{RE}, I_{RW}, I_{RD}			40	µA	V_{IN} = 5.25 Volts
	Input Clamp Voltage	V_{CA}, V_{CE}, V_{CW}, V_{CD}			1.0	Volts	I_{IN} = -5.0 mA
	Output "Low" Voltage	V_{OL}			0.45	Volts	I_{OL} = 16 mA
	Output Leakage Current	I_{OH}			100	µA	V_{OH} = 5.25 Volts
	Output Capacity	C_{OUT}		8.0		pF	V_O = 2.0 Volts
	Input Capacity	C_{IN}		6.0		pF	V_I = 2.0 Volts
	Input Threshold "0"	V_{IL}			0.8	Volts	
	Input Threshold "1"	V_{IH}	2.0			Volts	
	Standby Power Supply Current	I_{CC}			105	mA	Inputs/Outputs Open
A.C.	Enable To Output Delay	t_{AE}		40	60	ns	R_1 = 300 Ω
	Sense Recovery Time	t_{RE}		40	60	ns	R_2 = 600 Ω
	Address To Output Delay	t_+, t_-		40	60	ns	C_L = 30 pF
	Write Setup Time	t_{WS}	5.0			ns	T = 25°C
	Write Pulse Width	t_{WP}	40			ns	V_{CC} = 5.0 Volts
	Write Recovery Time	t_{WR}			50	ns	

*Case temperature is commonly used in specifying complex circuits such as the HRAM-0064. This is done to simplify testing and to give the designer a firmer reference on which to base the thermal design of his system. Ambient temperature specifications require a description of the thermal characteristics of the test system used, and deviations from these require additional specification correlation by the system designer.

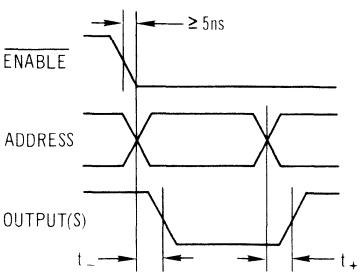
MEMORY DATA

SWITCHING TIME DEFINITIONS

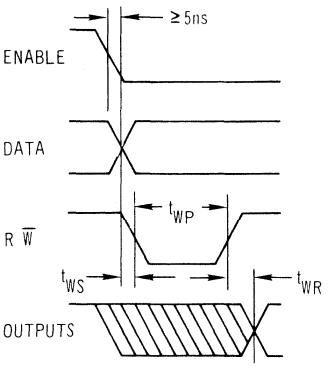
READ CYCLE "A"



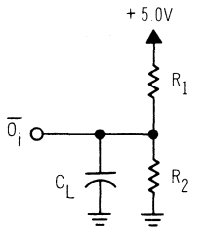
READ CYCLE "B"



WRITE CYCLE:



TEST LOAD:

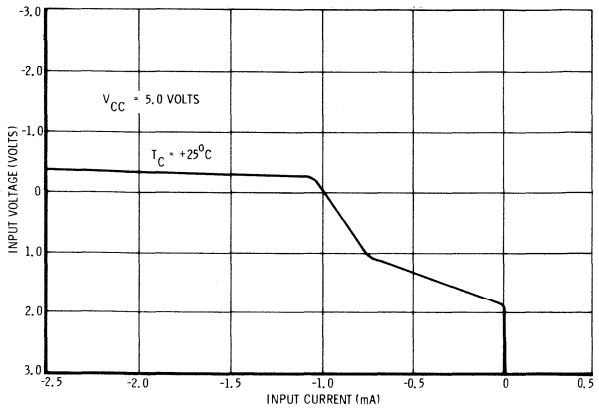


NOTES:

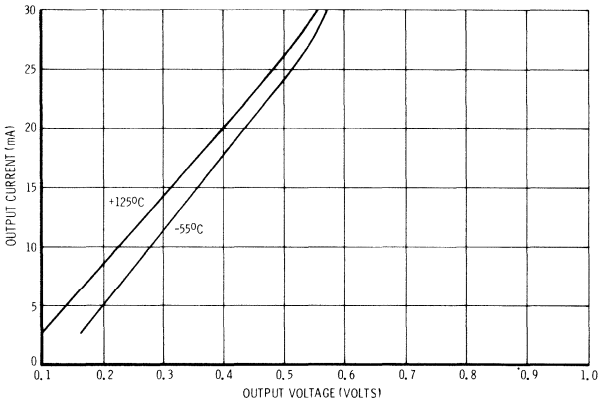
1. All rise and fall times ≤ 10 ns.
2. Measurements from 1.5V levels.
3. V_{IN} = 3.0 Volts.
4. Outputs not valid until after t_{WR}.

CHARACTERISTIC CURVES

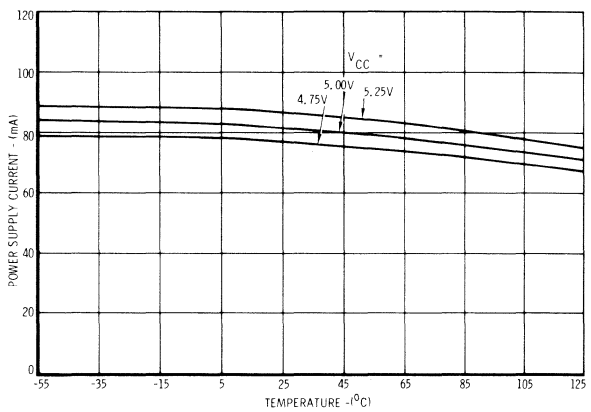
INPUT CURRENT VS. INPUT VOLTAGE



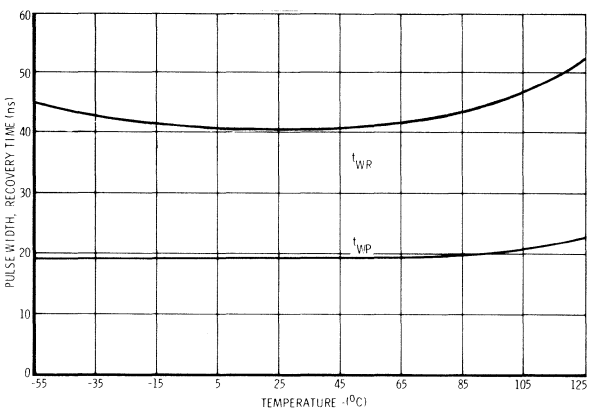
OUTPUT LOW V–I CHARACTERISTICS



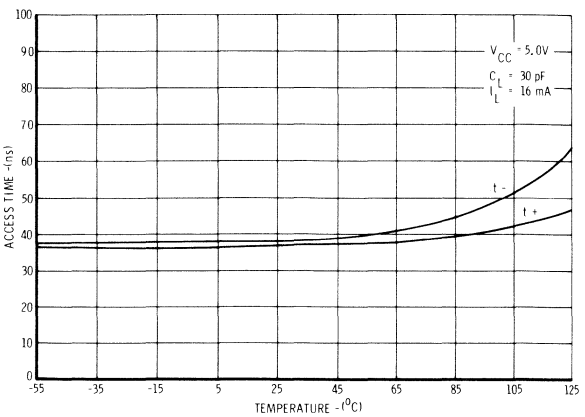
STANDBY POWER SUPPLY CURRENT VS. TEMPERATURE INPUTS/OUTPUTS OPEN



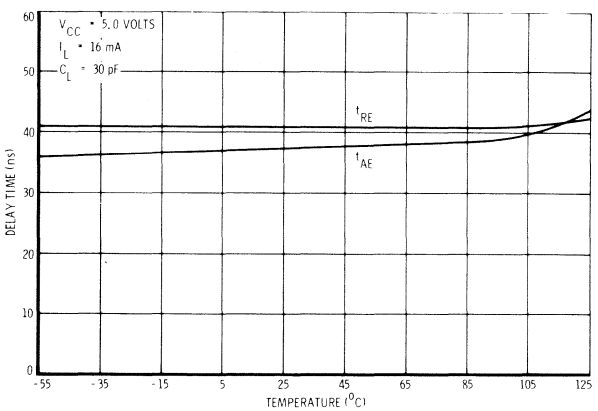
"WRITE" CHARACTERISTICS VS. TEMPERATURE



ADDRESS TO OUTPUT DELAYS VS. TEMPERATURE



ENABLE TO OUTPUT DELAY VS. TEMPERATURE



OPERATION

The HRAM-0064 is a TTL Bipolar Random Access Memory organized in a 16 word by 4 bits/word configuration. The basic memory cell is a multiple-emitter flip-flop designed for high speed and low power.

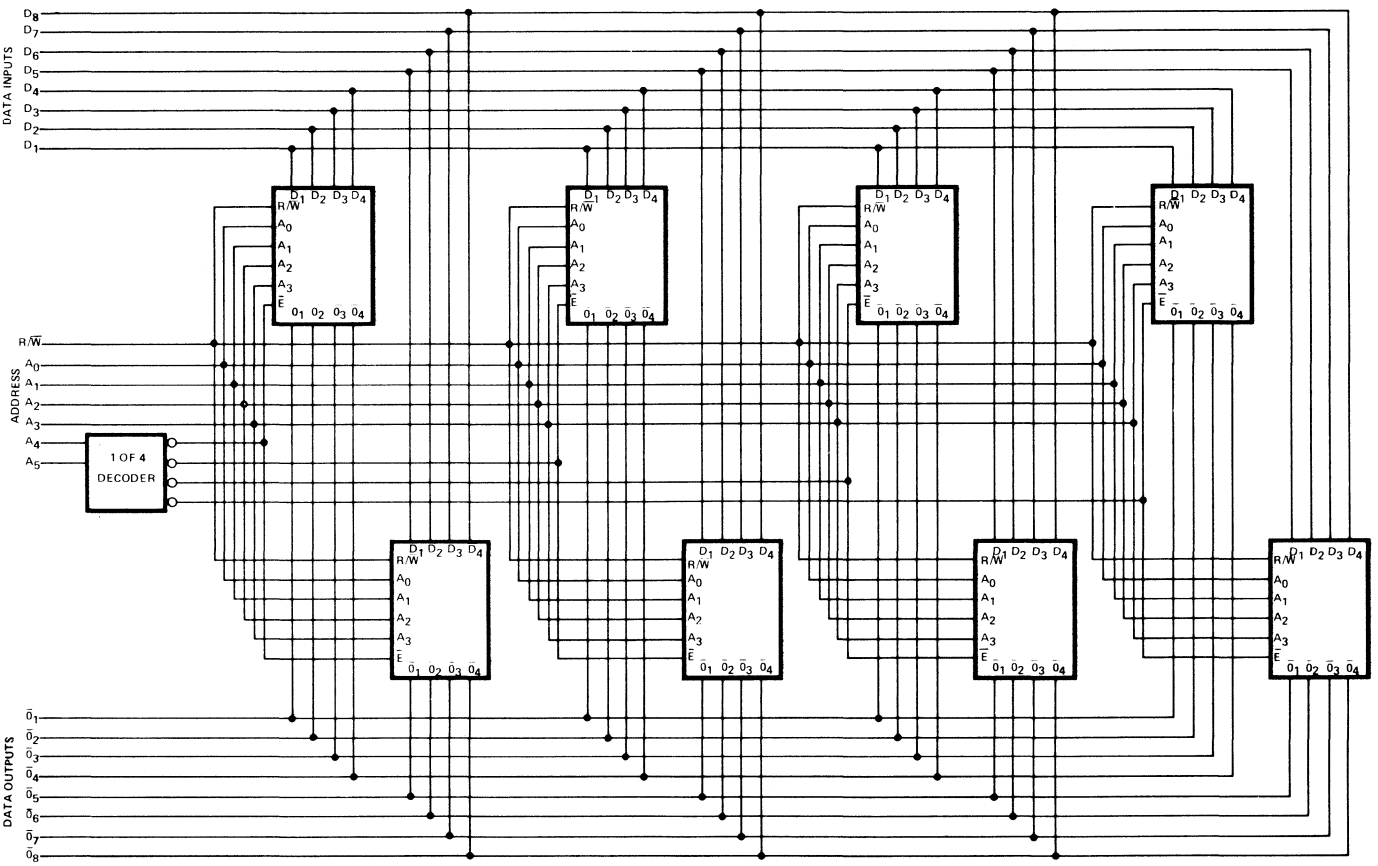
To WRITE data into the memory, a four-bit binary address is placed on the A_0 through A_3 ADDRESS INPUT terminals and the data is placed on the D_1 through D_4 DATA INPUT terminals. This data is entered when the $\overline{\text{ENABLE}}$ and READ/$\overline{\text{WRITE}}$ inputs are brought low.

To READ the data stored in a particular memory location, the appropriate address is again placed on the ADDRESS INPUT terminals and the $\overline{\text{ENABLE}}$ input is brought low. With the READ/$\overline{\text{WRITE}}$ input at logical "one" (high), the complement of the stored data appears at the $\overline{O}_1$ through $\overline{O}_4$ DATA OUTPUT terminals. Reading can also be accomplished by leaving the $\overline{\text{ENABLE}}$ input at logical zero and varying the address data to access the desired memory cells.

The open-collector OUTPUT and $\overline{\text{ENABLE}}$ input provide a convenient means of expanding the memory in the word dimension. Expansion in the bit dimension is accomplished by simply connecting in parallel the $\overline{\text{ENABLE}}$ and ADDRESS terminals of two or more RAM's.

Typical access times for the HRAM-0064 are 40ns for either addressing method, and writing can be accomplished with write pulses as low as 20ns. These speeds make the HRAM-0064 ideal for use in high speed scratch pad and buffer applications.

MEMORY EXPANSION



64 WORD BY 8-BIT

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HPROM-1256

256-Bit, Bipolar PROM™*

FEATURES

- FIELD PROGRAMMABLE
- 256 WORDS/1 BIT PER WORD
- SCHOTTKY CLAMP TRANSISTORS
- 16 PIN DUAL-IN-LINE
- DTL – TTL COMPATIBLE
- PROVEN RELIABLE NICHROME FUSES
- AVAILABLE IN EITHER MILITARY OR COMMERCIAL TEMPERATURE RANGE
- 55ns ADDRESS ACCESS TIME
- 30ns ENABLE TIME

MEMORY DESCRIPTION

The HPROM-1256 is a field-programmable, read-only memory (ROM) organized in a 256 word by 1-bit/word configuration. The memory elements are nichrome links that may be programmed after the device has been packaged and tested. The convenience and utility of field-programming has been shown by the wide acceptance of Harris' first "do-it-yourself" PROM, the HPROM-0512. In addition, extensive life test data on this device has proven the reliability of the nichrome links and the fusing process.

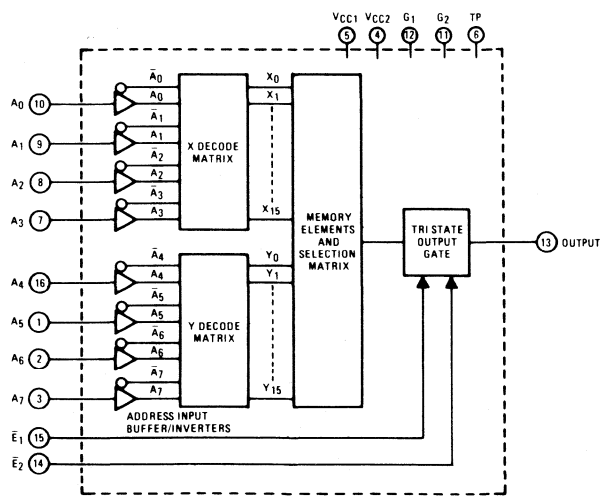
The HPROM-1256 is shipped with the output in a Logic "1" condition for all addressed words. The user then programs in appropriate Logic "0's". Programming is accomplished by opening one of the ground connections (Pin 11) and connecting one of the voltage supply pins (Pin 4) to 15.0V. This allows a sufficient amount of programming current through the nichrome link to cause it to open thus generating a Logical "0" output in that memory location. The programming set-up and step-by-step procedure is shown on page 4.

TRUTH TABLE

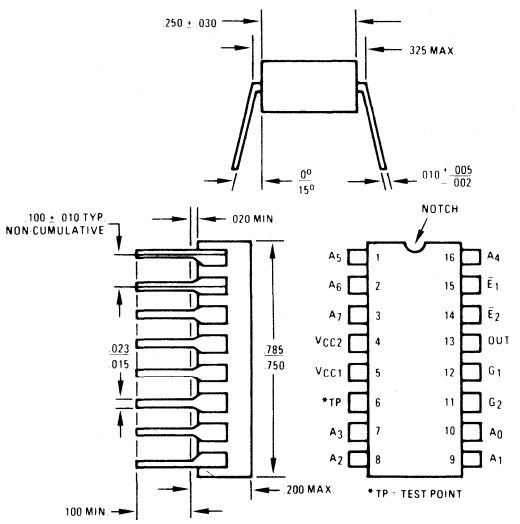
WORD NUMBER	INPUTS $\bar{E}_1$	$\bar{E}_2$	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OUTPUT B_0
X	0	1	X	X	X	X	X	X	X	X	OFF
X	1	0	X	X	X	X	X	X	X	X	OFF
0	0	0	0	0	0	0	0	0	0	0	‡
1	0	0	0	0	0	0	0	0	0	1	‡
2	0	0	0	0	0	0	0	0	1	0	‡
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
255	0	0	1	1	1	1	1	1	1	1	‡

X = DON'T CARE
"OFF" IMPLIES A HIGH IMPEDANCE STATE.
‡ ACTIVE STATE; INITIALLY LOGIC "1", PROGRAMMED FOR LOGIC "0".

BLOCK DIAGRAM



PACKAGE



*PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.

MEMORY DATA

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (Operating Mode), $V_{CC1,2}$	7.0V	Output Voltage, V_{OUT}	5.5V
Programming Voltage, V_{CC2P}	17.0V	Output Sink Current	70mA
Address/$\overline{\text{Enable}}$ Input Voltage, V_A, $V_{\overline{E}}$	5.5V	Ambient Storage Temperature	−65°C to +150°C
Input Current	−30mA	Case Operating Temperature	−55°C to +125°C

ELECTRICAL CHARACTERISTICS

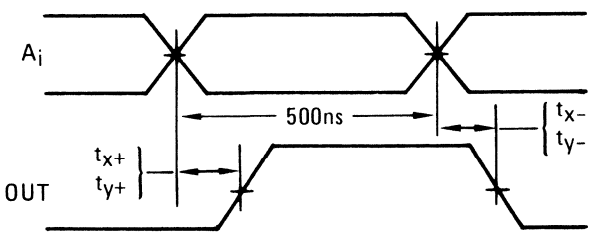
Test Conditions: $V_{CC1} = V_{CC2} = 5.0V \pm 5\%$, $G_1 = G_2 = 0V$

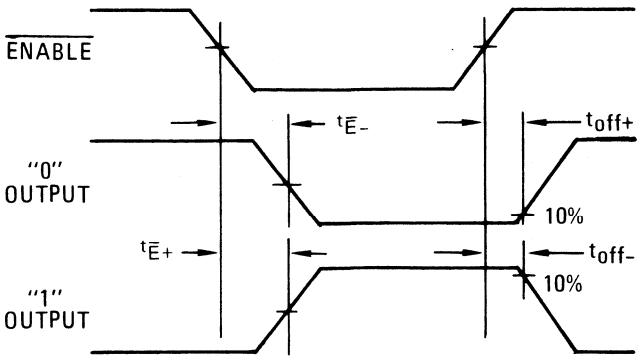
T_{CASE} = { −55°C to +125°C for HPROM-1256-2; 0°C to +75°C for HPROM-1256-5 } unless otherwise specified

	PARAMETER		SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current	"1"	I_{RA}, $I_{R\overline{E}}$			100	μA	V_{AH}, $V_{\overline{E}H}$ = 2.4V
		"0"	I_{FA}, $I_{F\overline{E}}$			1.6	mA	V_{AL}, $V_{\overline{E}L}$ = 0.4V
	Input Clamp Voltage		V_{CA}, $V_{C\overline{E}}$			−1.0	V	I_{IN} = −5mA
	Input Threshold Voltage	"1"	V_{IH}	2.0			V	
		"0"	V_{IL}			0.8	V	
	Output Voltage	"1"	V_{OH}	2.4			V	I_{OH}=2mA, V_{IH}=2.0V, V_{IL}=0.8V
		"0"	V_{OL}		0.25	0.45	V	I_{OL}=-16mA, V_{IH}=2.0V, V_{IL}=0.8V
	Output Leakage		I_{OFF}	−50		+50	μA	V_{OUT}=2.4V, V_E = 2.4V
	Output Capacity		C_O		5.0		pF	V_{OUT} = 2.4V, V_E = 2.4V
	Power Supply Current		I_{CC}		75	120	mA	Inputs/Output Open
A.C.	Address Access Time ($A_0 \rightarrow A_3$)	(Rise)	t_{x+} (1)		35	60	ns	R_L = 400Ω, C_L = 15pF; T = 25°C, V_{CC1}=V_{CC2}=5.0V
		(Fall)	t_{x-} (1)		35	60	ns	
	Address Access Time ($A_4 \rightarrow A_7$)	(Rise)	t_{y+} (1)		25	40	ns	R_L = 400Ω, C_L = 15pF
		(Fall)	t_{y-} (1)		25	40	ns	
	Enable Access Time ($\overline{E}_1$, $\overline{E}_2$)	(Rise)	$t_{\overline{E}+}$ (2)		20	30	ns	R_L = 1.2KΩ, C_L = 15pF
		(Fall)	$t_{\overline{E}-}$ (3)		20	30	ns	R_L = 400Ω, C_L = 15pF
	Disable Delay Time	"0"	t_{OFF+} (3)		10	30	ns	R_L = 1.2KΩ, $C_L \leq$ 5pF
		"1"	t_{OFF-} (2)		10	30	ns	R_L = 400Ω, $C_L \leq$ 5pF

NOTES: (1) See "Test Loads" on page 5 - Figure 1 (2) See "Test Loads" on page 5 - Figure 2 (3) See "Test Loads" on page 5 - Figure 3

SWITCHING TIME DEFINITIONS

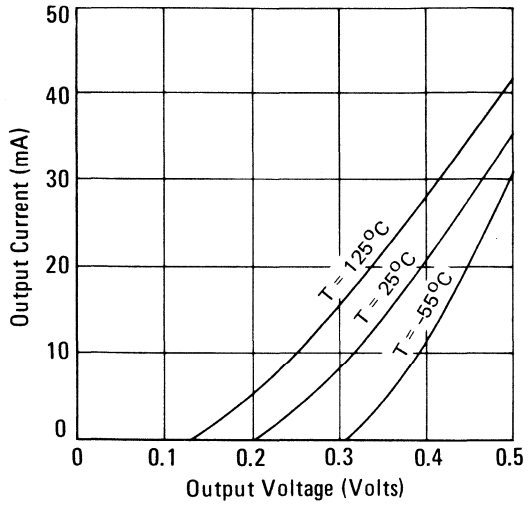




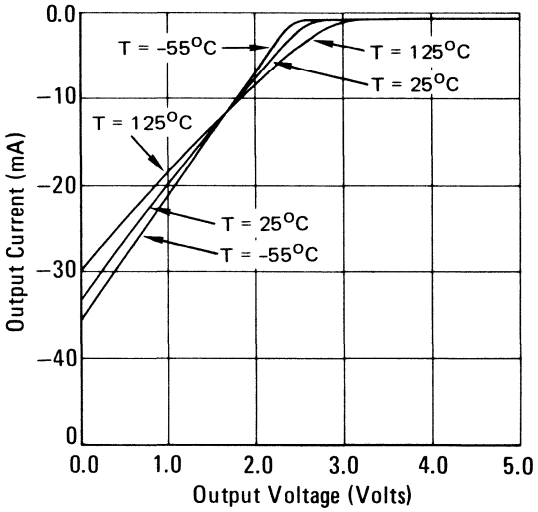
CHARACTERISTIC CURVES

$V_{CC1} = V_{CC2} = 5.0V$

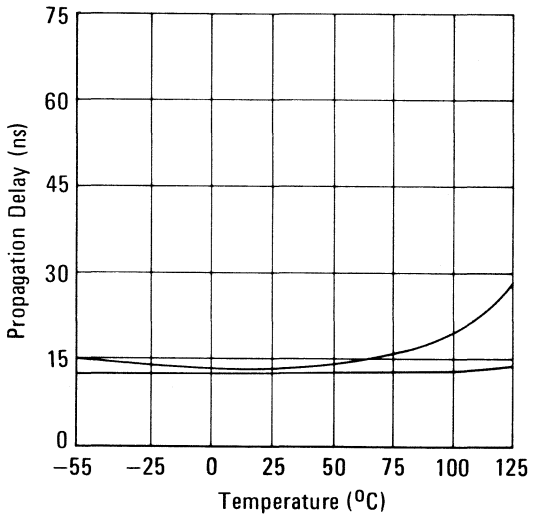
OUTPUT LOW V-I CHARACTERISTICS



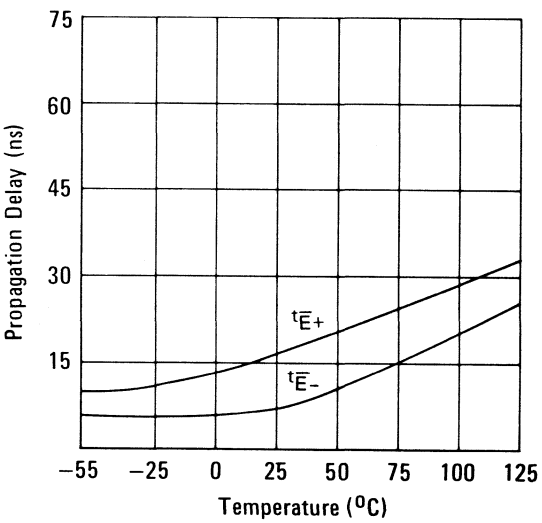
OUTPUT HIGH V-I CHARACTERISTICS



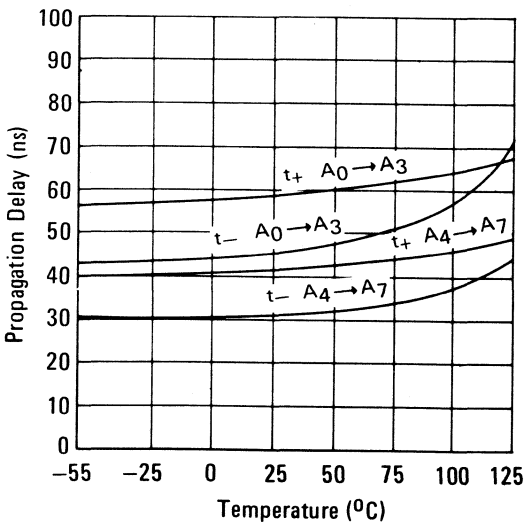
DISABLE TO OUTPUT DELAY VS. TEMPERATURE



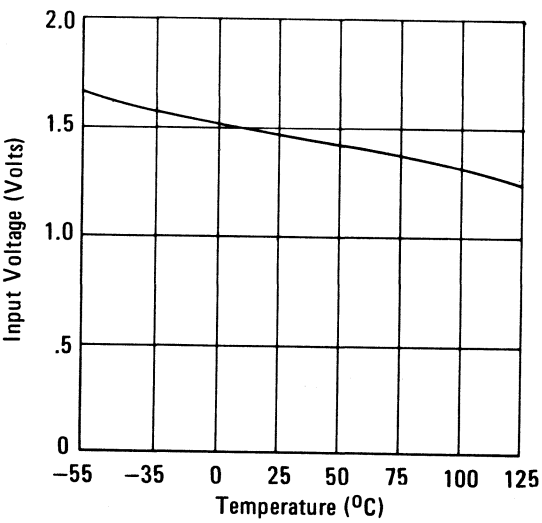
ENABLE TO OUTPUT DELAY VS. TEMPERATURE



ADDRESS TO OUTPUT DELAY VS. TEMPERATURE



INPUT THRESHOLD VS. TEMPERATURE



PROGRAMMING PROCEDURE

The HPROM-1256 can be programmed to any custom pattern simply by following the straightforward procedure given below. The degree of sophistication used in programming will vary from application to application, but in its simplest form, programming can be accomplished with nothing more than a few mechanical switches and two power supplies as shown in Figure 2.

For more automated programming systems, the circuit shown in Figure 3 can be used. This system accepts normal TTL logic levels for all input data except for the programming pulse itself, where an open-collector gate is recommended.

Adherence to the basic principles of programming outlined in the following step-by-step procedure will assure the user of a consistent and reliable product whether manual or automatic methods are employed:

1. With the power supply and ground terminals connected as shown in Figure 1, apply the address of the first word to be programmed to address terminals A_0 through A_7. Since programming involves changing the data stored in a particular memory location from a logical "1" to a logical "0", the first address programmed will usually be the address of the first "0" in the program specification.
2. With the proper address on terminals A_0 through A_7, apply a +15.0V pulse to terminal V_{CC2}. (While the duration of this pulse is not significant from a reliability point of view, it should be kept short to minimize power dissipation and thus maximize the programming rate. In manual programming systems, a one second pulse is acceptable; in automatic systems, a 200 – 800ms pulse should be used with a maximum duty cycle of 20%.)
3. Skipping any word specified as a logical "1", repeat step 2 for each logical "0" in the program specification.

The procedure outlined above is intended merely to convey the mechanics of programming, but (together with the specifications given below) it should serve as a basic guide in the design of more sophisticated systems which may be desirable in certain applications.

NOTE: V_{CC2} should always be at a higher potential than V_{CC1} or an open circuit.
Do not return V_{CC2} to ground with a voltage applied to V_{CC1}.

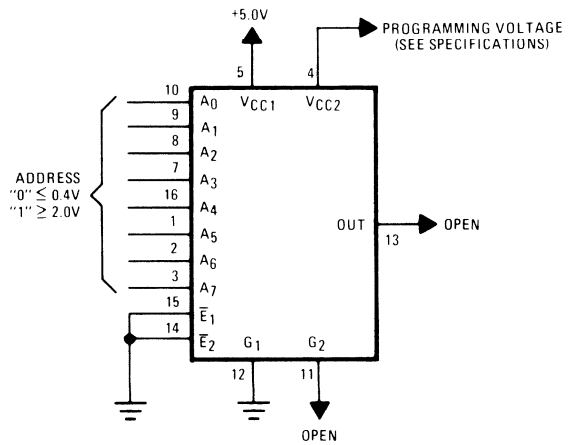


Figure 1. PROGRAMMING CONNECTIONS

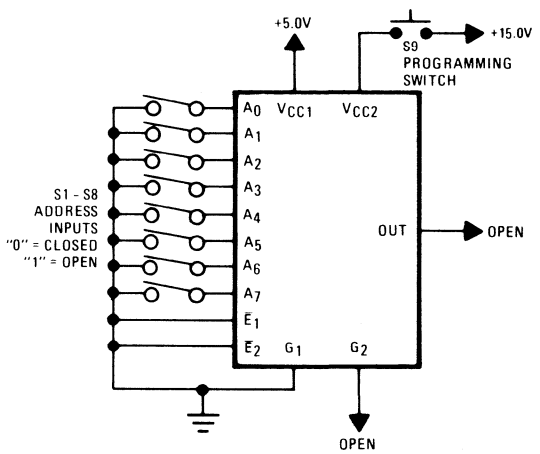


Figure 2. MANUAL PROGRAMMING SYSTEM

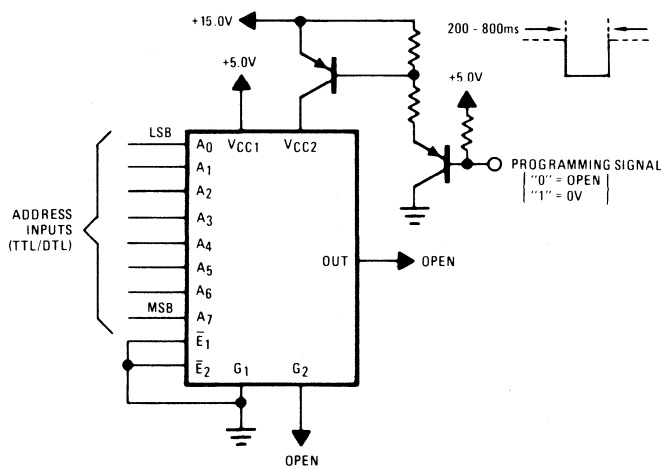


Figure 3. TYPICAL CIRCUIT FOR AUTOMATIC PROGRAMMING

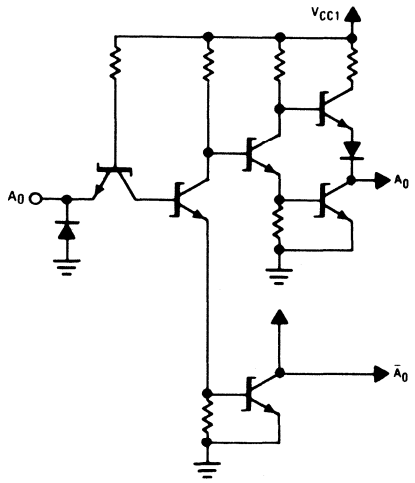
PROGRAMMING REQUIREMENTS

	RECOMMENDED VALUE	LIMIT MIN. MAX.	UNITS
Programming Voltage (V_P)	15	17	V
Programming Pulse Width	200	*	ms
T_{CASE}	75		°C
Duty Cycle	20	30	%

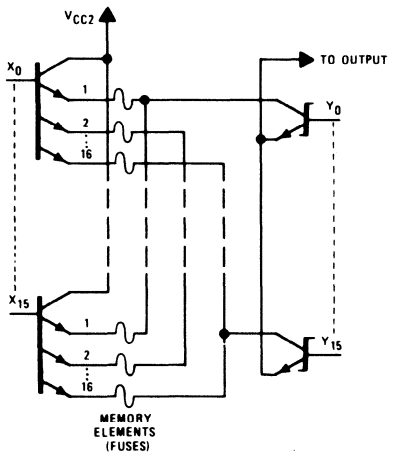
*All devices should program with $t_p < 800$ms.

MEMORY DATA

CIRCUITS



ADDRESS INPUT BUFFER/INVERTER



MEMORY ELEMENT & SELECTION MATRIX

TEST LOADS

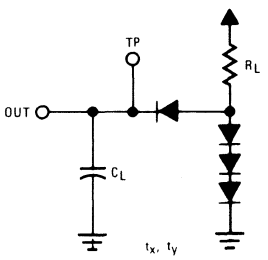


Figure 1

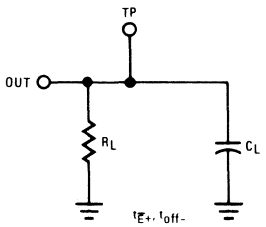


Figure 2

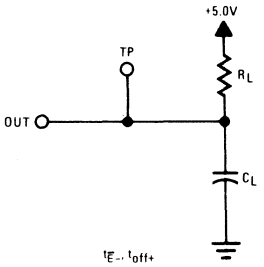


Figure 3

NOTES:

1. V_{IN} = 3.0V; all measurements referenced to 1.5V level except as indicated.
2. Input rise and fall time $\leq$ 10ns.
3. Test loads for Enable Access and Turn-Off Times were designed to simplify testing. The loads simulate loads encountered in actual usage.
4. For performance testing of an unprogrammed device, the generation of a Logic "0" on the output can be accomplished by grounding A_5, A_6 and TP (Pin 6) while supplying a Logic "1" to A_4 and A_7. A_0 thru A_3 are in a "Don't Care" condition.
5. All diodes are 1N3064.

CUSTOM PROGRAMMING

Although the HPROM-1256 is designed to be programmed by the user, there are certain applications where it may be desirable to obtain pre-programmed devices. This can be accomplished simply by generating a program specification similar to that shown in Figure 1. While the format for this specification is somewhat arbitrary, any alternate scheme should provide all of the information and utilize the same address and logic definitions as that shown in Figure 1.

To further minimize the possibility of errors, the programming information can be submitted on a punched card, following the format shown in Figure 2. Since this format is identical to that used to operate Harris' programming and test systems, any errors which could be generated in transferring the data from some other form to the card are virtually eliminated, along with the delays involved in actually performing the transfer. Thus, the punched card format is the preferrable method of specifying data for custom-programmed devices.

HPROM-1256
CUSTOM-PROGRAM SPECIFICATION FORM

INPUTS						OUTPUTS							
					A_7, A_6 →	00		01		10		11	
A_5	A_4	A_3	A_2	A_1	A_0	WORD	OUT	WORD	OUT	WORD	OUT	WORD	OUT
0	0	0	0	0	0	0		64		128		192	
0	0	0	0	0	1	1		65		129		193	
0	0	0	0	1	0	2		66		130		194	
0	0	0	0	1	1	3		67		131		195	
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮		⋮		⋮	
1	1	1	1	1	1	63		127		191		255	

CUSTOMER_____
CUSTOMER DRAWING NO._____
SPECIAL INSTRUCTIONS_____

Figure 1

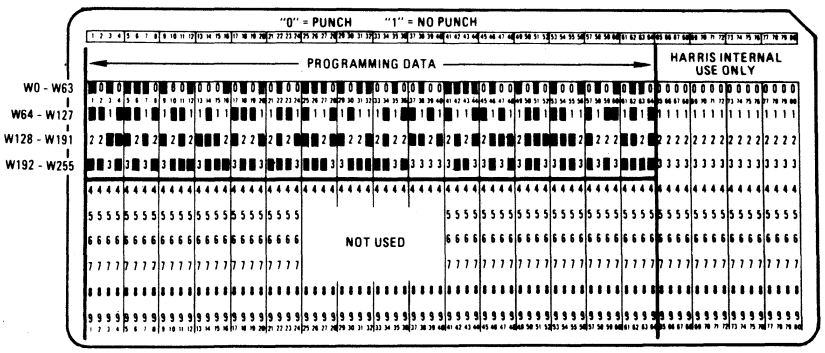
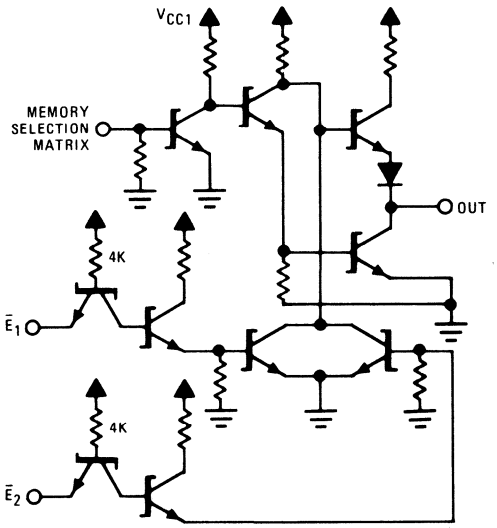


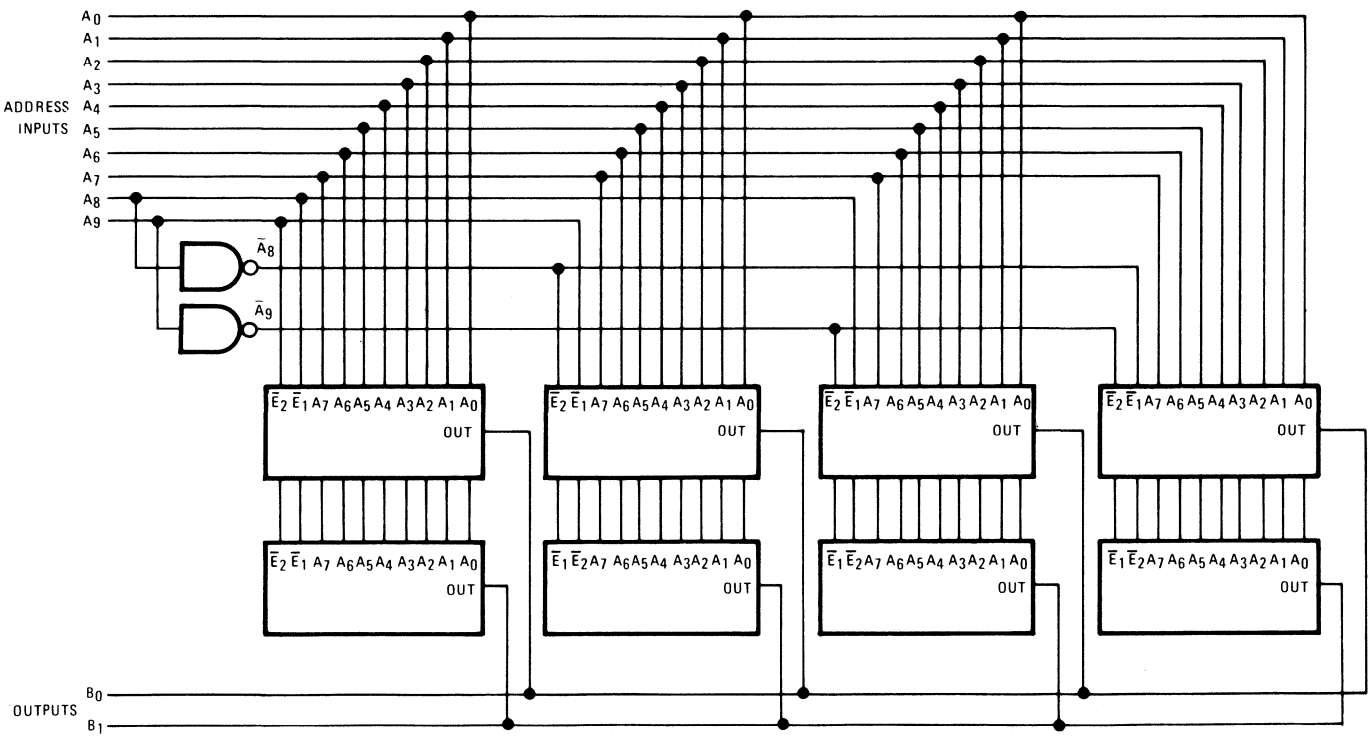
Figure 2

THREE STATE OUTPUT

The output circuit for the HPROM-1256 is shown in the figure on the right. This circuit is designed to provide current during both high and low transitions of the output signal and thus enhance switching times for large capacitive loads. At the same time, "wired-OR" connections are permitted, since a high $\overline{\text{ENABLE}}$ input signal turns off both output transistors, providing a high impedance state on the output terminal. This means that many "Disabled" outputs can be directly connected to a single "Enabled" output with little degradation in the overall fan-out capability. This feature is particularly advantageous in memory systems expanded in the word dimension (see below).



MEMORY EXPANSION



The HPROM-1256 is easily expanded in either the word or bit dimension. The example above shows a 1024 word/2 bits per word expansion which utilizes the dual "Enable" inputs and "wired-OR" output features of this device. The dual "Enables" provide another level of address decoding allowing expansion to 1024 words simply by generating the complement of the last two bits. Bit expansion beyond two bits is accomplished simply by adding more HPROM-1256's to the columns in the above example.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HPROM-8256

256-Bit, Bipolar PROM™*

FEATURES

- FIELD PROGRAMMABLE
- 32 WORDS/8BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 40NS ACCESS TIME
- PROVEN RELIABLE NICHROME FUSES
- SINGLE 5V POWER SUPPLY
- STATIC OUTPUT WITH FANOUT OF 10
- AVAILABLE IN MILITARY AND COMMERCIAL TEMPERATURE RANGES
- EXPANDABLE – "WIRED-OR" OUTPUTS – CHIP ENABLE INPUT

TRUTH TABLE

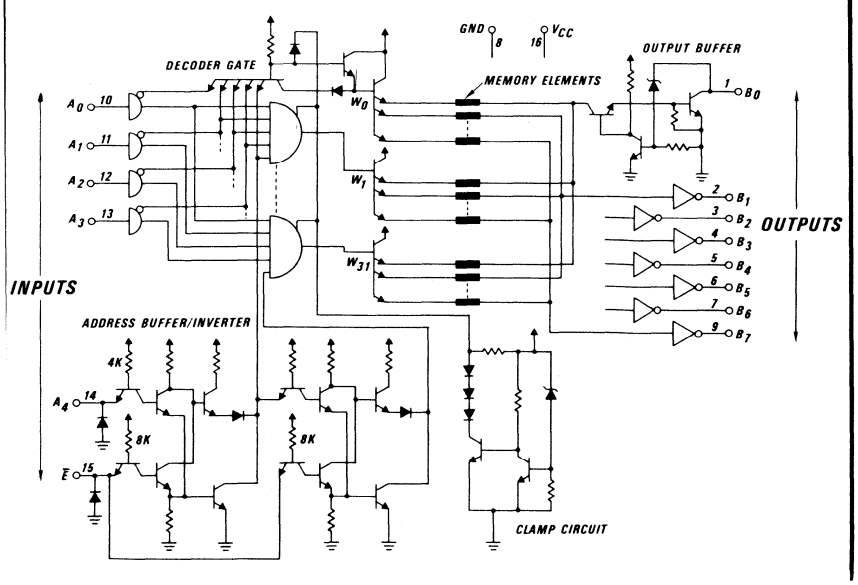
The HPROM-8256 is the third in a series of field programmable read-only memories from Harris Semiconductor. Field programming implies that the device (packaged with logical "0's" in all 256 memory locations) can be programmed electronically by the user to any specific pattern using the simple procedure shown on page 4.

Referring to the circuit diagram below, the status of any bit is determined by the condition of the "memory element" in that bit location. For a logical "0" output, the memory element is in the conducting state and the output transistor is turned "on". Programming, then, involves opening selected memory elements to prevent current flow to the output transistor, creating a logical "1" in each programmed bit location.

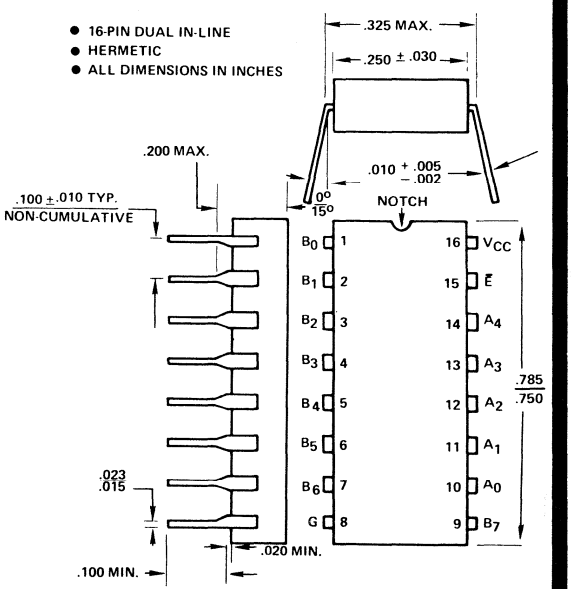
WORD	INPUTS						OUTPUTS							
NUMBER	$\bar{E}$	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
X	1	X	X	X	X	X	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
1	0	0	0	0	0	1	*	*	*	*	*	*	*	*
2	0	0	0	0	1	0	*	*	*	*	*	*	*	*
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
31	0	1	1	1	1	1	*	*	*	*	*	*	*	*

NOTE: X = DON'T CARE

CIRCUIT DIAGRAM



PACKAGE

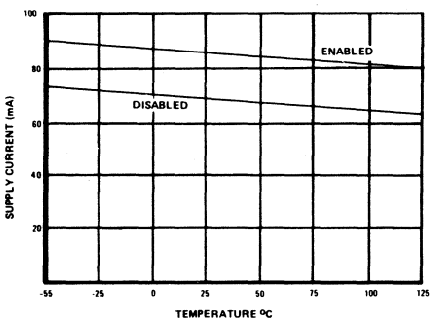


*PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.

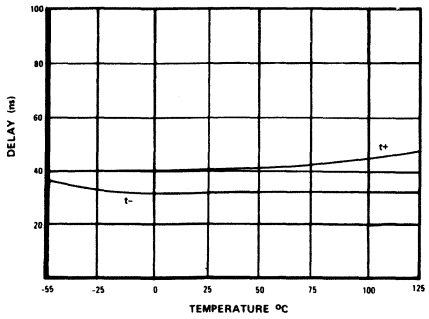
MEMORY DATA

CHARACTERISTIC CURVES

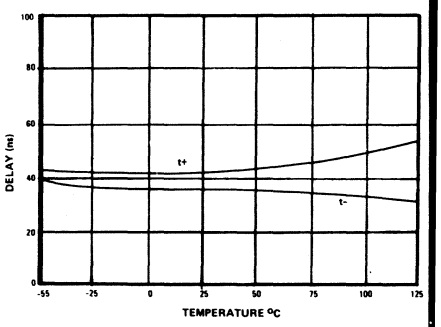
POWER SUPPLY CURRENT vs TEMPERATURE



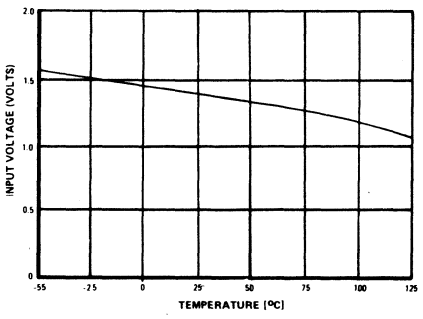
ADDRESS TO OUTPUT PROPAGATION DELAY vs TEMPERATURE



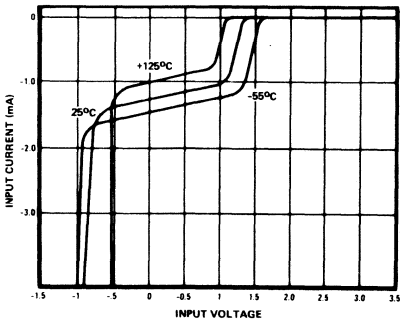
ENABLE TO OUTPUT PROPAGATION DELAY vs TEMPERATURE



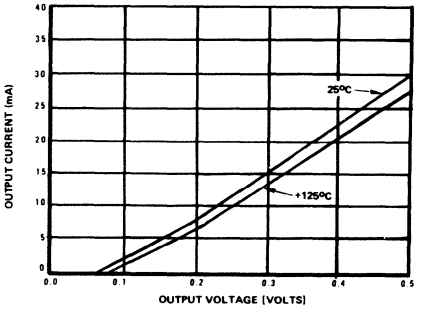
INPUT THRESHOLD vs TEMPERATURE



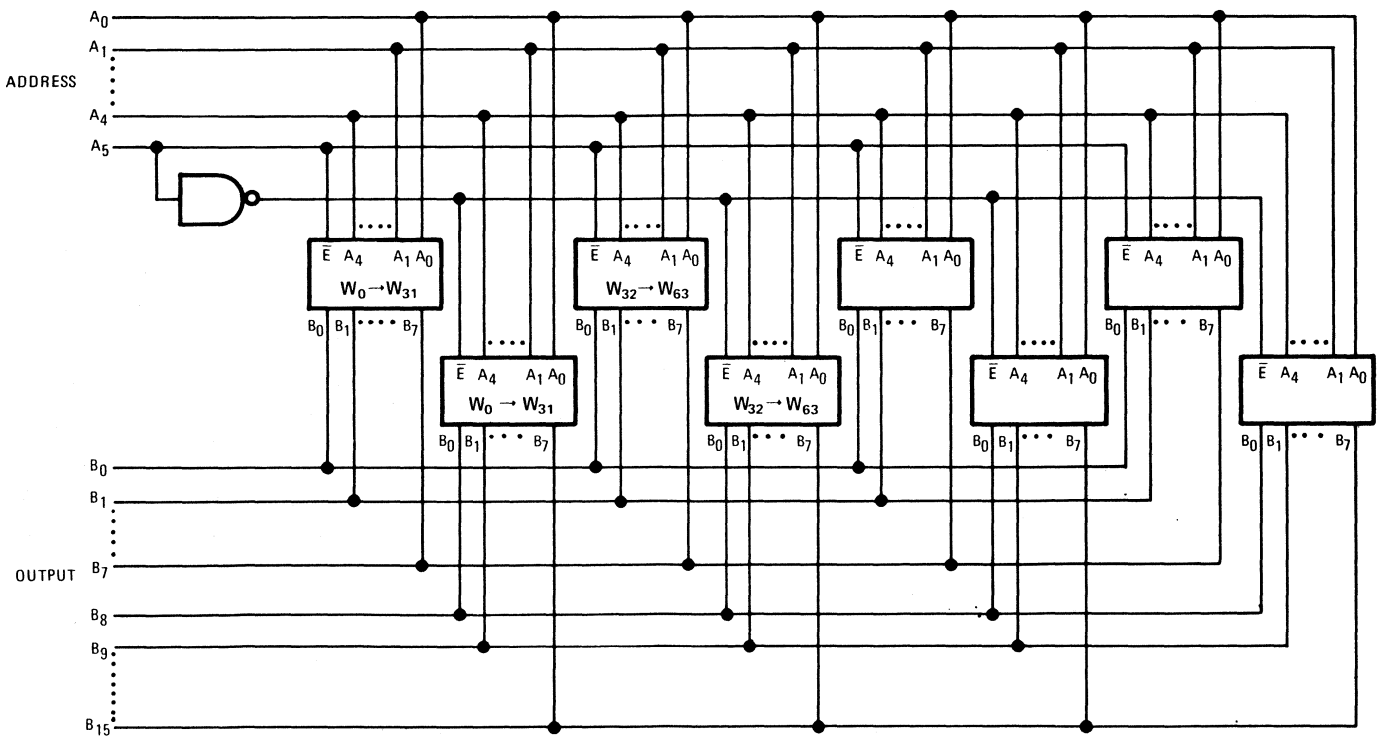
INPUT CURRENT vs INPUT VOLTAGE



OUTPUT LOW V-I CHARACTERISTICS



EXPANDABILITY



MEMORY DATA

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Operating), V_{CC}	7.0V
Address/Enable Input Voltage, V_A, V_E	−1.5V to +5.5V
Output Supply Voltage (Operating), V_{BS}	−1.5V to +7.0V
Output Sink Current, I_{OL}	−30mA
Input Current	−30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C

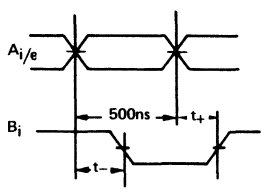
ELECTRICAL CHARACTERISTICS

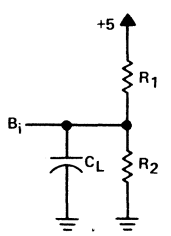
TEST CONDITIONS

HPROM-8256-2 (V_{CC} = +5.0V ±10%, T_C = -55°C to +125°C)
HPROM-8256-5 (V_{CC} = +5.0V ± 5%, T_A = 0°C to +75°C)

PARAMETER		SYM	HPROM-8256-2 (-55°C to +125°C) MIN	TYP	MAX	HPROM-8256-5 (0°C to +75°C) MIN	TYP	MAX	UNITS	TEST CONDITIONS
$\overline{\text{ENABLE}}$ Current	"1"	I_{RE}			100			100	µA	V_{IN} = 4.5V
	"0"	I_{FE}			-1.6			-1.6	mA	V_{IN} = 0.4V
Address Current	"1"	I_{RA}			100			100	µA	V_{IN} = 4.5V
	"0"	I_{FA}			-1.6			-1.6	mA	V_{IN} = 0.4V
Input Threshold Voltage	"1"	V_{IH}	2.0			1.9			V	
	"0"	V_{IL}			0.9			0.85	V	
Output "0" Voltage		V_{OL}			0.4			0.45	V	V_{CC}=V_{MIN}, I_{OL} = 10mA
Output "1" Leakage		I_{OH}			200			200	µA	V_{OH} = 5.25V
Input Clamp Voltage		V_C			-1.5V			-1.5V	V	I_{IN} = -5.0mA
Power Supply Current	(Quiescent)	I_{CC}			80			80	mA	V_E = V_{IH}, Outputs open
	(Operating)				100			110	mA	V_E = V_{IL}, Outputs open
Address/Enable to Output Fall Delay		t-		40	50		40	50	ns	R_1 = 470Ω, R_2 = 1KΩ, C_L = 30pF
Address/Enable to Output Rise Delay		t+		40	50		40	50	ns	T = 25°C, V_{CC} = 5.0V

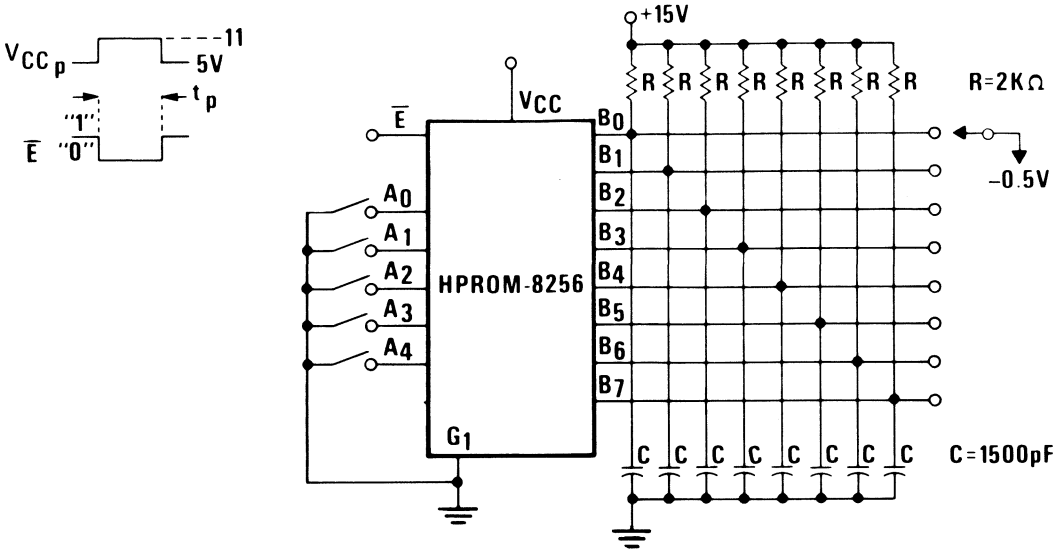
SWITCHING TIME DEFINITIONS





1. All measurements referenced to +1.5V.
2. Address rise and fall times ≤ 10ns.

PROGRAMMING



REQUIREMENTS

	RECOMMENDED VALUE	LIMITS MIN.	LIMITS MAX.	UNITS	NOTES
Enable/Address Input Low Current			-6.0	mA	V_{IN} = 0.4V
Programming Voltage (V_{CC_p})	11		11.5	V	I_{Limit} = 250mA
Programming Pulse Width (t_p)	200		800*	ms	*All devices should program with $t_p \leq$ 800ms.
Programming Output Voltage	-0.5	-1.0	0.0	V	
Non–Programming Output Current	4.0	2.0	8.0	mA	Output voltage nominally 8.3V.
T_{CASE}			75	°C	
Duty Cycle (T_A = 25°C)	60		80	%	

PROCEDURE

1. Connect the PROM as shown in figure 1.
2. Address the desired word by applying an open circuit for Logic "1" and ground for Logic "0".
3. Select first output bit to be programmed by taking that output to a negative 0.5V.
4. Dissable device (E $\geq$ 2.5V.). (Nonprogramming outputs will rise to approximately 8.3V.) Raise supply to +11V and enable device (E $\leq$ 0.4V) to program the selected memory element. (Enable signal must not be applied prior to raising V_{CC} to +11V.)
5. Disable device and select next bit to be programmed. Repeat step 3.

HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

HPROM-0512

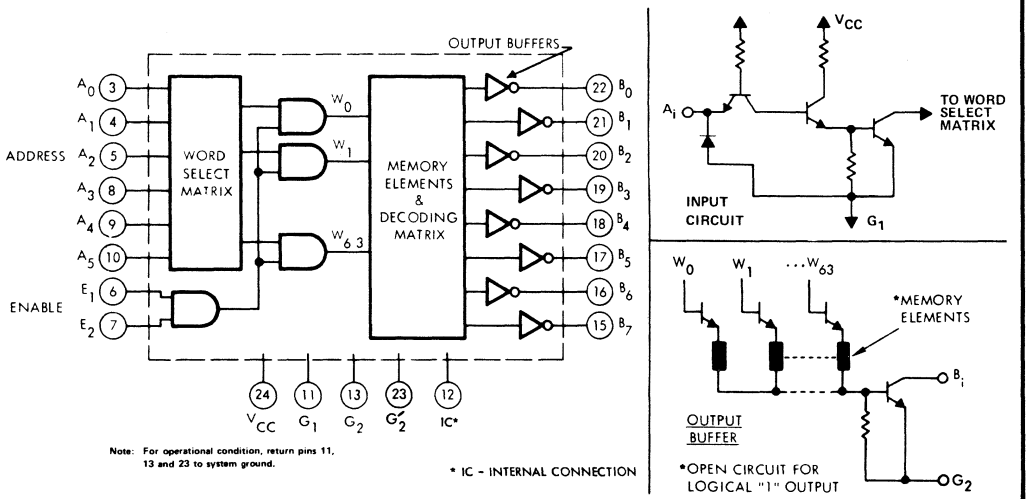
512-Bit, Bipolar PROM™*

FEATURES

- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 55 NS ACCESS TIME
- SINGLE 5 VOLT POWER SUPPLY
- STATIC OUTPUT WITH FANOUT OF 10
- AVAILABLE IN EITHER MILITARY OR COMMERCIAL TEMPERATURE RANGE
- EXPANDABLE – "WIRED-OR" OUTPUTS "AND" ENABLE INPUTS

BLOCK DIAGRAM

HPROM-0512

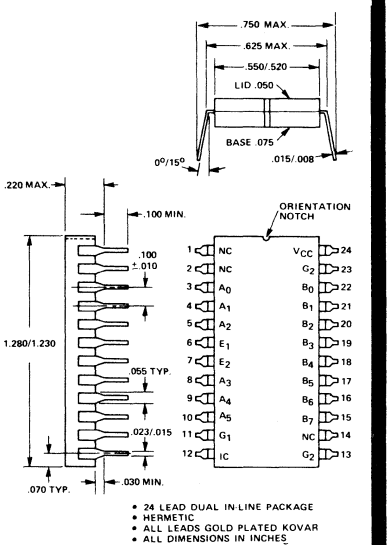


Note: For operational condition, return pins 11, 13 and 23 to system ground.

* IC - INTERNAL CONNECTION

*OPEN CIRCUIT FOR LOGICAL "1" OUTPUT

PACKAGE



* 24 LEAD DUAL IN-LINE PACKAGE
* HERMETIC
* ALL LEADS GOLD PLATED KOVAR
* ALL DIMENSIONS IN INCHES

TRUTH TABLE

Word Number	INPUTS							OUTPUTS							
	(1)E	A_5	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
(2)X	0	X	X	X	X	X	X	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	*	*	*	*	*	*	*	*
1	1	0	0	0	0	0	1	*	*	*	*	*	*	*	*
2	1	0	0	0	0	1	0	*	*	*	*	*	*	*	*
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
63	1	1	1	1	1	1	1	*	*	*	*	*	*	*	*

NOTE: (1) $E = E_1 \cdot E_2$ (2) X = "Don't Care"

FIELD PROGRAMMING

The HPROM-0512 is the first read-only memory which can be programmed electronically after manufacture and packaging. Most semiconductor read-only memories are programmed during manufacturing by designing the final metallization to correspond to the desired memory configuration. This process requires a different mask for each unique design and once the device is packaged, no further changes can be made. In contrast, the technique for programming the HPROM-0512 (see page 5) is straightforward and can be implemented at the user's facility with little difficulty.

Referring to the block diagram above, the status of any bit is determined by the condition of the 512 "Memory Elements" which connect the input word lines to each of eight (8) output bit buffers. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreverisible and cannot be accomplished under normal operating conditions – thus, the HPROM-0512 is a true permanent memory when inserted in a system.

*PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.

MEMORY DATA

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0V	Storage Temperature	−65°C to +150°C
Address/Enable Input Voltage, V_A, V_E	-1.5V to +5.5V	Operating Temperature (Case)	−55°C to +125°C
Output Supply Voltage, V_{BS}	-0.5V to +7.0V	θ_{JC} = 40°C/W	
Output Sink Current, I_{OL}	-30mA	θ_{JA} = 150°C/W	
Input Current	-30mA		

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0 ± 5%, $G_1 = G_2 = G_2' =$ Ground
T_{CASE} = −55°C to +125°C for HPROM-0512-2
0°C to +75°C for HPROM-0512-5
unless otherwise specified.

	PARAMETER		SYM	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITION
D.C.	Enable Current	"1"	I_{RE}		10	60	μA	V_E = 2.4V, V_{CC} = 5.25V
					30	100		V_E = 5.25V
		"0"	I_{FE}		−1.0	−1.6	mA	V_E = 0.4V, V_{CC} = 5.25V
	Address Current	"1"	I_{RA}		10	60	μA	V_A = 2.4V, V_{CC} = 5.25V
					30	100		V_A = 5.25V
		"0"	I_{FA}		−1.0	−1.6	mA	V_A = 0.4V, V_{CC} = 5.25V
	Input Threshold Voltage (1)	"1"	V_{IH}	2.0			V	V_{CC} = 4.75V
		"0"	V_{IL}			0.8	V	V_{CC} = 5.25V
	Output "0" Voltage		V_{OL}		0.25	0.45	V	V_{CC} = 4.75V, I_{OL} = 10mA, V_{IH} = 2.0V, V_{IL} = 0.8V
	Output "1" Leakage Current		I_{OH}			100	μA	V_{OH} = 2.4V
						200		V_{OH} = 5.25V
	Power Supply Current (3)	(Quiescent)	I_{CC}		70	95	mA	V_{CC} = 5.25V; $V_E = V_A$ = 0V
		(Operating)	I_{CC}		80		mA	V_{CC} = 5.25V; f = 4MB/s (2)
	Output Capacity		C_{OUT}		5		pF	V_{OUT} = 2.0V
A.C.	Address or Enable to Output Fall Delay (4)		t_-	25	55	75	ns	R_1 = 470Ω, R_2 = 1KΩ, C_L = 30pF, T_A = 25°C, V_{CC} = 5.0V
	Address or Enable to Output Rise Delay (4)		t_+	25	55	75	ns	

NOTES: (1) Threshold voltages are defined as the limits on the input levels which ensure that the desired input state is achieved.

(2) A typical device is one programmed to output 50% "ones".

(3) Output terminals left open —see Test Circuit 1.

(4) See Test Circuit 2.

MEMORY DATA

TEST CIRCUITS

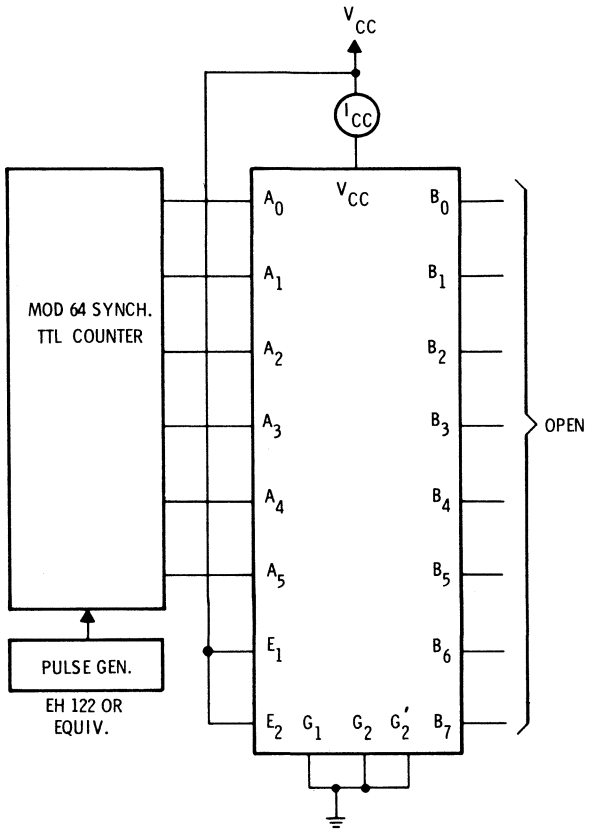


Figure 1.
OPERATING POWER SUPPLY CURRENT

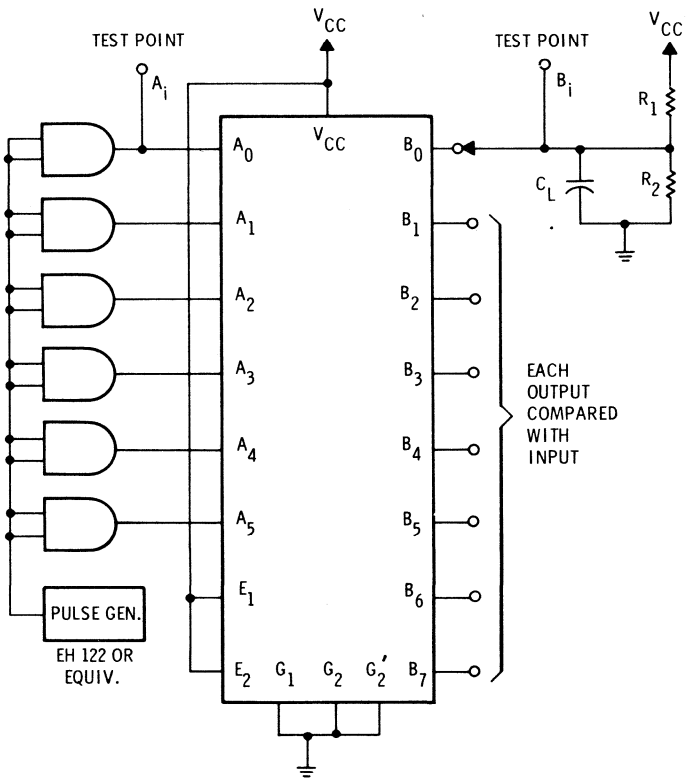
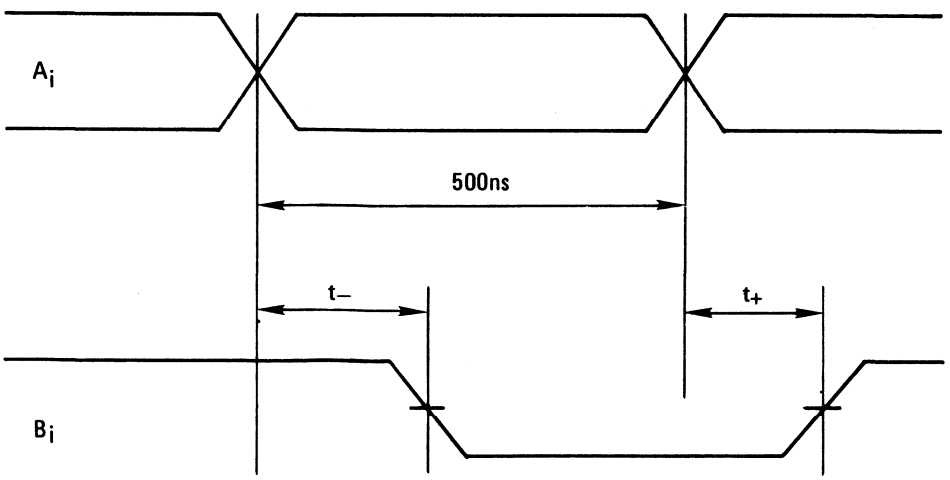


Figure 2.
PROPAGATION DELAYS

NOTE: Applies only to programmed units.

SWITCHING TIME DEFINITIONS



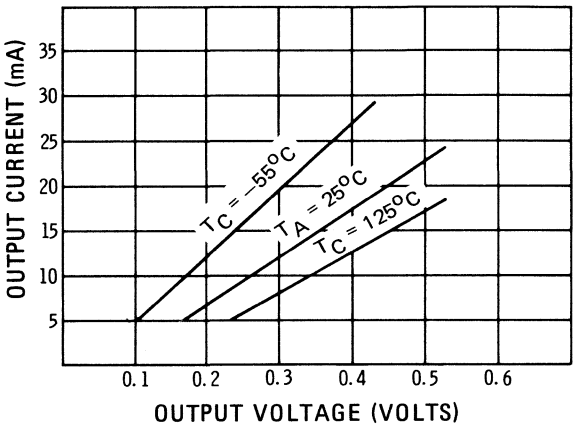
NOTES: (1) $E_1 = E_2 =$ "1"

(2) All measurements referenced to +1.5V level.

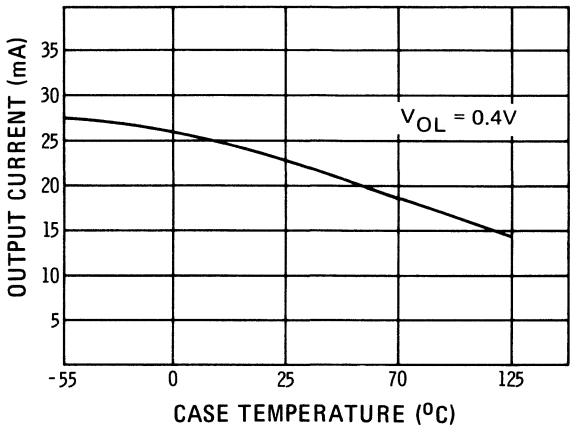
(3) Address rise and fall times $\leq$10ns.

CHARACTERISTIC CURVES

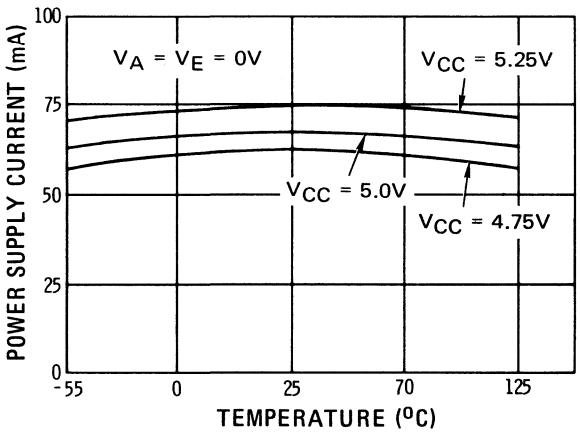
OUTPUT CHARACTERISTICS



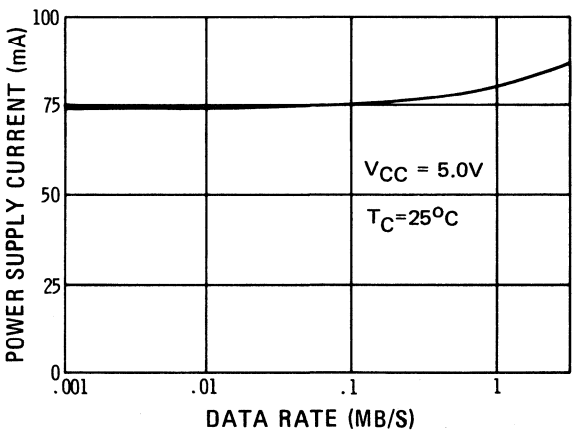
OUTPUT CURRENT VS. TEMPERATURE



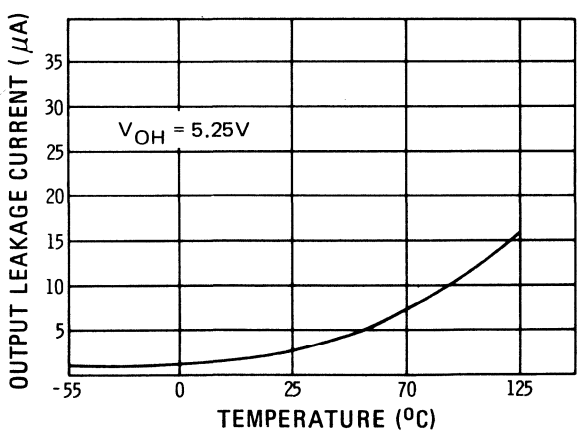
POWER SUPPLY CURRENT VS. TEMPERATURE



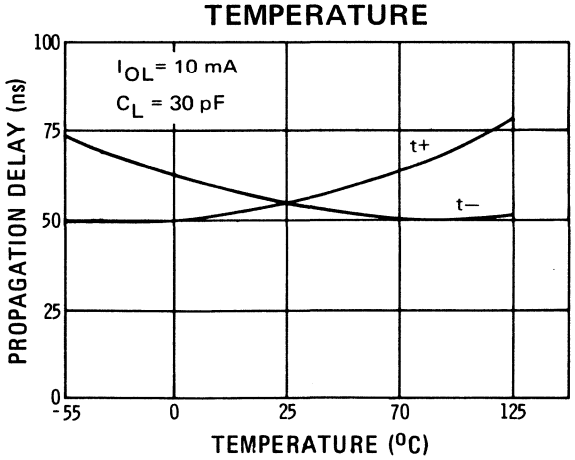
POWER SUPPLY CURRENT VS. DATA RATE



OUTPUT LEAKAGE CURRENT VS. TEMPERATURE



PROPAGATION DELAY VS. TEMPERATURE



TEST CONDITIONS: V_{CC} = 5.0V UNLESS OTHERWISE SPECIFIED.

PROGRAMMING SPECIFICATIONS

PARAMETER	SYM.	RECOMMENDED VALUE
Address Input Voltage "1"	V_{AH}	(1) Open Circuit
"0"	V_{AL}	−5.0V
Power Supply Voltage	V_{CC}	5.0V + 5% − 0% @ $I_{CC} \leq 250mA$
G_1 Voltage (2)	V_{G1}	−5.0V
G_2 Voltage	V_{G2}	0V
Programming Voltage (MAX)	$\overline{V}_{BP}$	−7.0V
Programming Current (MAX)	$\overline{I}_P$	100mA
Maximum Programming T_{CASE}	$\overline{T}_{CASE}$	75°C

(1) An open collector TTL gate meets this specification.

(2) G_1 must be connected to −5.0V prior to applying V_{CC} or programming voltage.

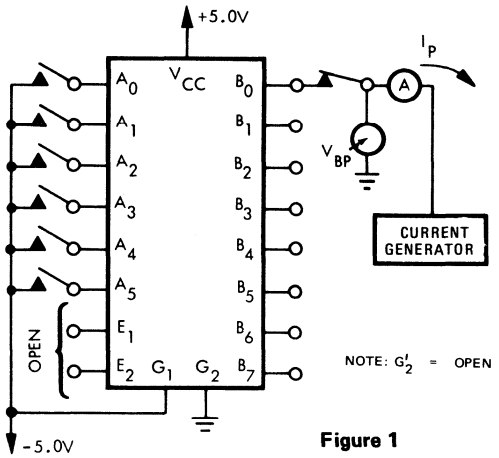


Figure 1
PROGRAMMING CONNECTIONS

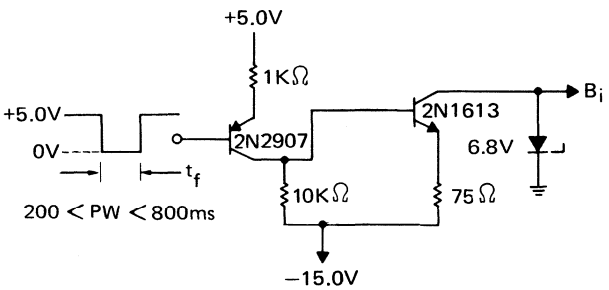


Figure 2
PROGRAMMING CIRCUIT

PROGRAMMING

Programming the HPROM-0512 is a simple operation which can be accomplished with a minimum of equipment. A negative going current ramp is applied to each output terminal where the initial logic "zero" is to be changed to a logic "one." The power supply and ground connections described below ensure that alteration of a specific logic element will not occur under normal operating conditions.

The following is the recommended procedure for reliably programming the HPROM-0512.

1. Connect the HPROM-0512 as shown in Figure 1. To address a particular word in memory, set the input switches to the binary equivalent of that word, where a logic "zero" is −5.0V and a logic "one" is an open circuit. (Do not return to supply.) All output bits (B_0, B_1 . . . . B_7) of this word are now available for programming.

2. With the output of the current generator limited to 100mA, apply a negative going pulse to the pin associated with the first bit to be changed from a "zero" to a "one." This is most easily accomplished by connecting the negative terminal of a variable power supply to the proper output pin and manually increasing the voltage to approximately 6.0V.

   (The circuit shown in Figure 2 can be used in more automated programming systems. This circuit generates a fusing pulse which is at the proper voltage and current levels for fast, reliable programming. Most devices will program with input pulse widths (PW) as low as 200ms.)

3. Skipping any bit which is to remain a "zero," repeat Step 2 for each "one" in the word being addressed. (For maximum reliability, program only one bit at a time.)

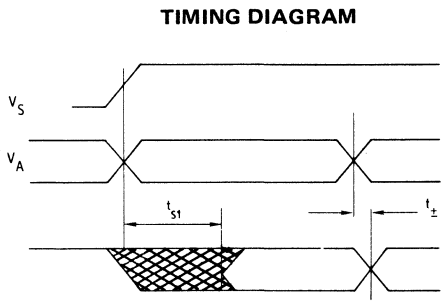
4. Set the next input address and repeat Steps 2 and 3. This procedure repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A "zero" can always be changed to a "one" simply by repeating Steps 1 and 2. A "zero" once programmed to "one" cannot be reprogrammed to "zero."

The procedure given above is intended merely to convey the mechanics of programming the HPROM-0512. Obviously, more sophisticated electronic methods can be devised to automate the process and minimize the time required for programming. Such a system is used by Harris to custom-program ROM's for customers whose memory configurations are already established and also for certain standard patterns. This particular system operates with punched card inputs which convey the programming information and also provide the test conditions for each programmed ROM.

APPLICATION INFORMATION

POWER STROBE

Since the HPROM-0512 is a permanent memory, V_{CC} may be removed from the chip during periods when the memory is not being accessed thus reducing the average power consumption. A circuit which performs this function is shown in Figure 1. Using the components shown, the propagation delay from the power strobe to the first output word (t_{s1}) becomes ~140ns. Figure 2 shows the variation in t_{s1} as a function of temperature.



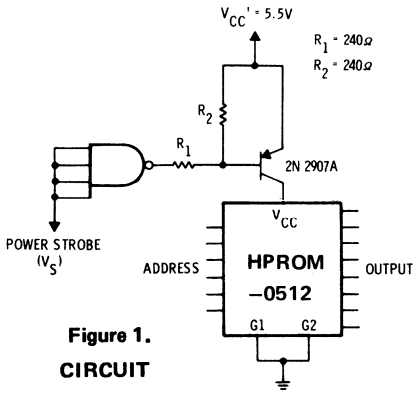


Figure 1.
CIRCUIT

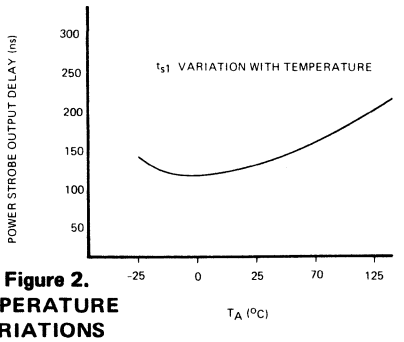
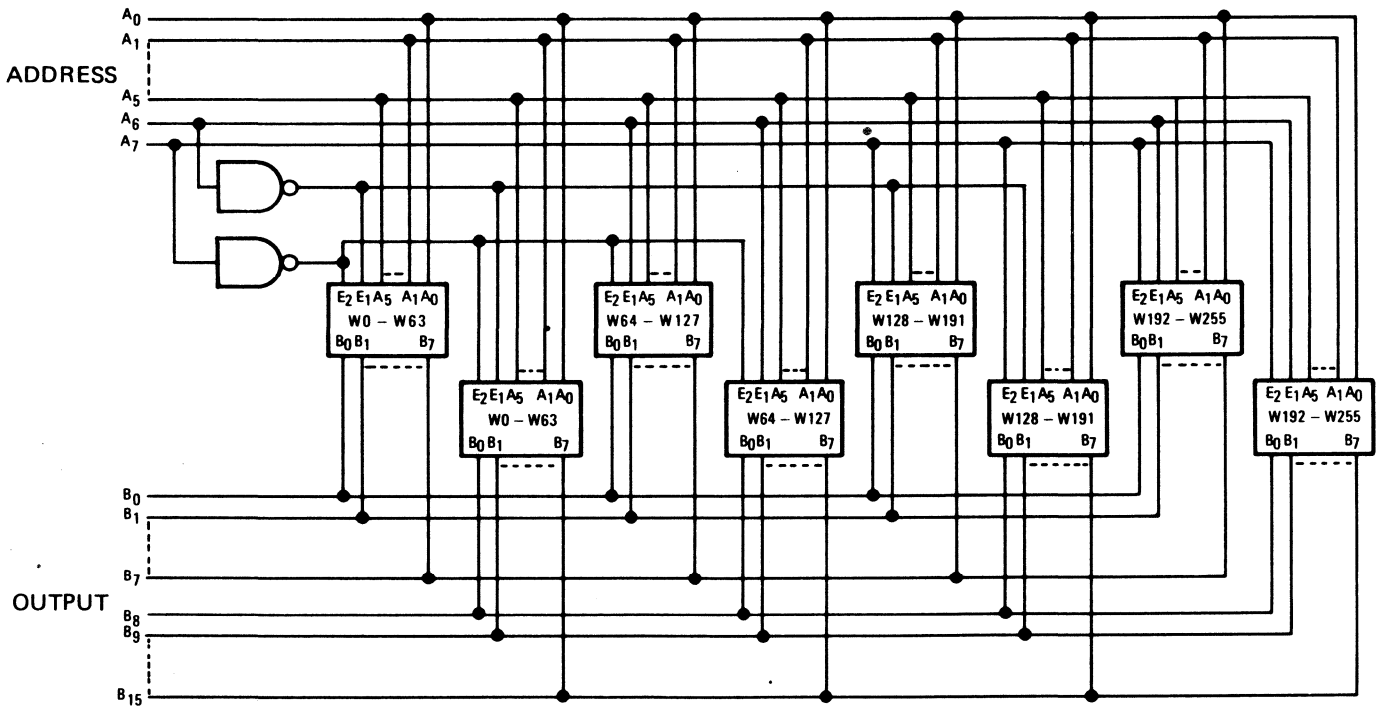


Figure 2.
TEMPERATURE VARIATIONS

EXPANDABILITY



The HPROM-0512 is easily expanded in both bit and word dimensions. Expanding in the word dimension is accomplished by using the E_1 and E_2 Enable Inputs as further decoding elements for the input address and wiring together (WIRE-OR) two or more output pins from corresponding bits of different words. The "WIRE-OR" connection results in increased capacitance and leakage at the output node as each additional package is connected. Expansion in the bit dimension is accomplished by paralleling corresponding address pins on two or more units. The Block Diagram above depicts a 256 word by 16-bit system.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

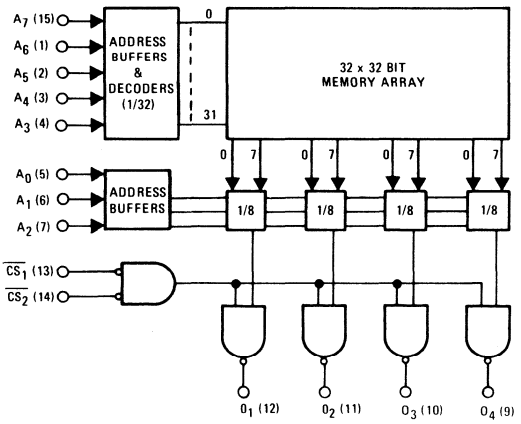
HPROM-1024/1024A

1024-Bit Field Programmable Bipolar PROM™

FEATURES

- FIELD PROGRAMMABLE
- 256/4 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 50ns ACCESS TIME
- PROVEN RELIABLE NICHROME FUSES
- LOW INPUT CURRENT ≤ 0.25mA
- SINGLE 5.0V POWER SUPPLY
- EXPANDABLE – "WIRED-OR" OUTPUTS WITH WITH CHIP SELECT INPUT
- AVAILABLE IN MILITARY AND COMMERCIAL TEMPERATURE RANGES

BLOCK DIAGRAM



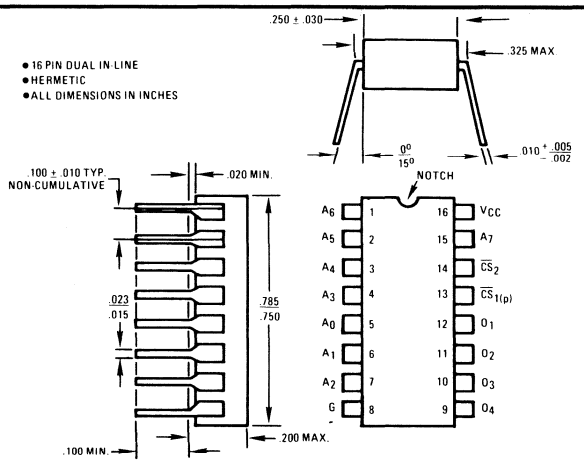
DESCRIPTION

The HPROM-1024 (3-State) and the HPROM-1024A (Open Collector) are fully decoded, high speed, 1024-bit, field programmable ROM's organized as 256 words by 4 bits per word. Field programmable implies that, by following a simple programming procedure, users are able to program the PROM to any custom pattern to satisfy their system requirements.

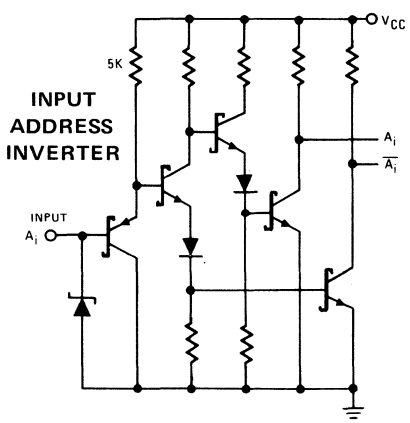
The HPROM-1024 and the HPROM-1024A are identical except for the output stage. The HPROM-1024A has an Open Collector output while the HPROM-1024 has a third high impedance state output, allowing the device to work in a "Wire – OR" configuration. The third state is activated by disabling the device ($\overline{CS}_1$ or $\overline{CS}_2$ High).

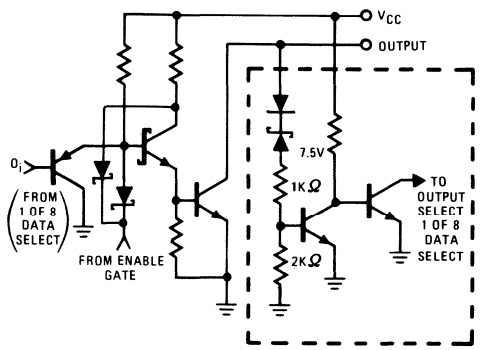
The HPROM-1024/1024A are supplied with all bits storing a Logical "1" (Output High) and can be selectively programmed for a Logical "0" (Output Low). The addressing scheme for programming and reading the information in the system is the same.

PACKAGE

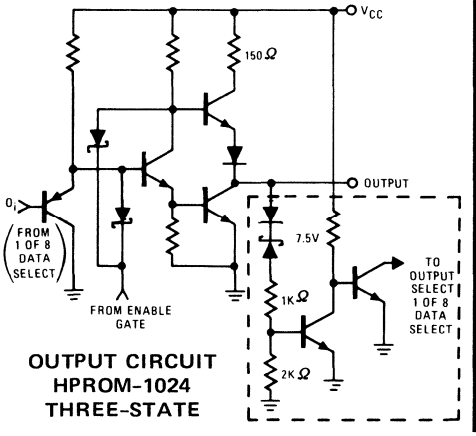


INPUT/OUTPUT SCHEMATICS





OUTPUT CIRCUIT
HPROM-1024A HPROM-1024
OPEN COLLECTOR



OUTPUT CIRCUIT
HPROM-1024
THREE-STATE

MEMORY DATA

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

Output or Supply Voltage	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Case)	+125°C
Maximum Junction Temperature	+175°C

Note:

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (Operating Mode)

TEST CONDITION: V_{CC} = 5.0± 5%, T_C = -55°C to + 125°C (HPROM-1024-2, HPROM-1024A-2)
V_{CC} = 5.0± 5%, T_A = 0°C to +75°C (HPROM-1024-5, HPROM-1024A-5) unless otherwise specified.

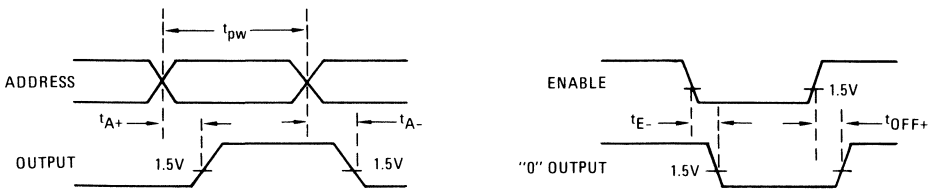
	PARAMETER		SYMBOL	HPROM-1024 MIN.	HPROM-1024 TYP.	HPROM-1024 MAX.	HPROM-1024A MIN.	HPROM-1024A TYP.	HPROM-1024A MAX.	UNITS	TEST CONDITIONS
D.C.	Address/Enable Input Current	"1"	I_{RA}, I_{RE}			40			40	µA	$V_{IH} = V_{CC}$ Max.
		"0"	I_{FA}, I_{FE}			-0.25			-0.25	mA	V_{IL} = 0.45V
	Input Clamp Voltage		V_C		-0.7	-1.0		-0.7	-1.5		$V_{CC} = V_{CC}$ Min. I_C = 10mA
	Input Threshold Voltage	"1"	V_{IH}	2.0			2.0			V	
		"0"	V_{IL}			0.8			0.8	V	
	Output Voltage	"1"	V_{OH}	2.4					N.A.	V	
		"0"	V_{OL}			0.45	N.A.	N.A.	0.45	V	I_{OL} = 15mA
	Output Leakage	"1"	I_{OH}	N.A.	N.A.	N.A.			100	µA	$V_{OH} = V_{CC}$ Max.
	Output Disabled Current		$I_{O\overline{E}}$			100			100	µA	V_{OH} = 2.4V, V_{E1}/V_{E2} = 2.0V
	Power Supply Current		I_{CC}			130			130	mA	All Inputs Grounded. $V_{CC} = V_{CC}$ Max.
A.C.	Address to Output		t_{A+}		50	70		50	70	ns	T_A = +25°C
			t_{A-}		50	70		50	70	ns	
	Enable Access Time		t_{E-}		20	35		20	35	ns	V_{CC} = 5.0V
			t_{off+}		20	35		20	35	ns	

CAPACITANCE (1): T_A = 25°C

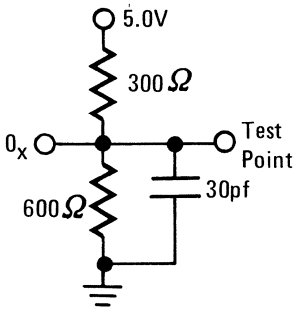
PARAMETER	SYMBOL	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITION	
Add. Input Cap.	$C_{IN\ A,\ CS2}$	7	15	pf	V_{CC} = 5V V_{IN} = 2.0V	T_A = 25°C
Chip Select Input Cap.	C_{CS1}	10	20	pf	V_{CC} = 5V V_{IN} = 2.0V	
Output Cap.	C_{OUT}	6	12	pf	V_{CC} = 5V V_{OUT} = 2.0V	

NOTE (1): These parameters are only periodically sampled and are not 100% tested.

SWITCHING TIME DEFINITIONS



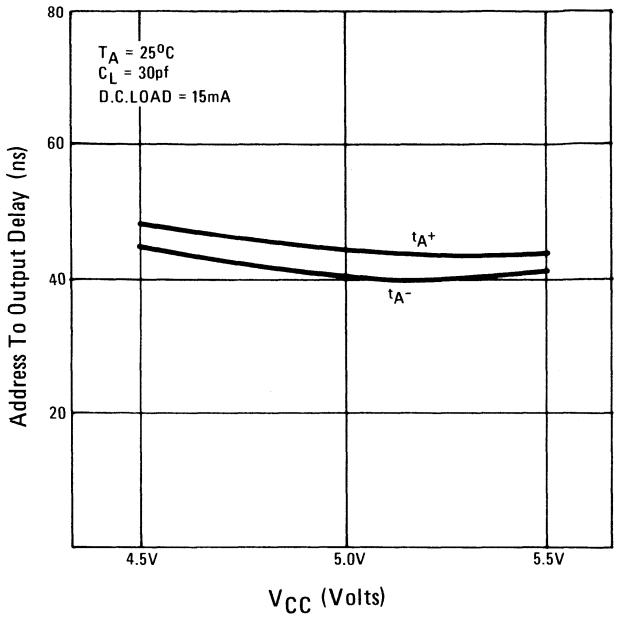
A.C. TEST LOADS



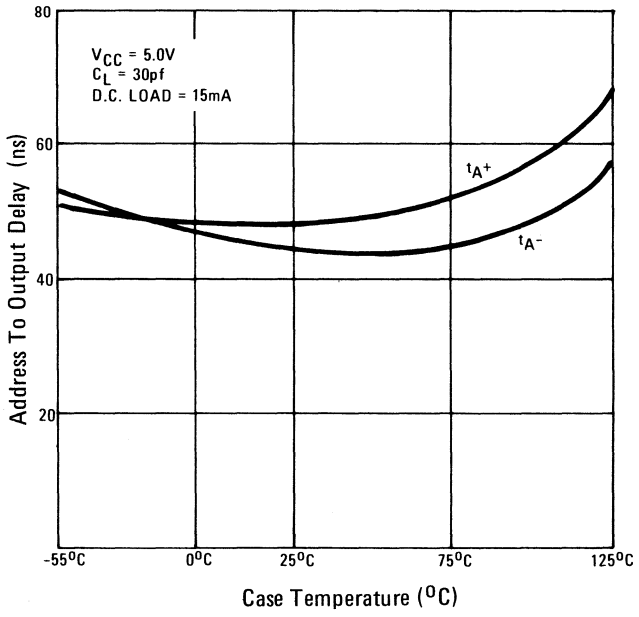
MEMORY DATA

TYPICAL A.C. CHARACTERISTICS

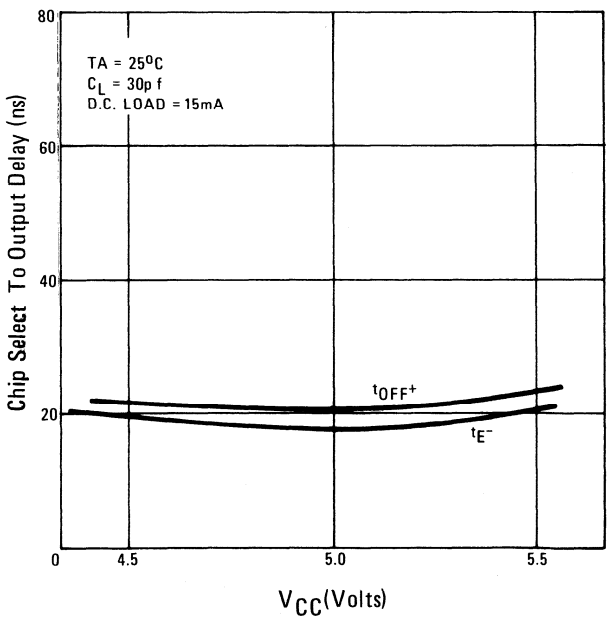
ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



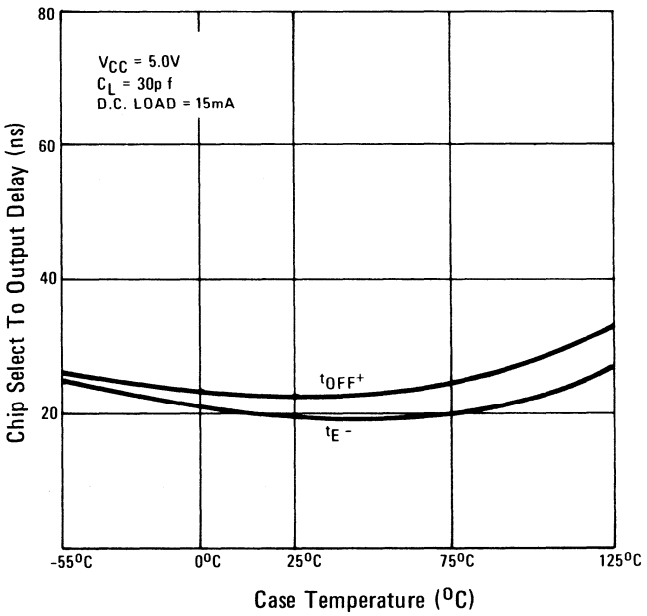
ADDRESS TO OUTPUT DELAY
VS. CASE TEMPERATURE



CHIP SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



CHIP SELECT TO OUTPUT DELAY
VS. CASE TEMPERATURE



MEMORY DATA

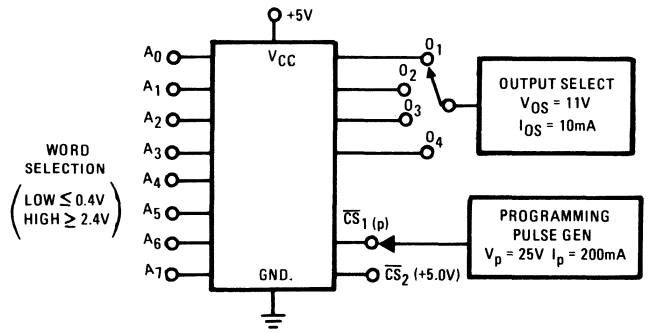
PROGRAMMING

The HPROM-1024/1024A is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HPROM-1024/1024A can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN.	RECOMMENDED VALUE	MAX.	UNITS.	NOTES
Address Input Voltage	V_{IH}	2.4	5.0	5.0	V	Address inputs should not be left open for V_{IH}.
	V_{IL}	0.0	0.0	0.4	V	
Chip Select 2 Voltage (Pin 14)	$V_{\overline{CS2}}$	2.4	5.0	5.0	V	
Programming Voltage $\overline{CS}_1$ (Pin 13)	$V_{\overline{CS1}}$ (P)	24.0	25	25.5*	V	*Including overshoot
Programming Current Limit $\overline{CS}_1$ (Pin 13)	$I_{\overline{CS1}}$ (P)		200	300	mA	125mA is the typical programming current requirement.
Programming Pulse Width	T_{PW}	10	20	100	mS	$t_{RISE} \leq 1\mu s$
Output Select Voltage	V_{OS}	10.5	11	11.5	V	
Output Select Current limit	I_{OS}		10	20	mA	2mA is the typical current requirement.
Power Supply Voltage	V_{CC}	5.0	5.0	5.25	V	
Case Temperature	T_C	-25	25	75*	°C	*20% duty cycle with $T_A = 25°C$

MANUAL PROGRAMMING



The HPROM-1024/1024A may be programmed using the method shown in the figure above.

(1) Select the word to be programmed by applying the appropriate voltages to the address pins A_0 through A_7.

(2) Apply 11.0 volts to the output associated with the bit to be programmed. The other outputs may be left open or connected to any normal circuitry which does not apply more than 5 volts to these outputs. Only one output is programmed at a time.

(3) Apply the 25 volt programming pulse to the Input Pin $\overline{CS}_1$ (Pin 13). The recommended programming pulse width is 20ms, however, 10ms is generally adequate for most devices. Bits which do not program with these pulse widths may be programmed either by repeating the 10ms or 20ms pulses, or by increasing the programming pulse width to 100ms. The multiple application of the programming pulse or the increased pulse width in no way affects the reliablity of the device. The case temperature of the device being programmed, however, must not exceed 75°C. The 20% duty cycle (at T_A = 25°C) generally maintains a T_{CASE} of 75°C.

(4) To verify that the output has been programmed following each application of the programming pulse, bring Pin 13 and Pin 14 to 0.4 volts or less.

(5) The above procedure is repeated to program other bits on the chip.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

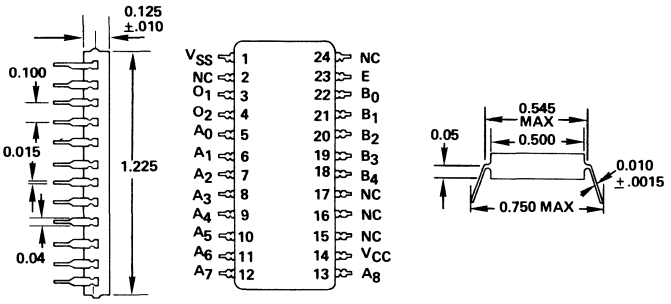
HROM-2560/2561

2560-Bit, MOS Read-Only Memory for Horizontal, 5x7 Dot Matrix Character Generator

FEATURES

- LOW POWER - 50mW AT 1 MHz
- SIMPLE TTL INTERFACE
- STATIC CHARGE PROTECTION
- STANDARD 24-PIN DUAL IN-LINE PACKAGE
- HPROM-2561 CONTAINS STANDARD ASCII TO 5 x 7 DOT MATRIX PATTERN
- FULLY DECODED - 512 WORDS/5 BITS PER WORD
- EXPANDABLE – "WIRED-OR" OUTPUTS/CHIP ENABLE INPUT

PACKAGE

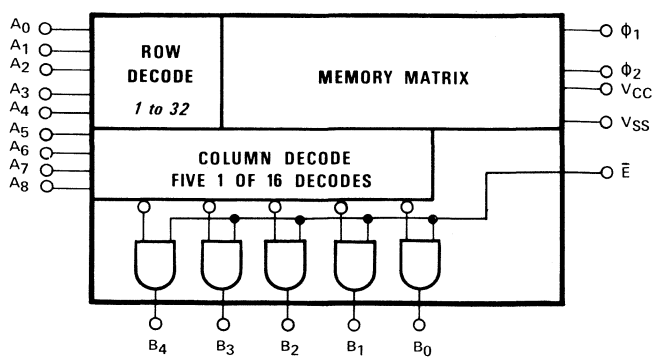


SAMPLE MEMORY PATTERN

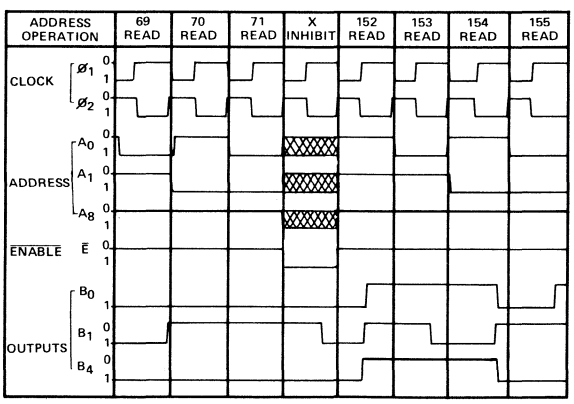
WORD	INPUTS E	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OUTPUTS B_4	B_3	B_2	B_1	B_0
X	1	X	X	X	X	X	X	X	X	X	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
65	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
66	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1
67	0	0	0	1	0	0	0	0	1	0	1	0	0	0	1
68	0	0	0	1	0	0	0	0	1	1	1	0	0	0	1
69	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1
70	0	0	0	1	0	0	0	1	0	1	1	0	0	0	1
71	0	0	0	1	0	0	0	1	1	0	1	0	0	0	1
72	0	0	0	1	0	0	0	1	1	1	1	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
153	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
154	0	0	1	0	0	1	1	0	0	1	0	1	1	1	0
155	0	0	1	0	0	1	1	0	1	0	1	0	0	0	1
156	0	0	1	0	0	1	1	0	1	1	1	0	0	0	0
157	0	0	1	0	0	1	1	1	0	0	0	1	1	1	0
158	0	0	1	0	0	1	1	1	0	1	0	0	0	0	1
159	0	0	1	0	0	1	1	1	1	0	1	0	0	0	1
160	0	0	1	0	0	1	1	1	1	1	0	1	1	1	0

Notes: X=Don't Care, "0"=0.0V, "1"=-12.0V

BLOCK DIAGRAM



TYPICAL OPERATING SEQUENCE



MEMORY DATA

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

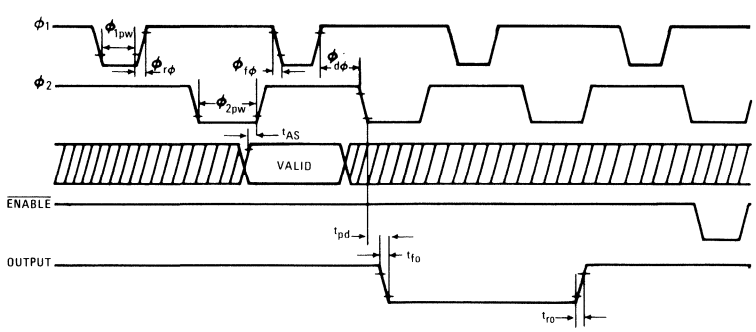
Power Supply Voltage, V_{SS}	0 to +30V
Address, Clock, Enable Inputs V_A, V_Φ, V_E	(V_{SS} −40.0) to (V_{CC} +0.3V)
Power Dissipation	300mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{SS}=+10.0V ±10%, V_{CC}=+5.0V ±10%, T_A=−55°C to +125°C unless otherwise specified

	PARAMETER		SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Clock Voltage	"0" "1"	$V_{\Phi H}$ $V_{\Phi L}$	4.5 −22.5		5.5 −19.5	V V	See Note 1 See Note 1
	Address/$\overline{\text{Enable}}$ Voltage	"0" "1"	V_{AH}, $V_{\bar{E}H}$ V_{AL}, $V_{\bar{E}L}$	4.0		5.5 0.4	V V	See Note 1 See Note 1
	Clock Leakage		$I_{\Phi L}$			−100	μA	T_A = 25°C V_Φ = −22.5V
	Address/$\overline{\text{Enable}}$ Leakage		I_{AL}, $I_{\bar{E}L}$			−1.0	μA	V_A = $V_{\bar{E}}$ = 0V
	Clock Capacitance	Φ_1 Φ_2	$C_{\Phi 1}$ $C_{\Phi 2}$		25 20		pF pF	V_Φ = +5.0V T_A = 25°C
	Address Capacitance		C_A		8.0		pF	T_A = 25°C V_A = +5.0V
	Enable Capacitance		C_E		6.0		pF	T_A = 25°C $V_{\bar{E}}$ = +5.0V
	Output Voltage		V_{OH}	2.4	3.3		V	I_{OH} = +3.3mA
	Output Resistance		R		300			V_{OH} = 2.4V T_A = 25°C
	Power Dissipation		P_{AC}		50		mW	See Note 2
A.C.	Clock Rep. Rate		F_Φ	0.1		1.5	MHz	$t_{r\Phi} \leq$ 15ns $t_{f\Phi} \leq$ 15ns
	Clock Pulse Width	Φ_1 Φ_2	Φ_{1pw} Φ_{2pw}	350 250			ns ns	
	Clock Rise Time		$\Phi_{r\Phi}$			100	ns	
	Clock Fall Time		$\Phi_{f\Phi}$			100	ns	
	Clock Delay		Φ_d	0		4.7	μs	
	Address Set Up Time		t_{AS}	0			ns	
	Output Delay Time		t_{pd}			150	ns	R_L = 2.2K C_L = 30pF T_A = 25°C V_{CC} = 5.0V
	Output Rise Time		t_{ro}		100			
	Output Fall Time		t_{fo}		100			

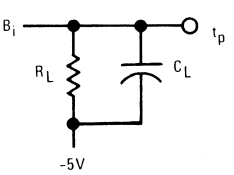
SWITCHING TIME DEFINITIONS



NOTES:

1. For V_{CC} different from that specified.
   $V_{OH,EH,AH} \geq V_{CC}$ -1.0V
   $V_{EL,AL} \leq V_{CC}$ - 4.1V
   $V_{OL} \leq V_{CC}$ - 24.0V
2. Dissipation shown is A.C. only. No D.C. power is dissipated except in output stage.

TEST LOAD:



MEMORY DATA

HARRIS SEMICONDUCTOR

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APPLICATION NOTE 201

DIODE MATRICES (4 × 10, 10 × 4)

BY D. C. UIMARI

GENERAL DESCRIPTION

The 4 x 10 and 10 x 4 diode matrices are particularly useful in decimal to BCD and BCD to decimal conversion applications. The two variations of the basic "40-bit" matrix allow these units to be used with input data of either polarity. For example, a decimal to BCD converter where the decimal number is represented by a positive voltage level can be realized with the 4 x 10 matrix as shown in Figure 1(a). In this system, the input circuitry may consist of ten single pole switches connected to a positive reference level or a logic gate whose outputs are low unless turned on by a particular decimal number.

In some systems, however, one may wish to indicate the presence of a particular decimal number by a ground or low voltage condition. For example, if the input switches described above were returned to ground, (which in some ways is a more desirable situation) the decimal inputs would be 0 volts when the switch is actuated and an open circuit when the switch is not actuated. Similarly, most line driver I.C.'s are designed as 4-Input NAND gates which generate low voltages for positive inputs.

For either situation, the 10 x 4 diode matrix patterned as shown in Figure 1(b) could be used to generate positive logic BCD numbers from negative logic decimal numbers.

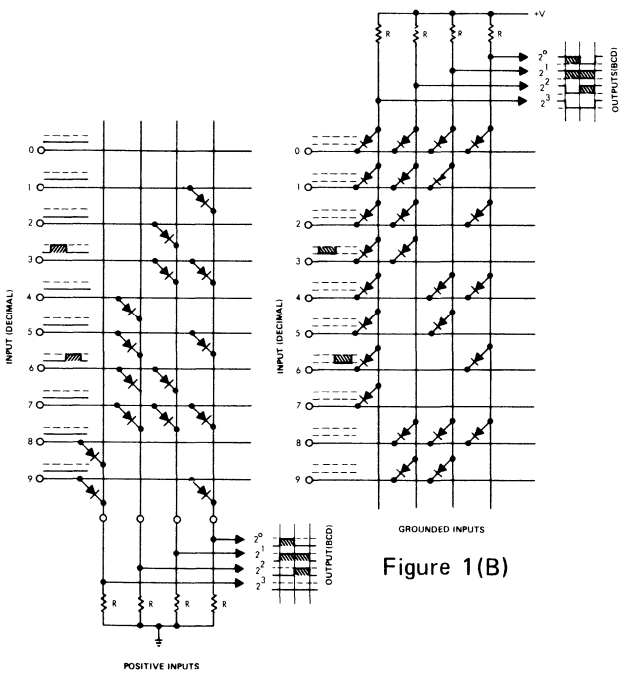


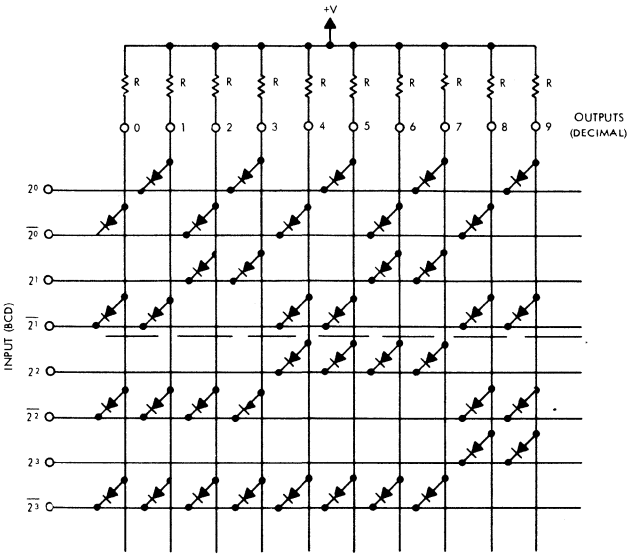
Figure 1(B)

Figure 1(A)

BCD to decimal conversion can also be accomplished with these circuits. Here, two matrices are required to accommodate each BCD digit and its complement. A typical arrangement is shown in Figure 2.

APP. NOTES

The most likely systems which would utilize decimal to BCD encoding are numerical keyboards, calculators, test equipment etc. BCD to decimal decoding would be used in displays, printers, calculators, etc. In general, encoding is required when an operator communicates with any digital system and decoding is required when the digital system communicates with the operator.



HARRIS SEMICONDUCTOR

A DIVISION OF HARRIS-INTERTYPE CORPORATION

APPLICATION NOTE 202

HPROM-0512 BIPOLAR PROM™*

GENERAL DESCRIPTION

The Field-Programmable HPROM-0512 is a 512-bit, bipolar read-only memory configured in a 64 word by 8-bit format. The unique feature of this device is the fact that any of the 512 bits can be electronically programmed by the user with standard equipment found in any electronics laboratory. Thus, a custom-programmed, 50ns memory can be obtained without incurring the additional mask charges and four to eight week turnaround time inherent in using the more conventional mask-programming approach.

A block diagram of the HPROM-0512 is shown in Figure 1. The 6-bit ADDRESS INPUT data is buffered and inverted and the true or compliment data is routed to each of six inputs on the 64 multiple-emitter AND gates. A seventh input to these gates is connected to the chip "ENABLE," so that a logical "zero" on the "ENABLE" input keeps all gate outputs in the low or "zero" state and all ROM outputs in the high or "one" state.

*PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.

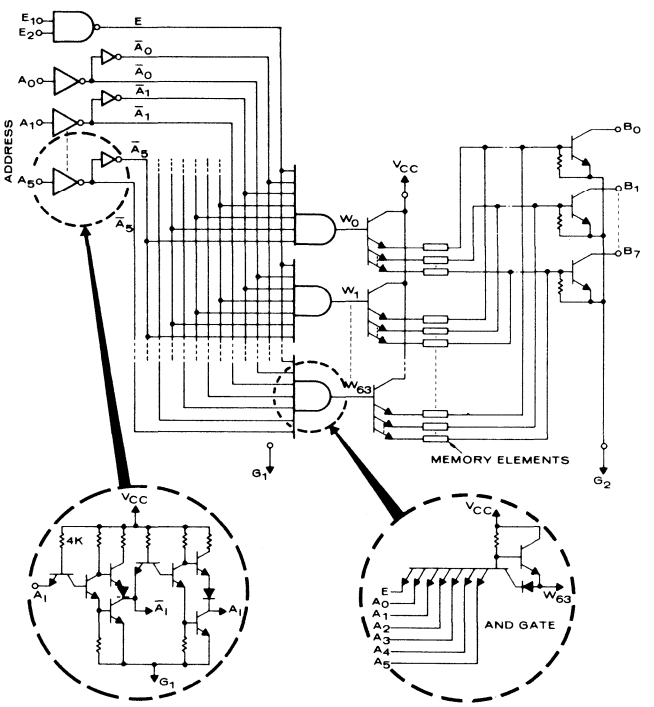


Figure 1

When the ENABLE is brought high, however, one of the 64 AND gates will have all of its inputs high, generating a logical "one" on one of the 64 word lines connected to each gate output. These word lines are connected to the bases of the 64 multiple-emitter transistors located in the memory section of the circuit. These transistors provide current gain, and isolate the selected memory elements from the unselected word lines.

APP. NOTES

The eight memory elements connected to the selected multiple-emitter transistor conduct a sufficient amount of current to turn on their respective output transistors. With the proper resistive load connected to their collectors, these transistors will saturate and a low voltage — or logical "zero" — will appear at the output terminals.

Since the only current path to a specific output transistor is through a selected memory element, the presence of that element corresponds to a logical "zero." To generate a logical "one" in a specific output bit position, the current path between the selected word line and the output transistor must be opened by removing the memory element which connects the selected multiple-emitter transistor and the output transistor.

In conventional mask-programmed ROM's, the elements are removed during the metallization process by designing the metallization mask with the aluminum interconnect removed in those areas where a logical "one" is specified. Therefore, a special mask must be generated for each different ROM pattern, incurring additional design costs and increasing turnaround time whenever a custom-programmed ROM is required. This is completely avoided with the field-programmable HPROM-0512, since the memory elements on this device can be removed electronically after the circuit has been metallized, packaged, and tested. Moreover, the technique for programming the HPROM-0512 is extremely simple and can be applied by the eventual user of the device with virtually no special equipment and with very little, if any, special training. A complete description of the programming requirements will be presented in a later section of this application note.

Since the HPROM-0512 is designed with high speed, TTL logic circuits, its operating characteristics are similar to most other bipolar ROM's currently on the market. The access time, for example, is typically 50 ns (75 ns worst case) at room temperature. The input circuit represents a fan-in of one and the output transistor is designed to sink 16 mA in its "on" state, which corresponds to a fan-out of ten. The unit is designed to operate over the full military temperature range (-55°C to +125°C) as well as the industrial temperature range (0°C to +75°C).

Two features are included on the HPROM-0512 which allow the memory to be conveniently expanded in the word dimension. The first of these is the open collector outputs which permit the direct connection of corresponding bits of parallel ROM's, forming a "wired-OR" of each output so connected. The second feature is the two ENABLE inputs which are ANDed on the chip to provide another level of address decoding through the chip select mechanism. To enable the HPROM-0512, both ENABLE inputs must be at logical "one."

ADVANAGES OF FIELD PROGRAMMING

There are two major advantages of field-programming, the first of which is the avoidance of the mask charges inherent in ROM's patterned in the conventional manner. While this is an obvious benefit to the small volume, small system manufacturer, it can also provide economic advantages in large volume, large system applications. For example, many large systems employ fifty to a hundred ROM's per system so that a hundred unit

production run amounts to a significant number of ROM's. In many of these situations, however, the number of different ROM patterns is almost as great as the number of ROM's per system, so that, economically, the situation here is quite similar to that of the small volume user as far as the impact of mask charges are concerned. In both cases, field-programming can provide a more economical alternative.

The other major advantage of field-programming is the avoidance of the four to eight week turnaround time required by semiconductor manufacturers to produce custom-programmed ROM's. With the HPROM-0512, a custom-programmed device can be obtained in a matter of minutes, thereby drastically cutting lead time, design time, and manufacturing time in a large variety of different situations. This advantage is particularly beneficial in modular/custom systems, where the specific system configuration--and hence the ROM pattern--varies from application to application. It has also been found useful in transducer calibration systems where the ROM must be matched to each individual transducer.

Field-programmable ROM's are also useful in the design, prototype, and initial production phases of new system designs. The advantages of the field-programming concept are apparent when the costs of design and programming errors are considered; but one should also consider the additional flexibility allowed by using this device prior to committing an entire design to production. Last minute design changes — which would have serious economic implications using the conventional programming approach — are easily accommodated using field-programming. Once a design is firmly established, completely automatic programming techniques can be employed which make the HPROM-0512 economically competitive with conventional mask programmed devices at substantial quantity levels. Thus the HPROM-0512 can be used in almost any application, regardless of eventual quantities. While some situations will require a field-programmable device only for design verification and system performance evaluation, other applications will find the HPROM-0512 economically superior throughout the system production run.

BASIC PROGRAMMING CONSIDERATIONS

The programming component in the HPROM-0512 is the memory element shown in the block diagram of Figure 1. When the circuit is manufactured and packaged, all 512 memory elements are intact, providing a low resistance path between the 64 word lines and the eight output buffers. To program a specific output bit to a logical "one," the memory element representing that specific bit must be effectively removed from the matrix, thus opening the path from the selected word line to the output transistor. This prevents the output transistor from turning on; no collector current flows, and the voltage at the output terminal is the same as the supply voltage. Thus programming a specific bit corresponds to writing a logical "one" in that particular memory cell.

To remove a selected memory element, it is necessary to increase the current through that element to the point where the heat generated causes the metal to flow and separate in much the same fashion as a conventional fuse. When the fusing current is applied, the metal separates and draws back, leaving a large

enough gap in the metallization to ensure that the electrical open circuit thus created will be maintained throughout the life of the circuit.

Under normal operating conditions, the current flow through the memory element is an order of magnitude less than that required for fusing. Thus, to provide the necessary fusing current for a specific element, terminal connections which are different from the normal operating connections must be used. These connections are shown in Figure 2.

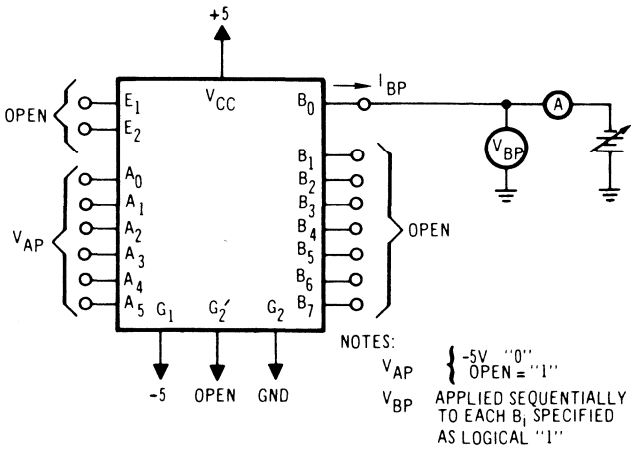


Figure 2

The first item to note regarding the programming terminal arrangement is that terminal G_1 – normally returned to ground – is connected to -5 volts for programming. Also, the logic levels at the address terminals are -5 volts for logical "0" and an open circuit for logical "1." Terminals E_1 and E_2 are also open-circuited (logical "one") for programming.

The eight output terminals B_0 through B_7, correspond to the eight bits of the output word and they are addressed in the normal fashion – other than the redefined logic levels – to select a particular word for programming. When a word is selected, the application of the programming voltage (V_{BP}) to a specific output terminal corresponds to writing a "one" into that specific memory cell. When that same word is then addressed in normal operation, only the programmed bits of the output word will be logical "ones"; all other bits of that word will remain logical "zeros".

The manner in which the memory element is programmed is quite straightforward. The selection of a particular input address causes one of the sixty-four decoder AND gates to have all of its inputs – and hence its output – at a high voltage level. This places approximately 3 volts at the base of one of the sixty-four multiple-emitter transistors and causes a relatively small current flow through each of the memory elements connected to the emitters of the selected transistor. The current through one of the elements can be increased significantly by forward biasing the base-collector junction of the output buffer to which it is connected. This is accomplished by placing approximately -5 volts at the collector (output) terminal, and allowing the current flow out of that terminal to increase to approximately 30 mA. When the current reaches this value, there is a sufficient amount of current flowing through the memory element to cause the metal to flow and separate, thus opening the path between the selected word line and the selected output buffer.

With the same logic levels at the address inputs, any of the remaining bits of the output word can be changed to logical "ones" simply by applying the programming current and voltage to those output pins corresponding to the selected bits. Other memory locations can be programmed in a similar fashion by changing the input address and repeating the programming procedure.

The input logical "zero" and input ground are specified as -5 volts to prevent current flow through the memory elements associated with unselected words when the base of the transistor to which they are connected is brought to -4 volts. This not only provides an additional safety margin to prevent these elements from fusing, but also minimizes the current which must be conducted through the base-collector junction of the output transistor. The "one" logic level is specified as an open circuit to prevent breakdown of the input emitter base junction and to minimize programming power dissipation.

Programming in this fashion while observing the ammeter will allow the programmer to actually "see" the element open, as the ammeter will rise to approximately 30 mA as the voltage is increased and then suddenly drop to 15 mA as the element fuses. The current will then continue to increase with voltage due to the inverse beta of the output transistor, which will start to conduct as V_{CE} approaches -5 volts. To prevent damage to this transistor, therefore, it is advisable to limit the power supply current (or the maximum current of any programming device) to 60 mA. This current level will not damage the output transistor and, at the same time, it will guarantee fusing.

Another precaution which should be observed is to limit the application of the programming current to a single output at a time. This is required to limit the current through the multiple-emitter transistor which connects the selected word line to the memory elements. The design of this particular device does not allow it to conduct the programming current for more than one memory element at a time.

The final precaution to be observed during programming is to maintain the case temperature of the PROM™ at or below 75°C. The programming system depicted in Figure 2 may require the use of a heat sink to dissipate the heat generated during programming. An alternate system can be used, however, which eliminates the need for heat sinking. This system, shown in Figure 3, applies voltage to the chip only during the time an element is actually being programmed. Thus the average power dissipation — and hence the heat generated — are held at acceptable levels without a heat sink.

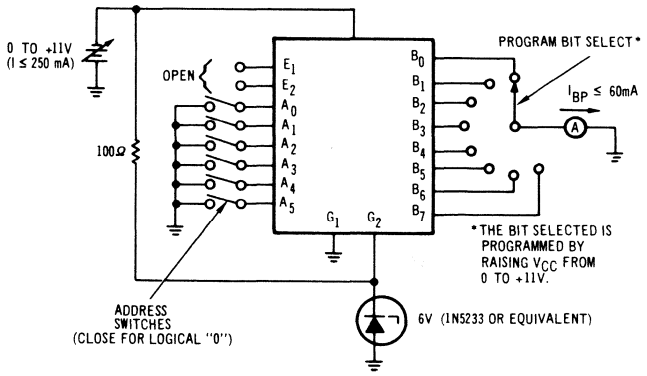


Figure 3

The following chart summarizes these requirements and also provides additional specifications which apply during the programming operation.

SPECIFICATIONS (1)

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{CC} . . . . . 5.5 Volts

Ground (G), Address "0" (V_{AL}) . . . . . -6.0 Volts

Enable Voltage (V_E), G_2', Address "1" (V_{AH}) . . . . . OPEN

Programming Voltage (V_{BP}) . . . . . -7.0 Volts

Programming Current (I_{BP}) . . . . . 60.0 mA

PROGRAMMING CHARACTERISTICS

(Test Conditions: V_{CC} = 5.0V, V_{G1} = -5.0V, T_{CASE} = 75°C)

PARAMETER(2)	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Address Input Current	I_{AL}		2.0	3.0	mA	V_{AL} = -5.0 Volts
Input "Ground" Current	I_{G_1}		120	160	mA	V_A = Open
Output "Ground" Current	I_{G_2}	0	25	40	mA	$0.0 \leq V_{BP} \leq -6.0V$
Power Supply Current	I_{CC}		150	200	mA	V_{BP} = -6.0 Volts
Programming Voltage	V_{BP}	3.0		-6.0	Volts	
Programming Current	I_{BP}	10.0		40.0	mA	

(1) All specifications refer to programming circuit shown in Figure 2.

(2) See Figure 4.

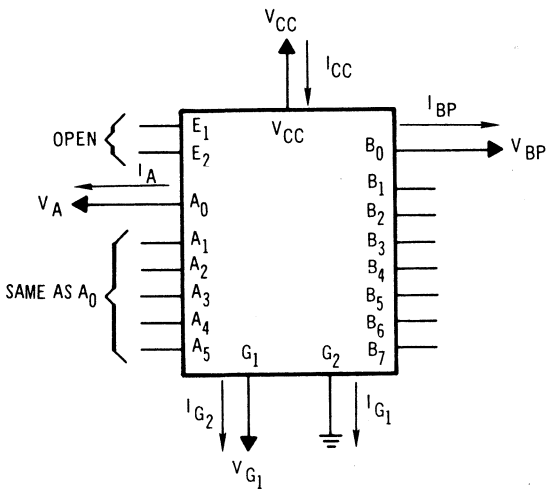


Figure 4

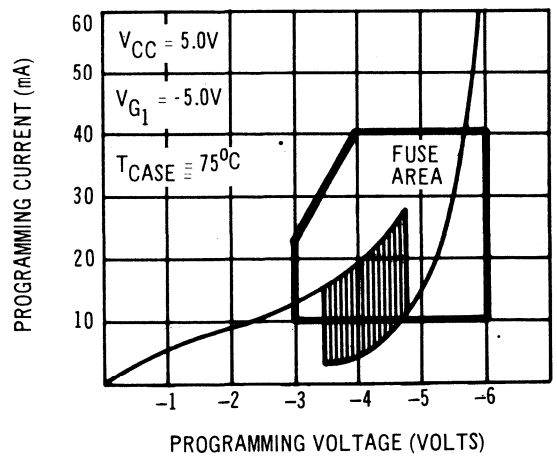


Figure 5

AUTOMATIC PROGRAMMING

While the manual programming systems shown in Figures 2 and 3 are extremely simple and inexpensive, the time required to program a typical PROM™ (~1 hour) when these systems are used is not generally suitable in applications requiring many ROM's of the same pattern. In these situations, a faster, more automated system is often desirable. Such a system is shown in Figure 6.

Addressing in this system is accomplished with a 6 bit counter whose outputs are connected to the address inputs of the PROM™ through level shifters which provide the specified logic levels required for programming.

A shift register, which continuously circulates a single bit, and the program input data determine the particular output bit to be programmed. These are applied to the fusing circuit through a NAND gate whose output goes low — and hence turns on the current generator — when both inputs are logical "ones." Thus, only one output bit at a time is addressed, and the programming of that bit depends on the data at the program inputs.

The shift register is also used to advance the address counter and to signal the external device providing the programming data after the last bit of the current input word has been programmed. A simple test circuit can easily be added to this system by comparing the output of the PROM™ with the program input when the circulating "one" in the shift register reaches the ninth stage. The address and program advance signal would, of course, be inhibited if the comparison indicated that a programming error had occurred.

The programming data can be provided by a variety of devices, including punched cards, paper tape, keyboards, etc. Since the minimum time required to program a specific word is approxi-

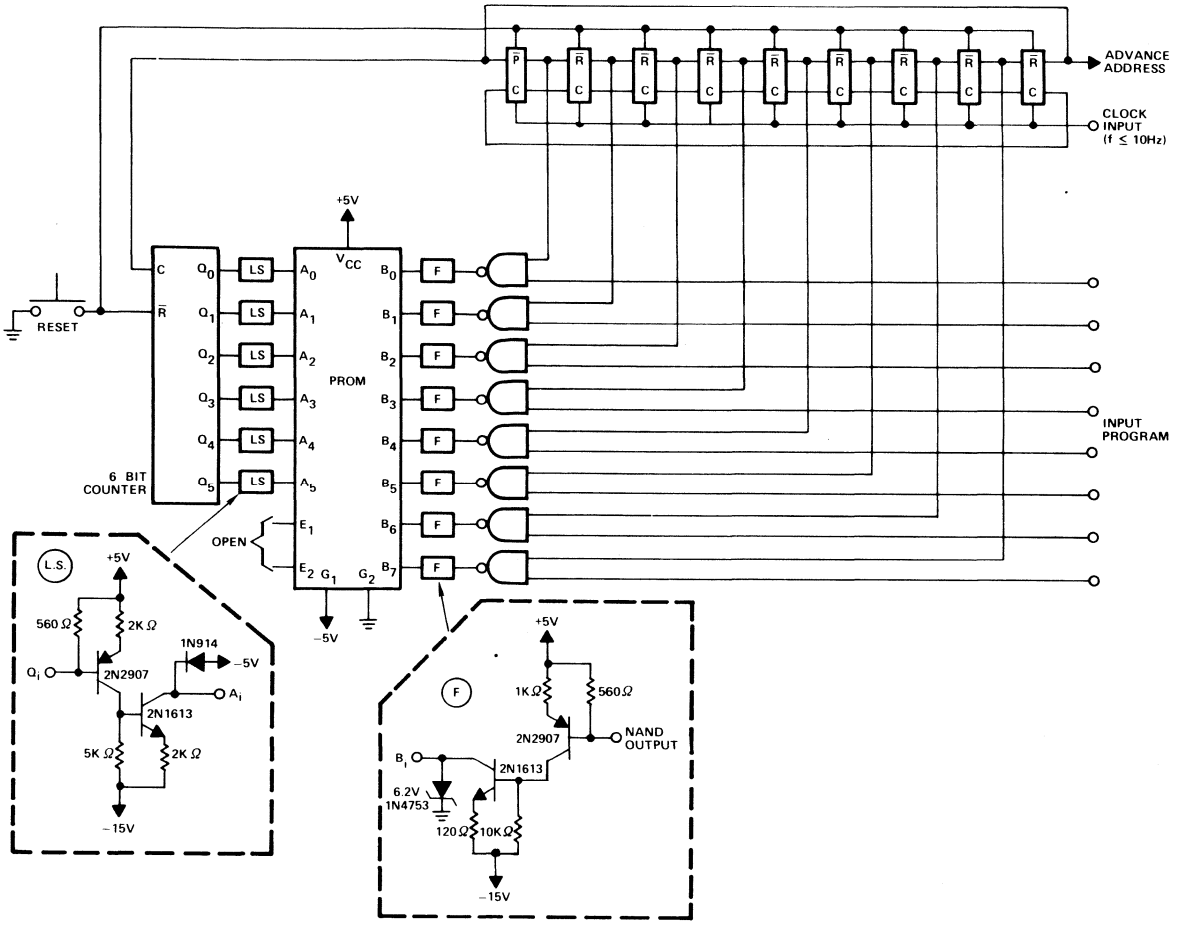


Figure 6

mately one second, any device capable of providing an eight bit word in this time interval can be used. Note, however, that the data for the next word to be programmed should be available at approximately the same time the address counter and shift register switch after the last bit of the previous word has been programmed. Here again, an additional stage on the shift register can be useful, in that an additional 100 ms would be provided during which none of the output pins were being addressed. This time could be used to switch the program input device and the address counter.

Using this system, a PROM™ can be completely programmed in less than a minute, regardless of the nature of the program or the number of "ones" in the program specifications.

CUSTOM PROGRAMMING

If for any reason, the user does not wish to do his own programming, Harris is thoroughly prepared to provide this service using an automatic programming system similar to that shown in Figure 6. This system is designed to program the device, verify the results, and perform all of the other electrical tests which are normally required. Since these latter tests must be performed in any event, the additional time required to program a device does not contribute a great deal to the overall cost of the product. Due to the additional paperwork and handling, however, a nominal fee is charged to custom-program small unit quantities.

The program specification can be transmitted to Harris in a number of ways.

One method requires the completion of the truth table shown in Figure 7. Punched cards are then prepared according to the information contained in the truth table, and these cards are used to operate the programming system described above.

PROM™

HPROM-0512

CUSTOM-PROGRAMMED SPECIFICATION FORM

EXAMPLE

WORD NO.	ADDRESS A_5	A_4	A_3	A_2	A_1	A_0	DATA B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	1	0	1	1	0	0	1
1	0	0	0	0	0	0	1	0	0	1	0	1	1	0
2	0	0	0	0	1	0	1	0	1	0	0	1	1	0
⋮				⋮						⋮				
63	1	1	1	1	1	1	0	0		1	0	1	1	0

Please include this form as a part of your purchase order.

NO.	ADDRESS A_5	A_4	A_3	A_2	A_1	A_0	DATA B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0								
1	0	0	0	0	0	1								
2	0	0	0	0	1	0								
3	0	0	0	0	1	1								
4	0	0	0	1	0	0								
5	0	0	0	1	0	1								
6	0	0	0	1	1	0								
7	0	0	0	1	1	1								
8	0	0	1	0	0	0								
9	0	0	1	0	0	1								
10	0	0	1	0	1	0								
11	0	0	1	0	1	1								
12	0	0	1	1	0	0								
13	0	0	1	1	0	1								
14	0	0	1	1	1	0								
15	0	0	1	1	1	1								
16	0	1	0	0	0	0								
17	0	1	0	0	0	1								
18	0	1	0	0	1	0								
19	0	1	0	0	1	1								
20	0	1	0	1	0	0								
21	0	1	0	1	0	1								
22	0	1	0	1	1	0								
23	0	1	0	1	1	1								
24	0	1	1	0	0	0								
25	0	1	1	0	0	1								
26	0	1	1	0	1	0								
27	0	1	1	0	1	1								
28	0	1	1	1	0	0								
29	0	1	1	1	0	1								
30	0	1	1	1	1	0								
31	0	1	1	1	1	1								
32	1	0	0	0	0	0								
33	1	0	0	0	0	1								
34	1	0	0	0	1	0								
35	1	0	0	0	1	1								
36	1	0	0	1	0	0								
37	1	0	0	1	0	1								
38	1	0	0	1	1	0								
39	1	0	0	1	1	1								
40	1	0	1	0	0	0								
41	1	0	1	0	0	1								
42	1	0	1	0	1	0								
43	1	0	1	0	1	1								
44	1	0	1	1	0	0								
45	1	0	1	1	0	1								
46	1	0	1	1	1	0								
47	1	0	1	1	1	1								
48	1	1	0	0	0	0								
49	1	1	0	0	0	1								
50	1	1	0	0	1	0								
51	1	1	0	0	1	1								
52	1	1	0	1	0	0								
53	1	1	0	1	0	1								
54	1	1	0	1	1	0								
55	1	1	0	1	1	1								
56	1	1	1	0	0	0								
57	1	1	1	0	0	1								
58	1	1	1	0	1	0								
59	1	1	1	0	1	1								
60	1	1	1	1	0	0								
61	1	1	1	1	0	1								
62	1	1	1	1	1	0								
63	1	1	1	1	1	1								

CUSTOMER

CUSTOMER DRAWING NO.

OTHER INFORMATION

HARRIS SEMICONDUCTOR DRAWING NO.

MARKING INSTRUCTIONS

PACKAGE:
24 LEAD FLAT PACK /24 LEAD DUAL IN-LINE

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS INTERTYPE CORPORATION
P O BOX 883 · MELBOURNE FLORIDA 32901

Figure 7

Another way to specify the program is by using the punched card format shown in Figure 8. This card can also be used to generate the punched cards required to operate the programming system. With either format, care should be taken to assure that the information is correct, neat, and legible.

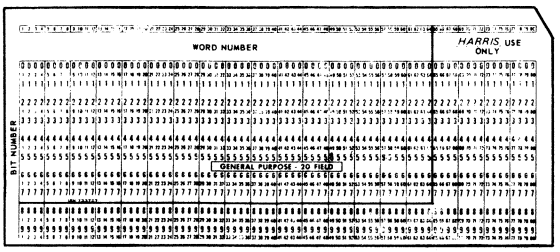


Figure 8

SUMMARY

As shown in the previous sections of this application note, the procedure for programming the HPROM-0512 is extremely simple and easy to accomplish using skills and equipment readily available to the typical systems manufacturer. The programming operation is also very reliable if the specifications outlined in this application note are adhered to in the programming system used.

Thus, the HPROM-0512 can be used in any ROM application without regard to quantity and without waiting the usual four to eight weeks to obtain a particular design. It is felt that the advantages provided by the PROM™ can make a significant difference in the number and variety of applications in which semiconductor ROM's can be economically employed.

HARRIS SEMICONDUCTOR

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APPLICATION NOTE 203

PROGRAMMING THE HPROM-0512 IN AN EXPANDED CONFIGURATION

BY J. P. SHEEHY

INTRODUCTION

It is often desirable to program an expanded, multi-package, read-only memory (ROM) after the individual circuits have been assembled on a printed circuit board. This is a relatively straightforward procedure for memories expanded in the output bit dimension, but programming memories expanded in the word dimension is somewhat complicated by the direct connection (WIRE-OR) of output pins and the leakage currents associated with the outputs of unselected circuits. A procedure which facilitates the programming of circuits assembled in this fashion is given below. Before discussing multi-package programming, however, the PROM™* concept and the normal programming procedure will be reviewed briefly.

PROGRAMMING CONCEPT

The memory elements in the HPROM-0512 are nichrome links that can be opened electronically by supplying enough current through the link to separate the metal in a manner similar to that of a conventional fuse. The 512 memory elements, decoder, and output buffer are all supplied on a single, monolithic, integrated circuit chip. The device is fully packaged and shipped with all memory elements in the conduction state, thus supplying logical "0's" on each of the eight outputs for any input word. Programming, therefore implies the writing of logical "1's" into selected bit positions for any given input word. Furthermore, programming is irreversible, which makes the HPROM-0512 a truly non-volatile, permanent storage device.

NORMAL PROGRAMMING PROCEDURE

The HPROM-0512 (PROM™) has three ground connections (G_1, G_2 and G_2'; pins 11, 13, 23 respectively) that are all connected to system ground under normal operating conditions. During programming, however, the address ground (G_1) is brought to −5.0V as is the logical "0" address input. One of the output grounds (G_2) is kept at 0V while the other, G_2', is left open, and the logical "1" address also open circuited (see Figure 1). With the desired address selected, the memory elements are programmed by applying a negative 6.0V to the appropriate output pins. This forward-biases the base-collector junction of the output buffer and causes a significant increase in current through the memory element corresponding to that bit of the selected input word.

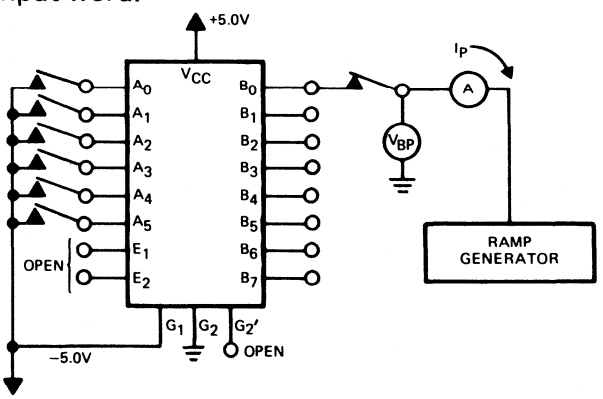

Figure 1. Programming Connections

The output transistor, in the programming mode, is in an inverse condition; that is, the emitter-base junction is reverse biased and the collector-base junction is forward-biased. Due to transistor geometry and the resistivity of the base diffusion, the breakdown voltage of the emitter-base is approximately 5.5V. Therefore, any programming voltage above 5.5V draws additional current from the emitter and G_2 that does not flow through the memory element, and therefore does not help in programming (Figure 2). This is an important consideration in multi-package programming.

***PROM is a trademark of Harris Semiconductor for its family of field programmable read-only memories.**

APP. NOTES

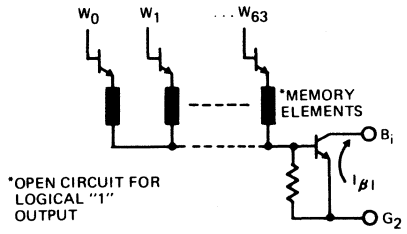

Figure 2.

Another consideration is the fact that the input circuit (see Figure 3) has twice the normal voltage across it in the programming mode, and thus a logical "0" input will draw twice the normal TTL input low current or roughly 3mA. The logical "1" condition is specified as an open circuit to prevent emitter-base breakdown of the input TTL device and to minimize power dissipation.

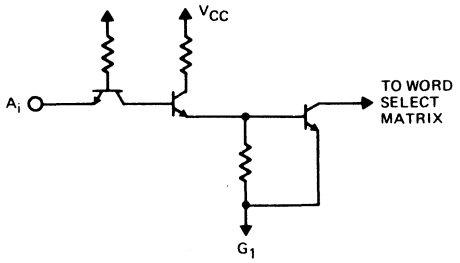

Figure 3.

EXPANDED BIT PROGRAMMING

Expanding the number of output bits for a given word is accomplished by hardwiring the corresponding inputs of more than one device and keeping the output bits separated. Programming in this configuration is accomplished by addressing the appropriate word and applying the programming voltage to each successive output pin specified as a logical "1". The only difference between bit-expanded programming and single-unit programming is the higher "0" level fan-out required for the address input circuit which must sink twice the normal current for each PROM,™ multiplied by the total number of PROM's connected in parallel.

EXPANDED WORD PROGRAMMING

Expanding the number of words in a system is usually accomplished by the direct connection (WIRE-OR) of the corresponding output bits of two or more PROM's. With "WIRE-OR" outputs, one must have the ability to program one device yet inhibit the others, even though all output pins see the same programming voltage. Inhibiting a device which is not to be programmed is accomplished by bringing the ENABLE input (Pin 6 or 7) to logical "0" (−5.0V) as shown in Figure 5. (With the switches as shown in Figure 5, device 1 will program while device 2 through N will not, even though all outputs are brought to the programming level.)

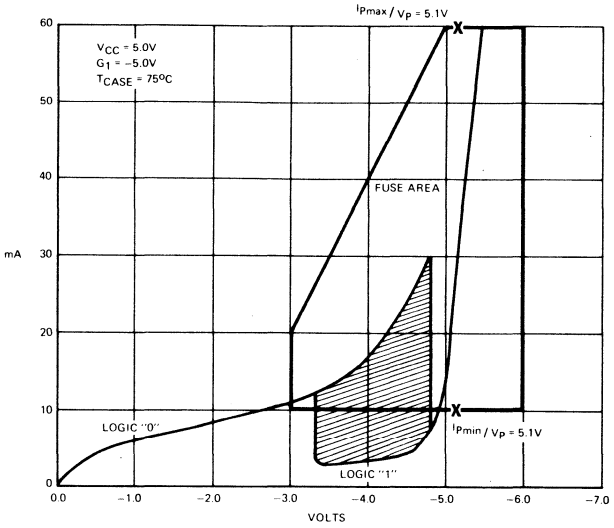

Figure 4. Typical Programming Current vs. Programming Voltage

Figure 4 shows V_P versus I_P for an enabled device. Comparing this with Figure 6, it is clear that reverse-biased, emitter leakage current and inverse current occur in a disabled device. The fusing circuit, therefore, must be capable of sinking both the fusing current of the enabled device and the additional current supplied by (N−1) disabled devices. For a fusing circuit limited to a specific programming voltage (V_P) this current can be determined by adding the maximum programming current (I_{Pmax}) to the maximum disabled circuits (see Figure 5).

Thus: **(1)**

$$I_{Fmax} = I_{Pmax} + (N-1)\, I_{Cmax}\Big|_{V_P = V_Z}$$

Where:

I_{Cmax} = maximum disabled current at $V_P = V_Z$ (from Figure 6).

I_{Pmax} = maximum programming current at $V_P = V_Z$ (from Figure 4).

V_Z = Zener diode clamp voltage.

The current sinking capability of the fusing circuit is set by R_1 and the Zener clamp as shown below:

$$I_F = \frac{15 - V_{SAT} - V_Z}{R_1} \qquad \textbf{(2)}$$

After selecting V_Z, the value of R_1 can be calculated to provide the maximum current (I_{Fmax}) established by Equation (1).

The Zener shown from the collector of Q_1 to ground is used to clamp the programming voltage to a specific level and the value selected should be large enough to guarantee

programming and yet small enough to minimize the leakage from unselected circuits. Figures 4 and 6 show a suitable value for V_Z to be 5.1V.

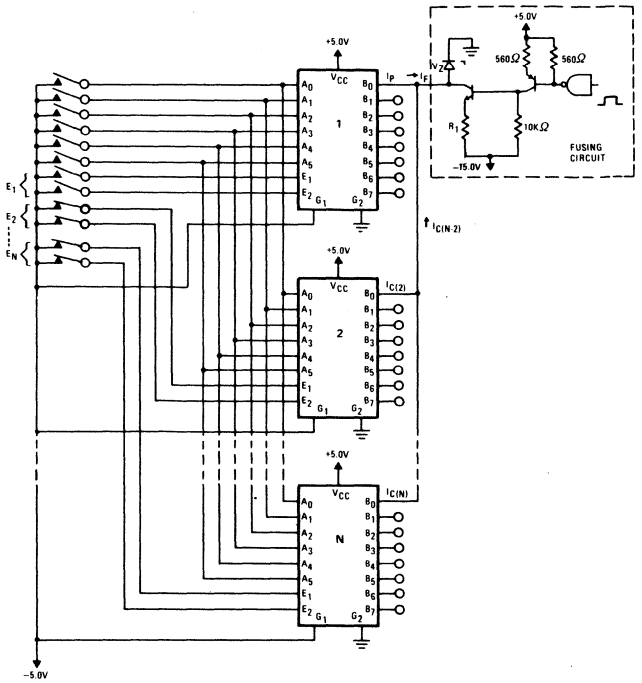

Figure 5. Multi-package Programming

The maximum Zener current (I_{Zmax}) is the difference between I_{Fmax} and I_{Fmin}, where I_{Fmin} is calculated as shown in Equation (1) using the minimum values of programming current (I_{Pmin}) and disabled current (I_{Cmin}) given in Figures 4 and 6. I_{Zmax} is used to calculate the power dissipation in the Zener diode.

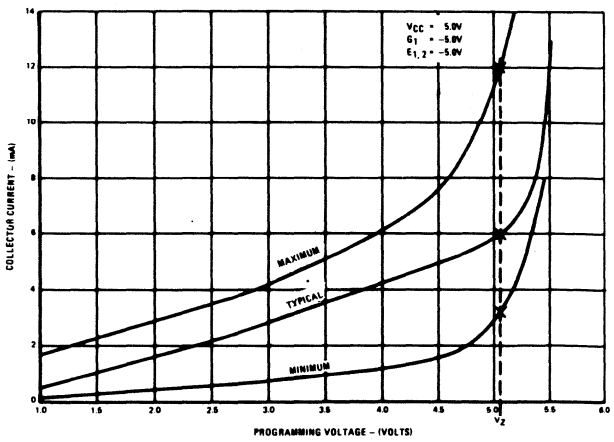

Figure 6. Collector Current vs. Programming Voltage for a Disabled Device

SAMPLE CALCULATION

To find R_1 and the Zener power dissipation for programming a 256 word system (4 circuits with outputs "WIRE-ORed"), assume a clamp voltage (V_Z) of 5.1V, and calculate I_{Fmax} as follows:

1. Find the maximum current contribution from the 4 circuits.

$$I_{Fmax} = I_{Pmax} + (N-1)\, I_{Cmax} \Big|_{V_P = 5.1V}$$

Where:
I_{Cmax} = 12mA (Figure 6)

I_{Pmax} = 60mA (Figure 4)

Thus:
$I_{Fmax} = 60 + 3 \times 12 = 96mA$

2. Determine the value of R_1 to sink I_{Fmax}.

$$I_F = \frac{15 - V_{SAT} - V_Z}{R_1}$$

Let I_F = 96mA; V_Z = 5.1V

$$R_1 = \frac{15 - 0.3 - 5.1}{.096}$$

R_1 = 100 Ohms

3. Calculate the power requirements of the Zener diode.

$$I_{Fmin} = I_{Pmin} + (N-1)\, I_{Cmin} \Big|_{V_P = 5.1V}$$

Where:
I_{Pmin} = 10mA* (Figure 4)

I_{Cmin} = 3mA (Figure 6)

$I_{Fmin} = 10 + 3 \times 3 = 19mA$

$I_{Zmax} = I_{Fmax} - I_{Fmin}$

$I_{Zmax} = 96 - 19 = 77mA$

Therefore:

$P_Z = V_Z I_Z = 5.1 \times 77 = 390mW$
(A 1N751 for the Zener diode would suffice)

Due to the lower voltage restriction on V_P (i.e. 5.1V) an increase in programming time is sometimes required when programming devices in a multi-package, expanded word configuration. Whereas a single device will

* After Programming

typically program in less than 200ms with $V_P \approx 6.0V$, it may require approximately 2.0 sec.with the programming voltage reduced to 5.1V. There is no problem with applying the programming voltage for a longer period of time as long as the maximum programming case temperature (+75°C) is not exceeded.

PROGRAMMING THE PROM™ IN A SYSTEM

Programming expanded ROM's in a logic system with typical TTL input levels is illustrated in Figure 7. This fusing technique differs from that discussed above in that the operating levels of the device are shifted positive by 5.0V (i.e. V_{CC} = 10.0V, G_2 = 5.0V, G_2' open, G_1, Logic "0" = 0V). The negative supply on the fusing circuit is also increased by 5.0V so that the V_{CEO} rating of the NPN programming transistor is not exceeded.

The devices are addressed with open collector gates, which have the current capacity necessary to fan-out to four (4) PROM™ inputs operating in the programming mode.

CONCLUSION

Programming the PROM™ in an expanded configuration can be easily accomplished by providing an adequate means of handling the additional current requirements of both the address input circuits and the fusing circuit. One must also have access to the input ground (G_1), and the output ground G_2' to establish the programming configuration; and the ENABLE inputs of all "WIRE-ORed" circuits to select the proper word for programming.

The following important points should be kept in mind during multi-package programming:

1. Address low current is two TTL loads. Logic low level is equal to G_1.
2. Address high level is an open circuit or a "turned-off" open collector transistor.
3. $T_{CASE} \leq +75°C$ in the programming mode.
4. Programming time is approximately 500ms at V_P = 6.0V.

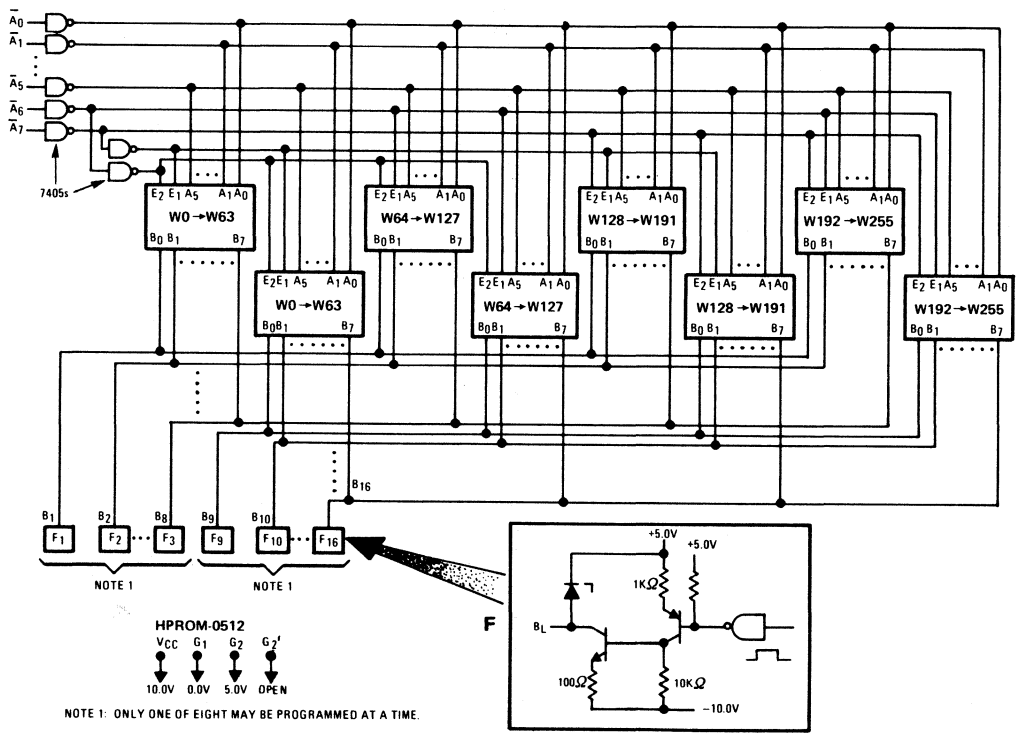

Figure 7. HPROM-0512 System Programming

HARRIS SEMICONDUCTOR

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APPLICATION NOTE 206

MONOLITHIC DIODE MATRICES

INTRODUCTION

The information presented in this application note is intended to serve as an aid to systems designers involved in the general field of electronic data processing.

Harris' monolithic diode matrices offer the designer a powerful and versatile tool to solve some of today's complex data processing problems. These matrices are ideally suited for the generation of complex logic functions as well as for encode/decode and fixed memory applications. Illustrative examples of such applications are included in this booklet.

A variety of matrix sizes are offered. Each matrix makes use of Harris' unique fusible link design which permits selective removal of diodes, thus providing the necessary flexibility in meeting any code pattern design requirement.

Combining the fusing technique with the availability of various matrix sizes and the possibility of assembling several matrices to form larger arrays, provide designers with the necessary flexibility in systems design.

MONOLITHIC DIODE MATRICES

Harris' Dielectric Isolation and epitaxial technology play important roles in fabricating monolithic diode matrices. Incorporation of a unique fuse link pattern used to connect each diode in the array provides the necessary flexibility to form any desired custom code pattern. These features combine to yield high performance matrices with flexibility for maximum system utilization.

With the Dielectric Isolation process, Harris practically eliminates parasitic coupling by forming rows of diodes in dielectrically isolated moats. The monolithic structure is shown in Figure 1. A low resistance epitaxial "bathtub layer" forms the common cathode connection for the row diodes. Use of low resistance epitaxial layers keep row resistances to a minimum, making large matrices feasible to produce in monolithic form.

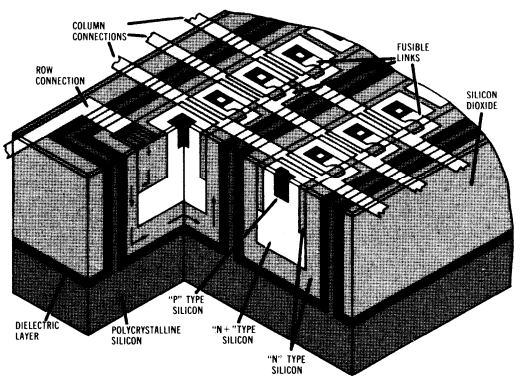


Figure 1

Column connections to the anode side of the diodes are made to metalized interconnect lines via fusible links. A detailed outline of the fusible link pattern is shown in Figure 2. The fuse links are so designed that within the specified maximum operating current limits of the matrix they can perform the normal interconnect function. The fuse links are selectively opened to provide custom patterns. Application of a short current pulse opens the link part of the metalized interconnect pattern, and effectively disconnects the selected diode from the matrix. An open fuse link is also shown in Figure 2. Control of fuse dimensions during manufacture assures

reliable fusing with no detriment to other parts of the matrix.

The matrix is electrically isolated from the package by virtue of the dielectric layer and the supporting polycrystalline substrate.

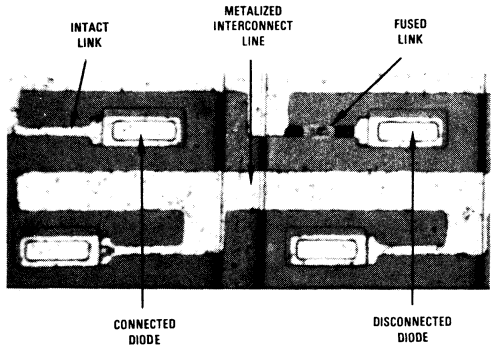


Figure 2

FUSING PRINCIPLE

The principle of the matrix fuse link is the same as a conventional electric fuse. A fuse is placed in series with an electrical element such that an overload will blow the fuse and open the circuit. This is the normal protection mode of a fuse. This protection mode can also be considered and used as an irreversible switching function; once blown, the fuse provides an open circuit.

When a fuse is placed at each junction of a matrix, a potential switching matrix is formed. By opening the interconnecting fuse links, custom code patterns are formed. The magnitude of the fusing current is specified to be well above maximum matrix current and voltage limits. The fusing current is determined by the fuse link design and its value is maintained by dimensional control in production.

FUSING CIRCUIT

A simple capacitor-transistor ramp generator is used to provide the fusing current. A custom matrix pattern is formed in a manual fusing fixture as shown in Figure 3. The diode to be eliminated is selected by setting the row and column switches S2 and S3 respectively as required. When switch $S1_A$ is in the position shown, the base of the transistor is grounded and no emitter voltage is present. Moving the switch to position 2 starts the fusing process. The base voltage of Q1 rises exponentially at a rate determined by R and C. The emitter voltage follows the base voltage, impressing this voltage across the diode and fuse. As the voltage increases the power dissipated in the fuse causes a temperature rise. As the temperature of the fuse is raised, the aluminum begins to melt. This melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum at approximately 650°C will not affect the passivating layer of silicon dioxide whose melting temperature is about 1350°C. Test verification is obtained by an indicating device placed in series with the column and row switches through the contacts $S1_B$ to give visual indication to the condition of each diode in the matrix before and after fusing.

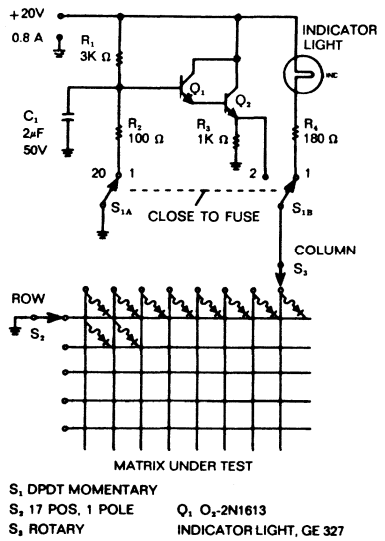
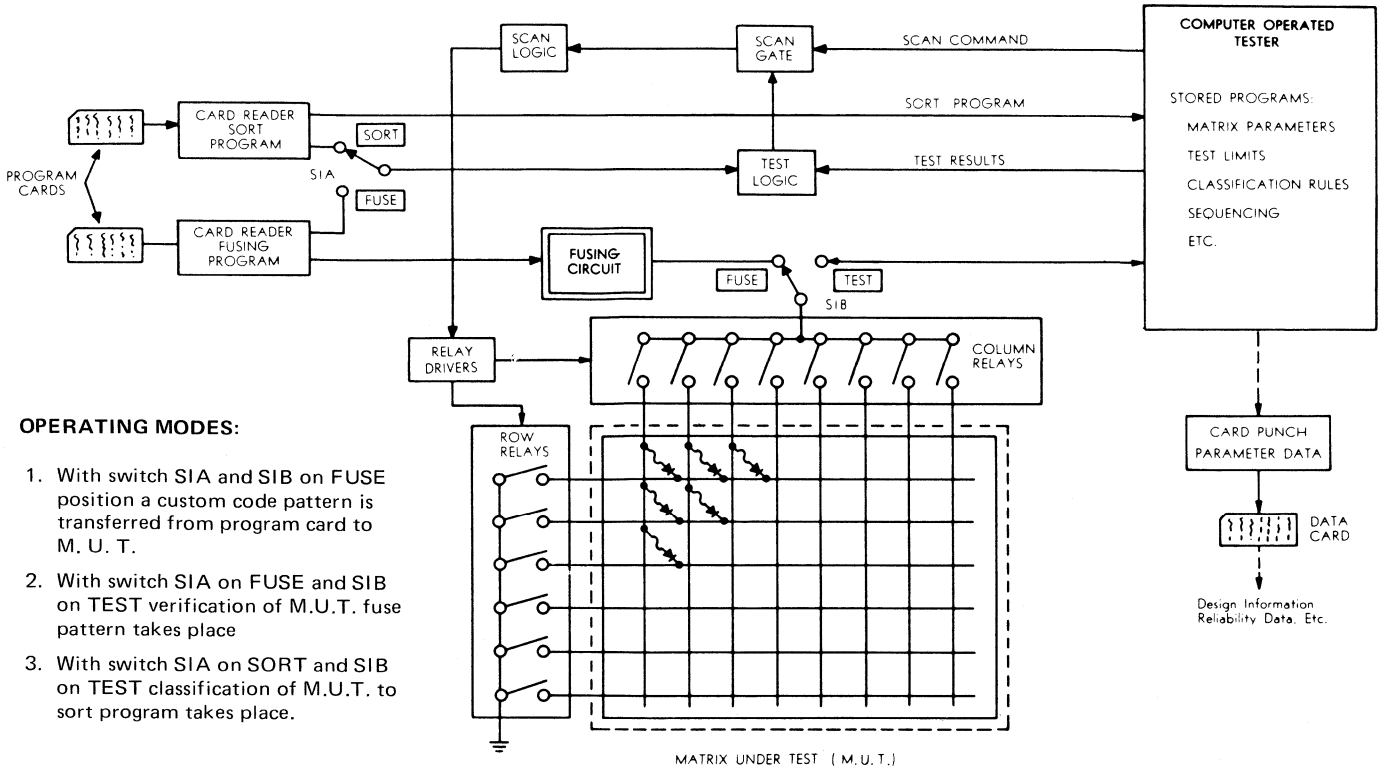


Figure 3

SEMIAUTOMATIC TEST SYSTEM

In order to handle large numbers of custom patterns, Harris has designed and built a high speed programmable matrix fusing test system. This system employs the same basic fusing technique used in the manual tester. In addition, the system has incorporated the features of matrix sorting, verification of diode parameters, and verification of fused patterns, to enable it to be used as a general purpose production tester. This allows rapid product classification and matrix customizing to be performed for the number of patterns and matrix quantities involved in mass production.

When a requirement is established for a particular matrix size and custom pattern, the following events occur. A program card is prepared to reflect the proper matrix size and diode pattern desired. This card is placed in a card reader and the test system is now operated in the fusing mode. Information



OPERATING MODES:

1. With switch SIA and SIB on FUSE position a custom code pattern is transferred from program card to M. U. T.
2. With switch SIA on FUSE and SIB on TEST verification of M.U.T. fuse pattern takes place
3. With switch SIA on SORT and SIB on TEST classification of M.U.T. to sort program takes place.

Figure 4

from the card is transferred to the row and column scan logic used to control the selective fusing process for the generation of a given custom pattern. The tester then automatically transfers to a final verification mode and makes a one-to-one check against the program data cards. The operations performed have been the selection of a matrix from production inventory to the customer's electrical requirements, fusing the customer's desired pattern and verification of the fusing operation. These operations are performed exceedingly fast, allowing the test system to customize matrices at a rate of 2100 diodes per hour. A simplified block diagram of the tester is shown in Figure 4.

MATRIX CONFIGURATION

Typical matrix configuration are shown in Figure 5. All matrices contain diodes with rows of common cathode connections and columns of common anode connections. The first number in the matrix title is the row identification and the second identifies the column. As an example, 5 x 8 signifies five rows and eight columns. Table 1, page 6, gives a complete list of the presently available matrix configurations.

Combining the fusing technique with the availability of various matrix sizes and the possibility of assembling several matrices to form larger arrays, provides designers with the necessary flexibility in systems design.

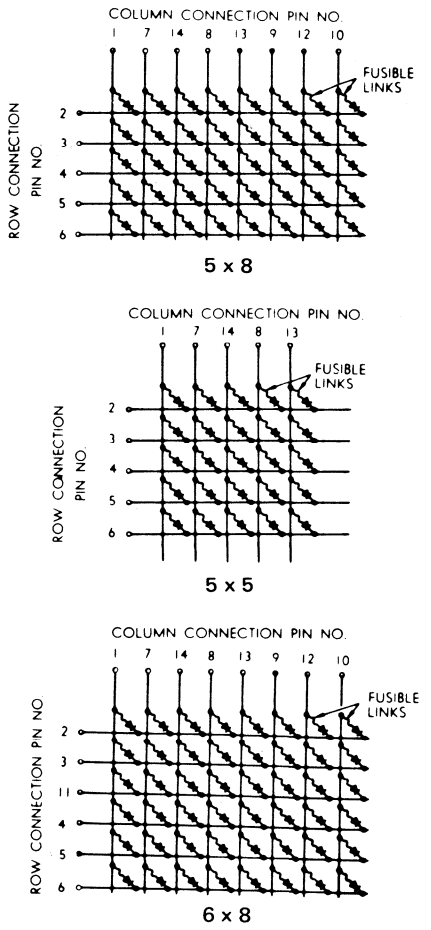


Figure 5

LOGIC GATES

A typical diode matrix of AND gates is shown in Figure 6A and is redrawn in circuit notation in Figure 6B. Positive logic is used where the definition of a logic "1" represents a positive voltage and a logic "0" represents zero or negative voltage. Figure 6B allows for easy interpretation of the matrix function being generated.

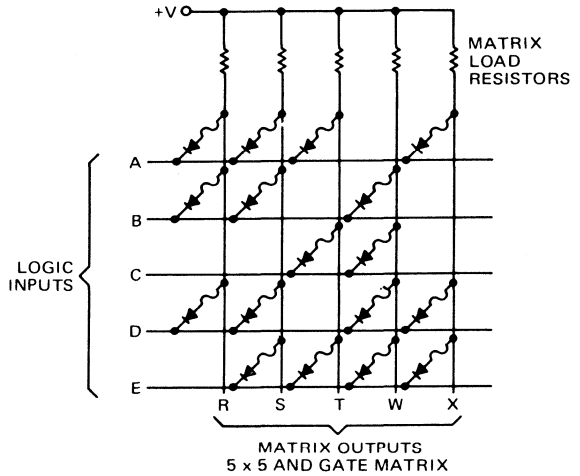


Figure 6A

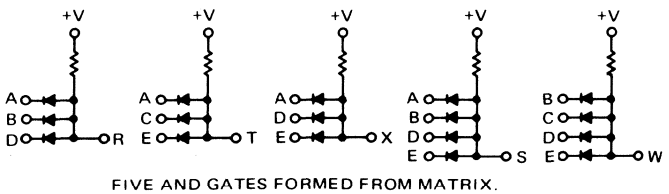


Figure 6B

Figure 7A shows a matrix of OR gates and 7B the equivalent circuit representation. The same matrix pattern is used in both figures 6 and 7.

The AND-OR gate function can be performed in an individual matrix array or in separate packages as desired.

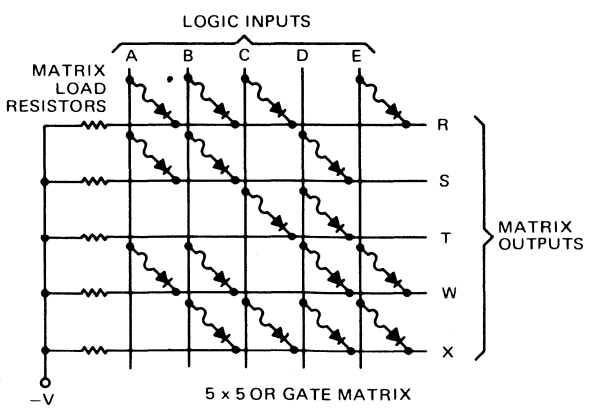


Figure 7A

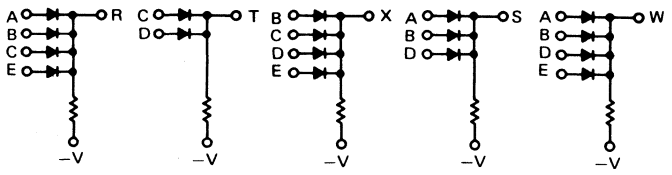


Figure 7B

Figure 8A is a matrix where both AND and OR gates are formed simultaneously. The matrix circuit is a two-level AND-OR gate array where the circuit notation, logic notation and logic equations are shown in Figures 8B, C, and D. The term A·B·D is formed twice to show the extended fanout capability of the matrix.

When negative logic is used, where the definition of a logic "1" is either ground or a negative voltage and a logic "0" is a positive voltage, the AND-OR gate definitions of Figures 6, 7, and 8 are reversed.

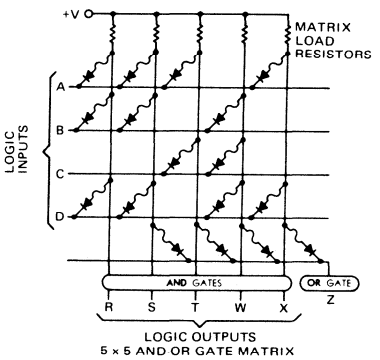


Figure 8A

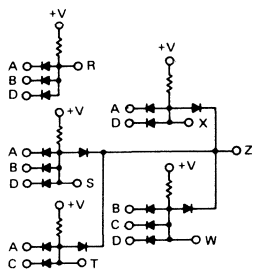


Figure 8B

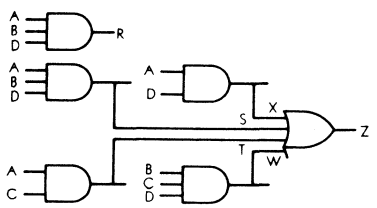


Figure 8C

Logic Equations:

R = A·B·D
S = A·B·D
T = A·C
W = B·C·D
X = A·D
Z = X + S + T + W

MATRIX LOADING

The drive requirements for dielectrically isolated diode matrices are usually less than those employed in discrete diode matrices. The small physical size and uniformity of the monolithic diode matrix reduce matrix capacity, forward voltage variation, and recovery current requirements. In most logic applications, integrated circuits will be employed to drive the matrix. The discussion here will center around integrated circuit and transistor drive requirements. Drive sources such as

APP. NOTES

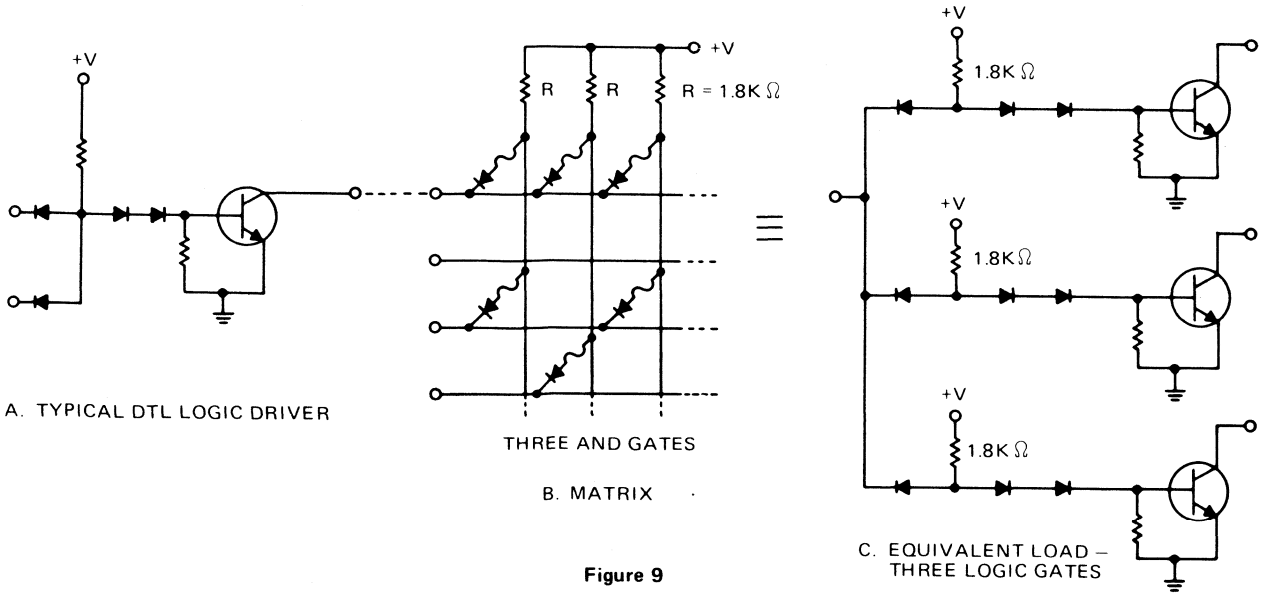


Figure 9

relays, switches, voltage sources, etc., can also be employed as long as maximum parameter limits are not exceeded.

The input drive requirement of a matrix is dependent on the value of the matrix load resistors. The matrix structure is such that the matrix output load requirements usually are reflected as load to the input drivers. The matrix load resistors are selected to provide the necessary output drive for each logic gate in the matrix. In an all AND gate matrix, the normal drive requirement of a unit logic load is generally required for each AND gate output. A unit logic load is defined as the load of a single logic input term for the compatible logic gates used with the matrix. The input driver will drive this unit logic load for each AND gate input in the same manner as the input to another logic gate. Figure 9 shows a logic gate driving an AND gate matrix and the equivalent logic gate loading.

When driving a matrix, it is important not to exceed the capability of the driver. When the matrix load resistor is selected to be equivalent to a unit logic load, the driver can drive as many AND gate terms as specified by its fan-out. When exclusive logic terms are present in the matrix, the reflected loading to the input drivers is reduced. By careful selection of logic terms, and of their placement in the matrix, input drive can be minimized. Where speed requirements and output driver gain permits, it is feasible to use load resistors much larger than the unit loads of the integrated circuit input gates.

The matrix output can be an AND or an OR function. Each logic gate of the matrix will usually drive only one output terminal. This output can be a compatible logic gate input or some special circuit for driving high level voltage or high current loads. Figure 10A shows an AND gate matrix and a typical output driver with logic notation in Figure 10B. With the output driver shown in Figure 10, the matrix and driver provide the NAND logic function. This combination of logic drivers and a matrix can perform the familiar logic function of NAND/NOR. The logic levels are compatible from input to output.

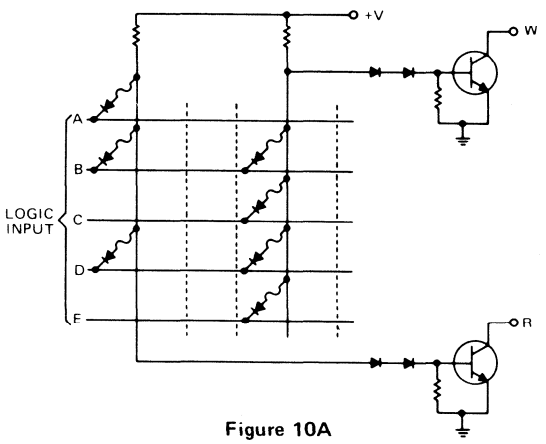


Figure 10A

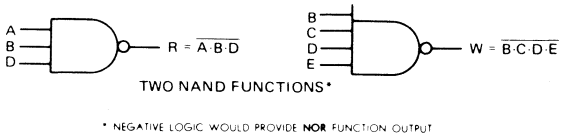


Figure 10B

The NAND function matrix output driver is a special circuit or can be obtained by using the expander input to a logic gate. In Figure 11, the load driver uses the expander input

for the matrix connection, while the additional inputs provide selective control over the matrix function.

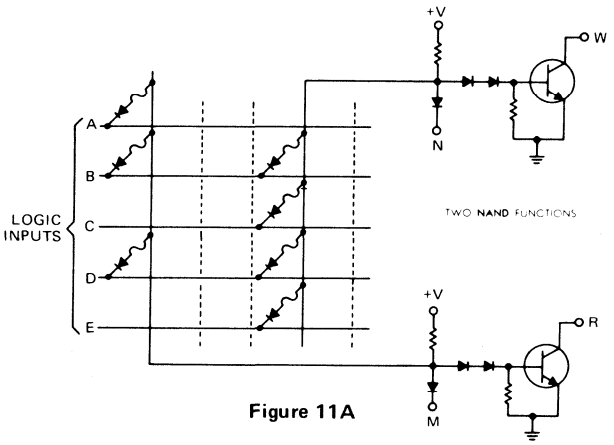


Figure 11A

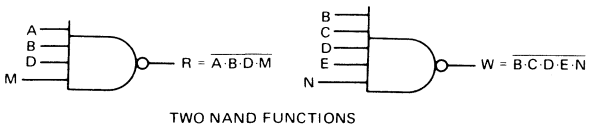


Figure 11B

The fan-out load requirement determines the unit load value of the matrix load resistor. The value of R_M, load resistor of the i^{th} logic gate in the matrix, is determined by the following equation:

$R_M = I_i U_L$ in equivalent unit loads, where:

I_i = number of outputs of the i^{th} AND or OR gate driving a unit load,

U_L = equivalent unit load

In the general matrix case, the input drive requirements can be expressed as L_M, load of the matrix, as a summation of the R_M terms.

$$L_M = \sum_{1}^{K} R_M \text{ in equivalent unit loads, where}$$

K = number of AND or OR gates driven

The capacitance load of the matrix is dependent on the AND or OR gate configuration. The capacity of the matrix diodes is measured and specified with all diodes floating except the one diode under test. The measured value of the capacity is greater than just the diode junction capacity by the accumulation of the rest of the matrix diodes that are reverse biased during test. The capacitance load for the AND gate configuration of Figure 6 is summarized in Figure 12. In most applications, matrix capacity can be neglected since the value of the worst case measured capacity is less than the driver output and stray packaging capacities.

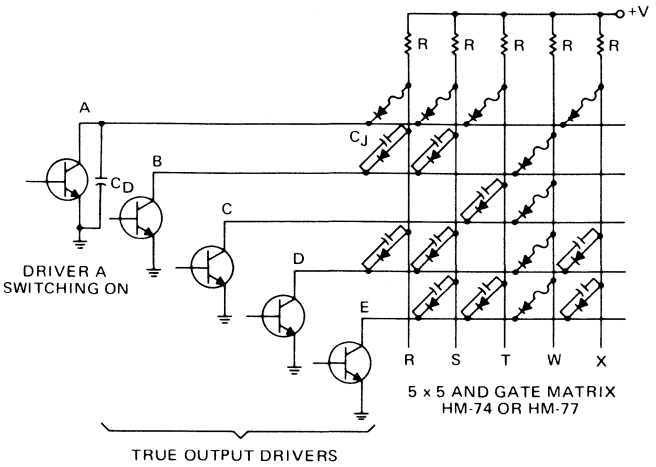
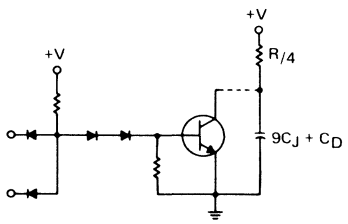


Figure 12A



CAPACITANCE LOAD ON DRIVER A
C_J = JUNCTION CAPACITANCE
$C_D = C_{OB} + C_{STRAY}$ OF DRIVER A

Figure 12B

MATRIX FAMILY - TABLE 1

The present matrix family is listed in Table 1. Larger matrix arrays can be constructed from multiple assemblies of these basic matrices.

-55°C to +125°C TEMPERATURE RANGE

PRODUCT	DESCRIPTION MATRIX CONFIG.	REV. VOLT. BREAKDOWN (MIN.)	REV. REC. TIME (MAX.)
HM1-010-2 HM9-010-2	5 x 8	45V	10ns
HM1-012-2 HM9-012-2	5 x 8	40V	25ns
HM1-013-2 HM9-013-2	5 x 8	35V	50ns
HM1-030-2 HM9-030-2	6 x 8	45V	10ns
HM1-031-2 HM9-031-2	6 x 8	40V	25ns
HM1-034-2 HM9-034-2	6 x 8	35V	50ns
HM1-040-2 HM9-040-2	8 x 6	45V	10ns
HM1-041-2 HM9-041-2	8 x 6	40V	25ns
HM1-044-2 HM9-044-2	8 x 6	35V	50ns

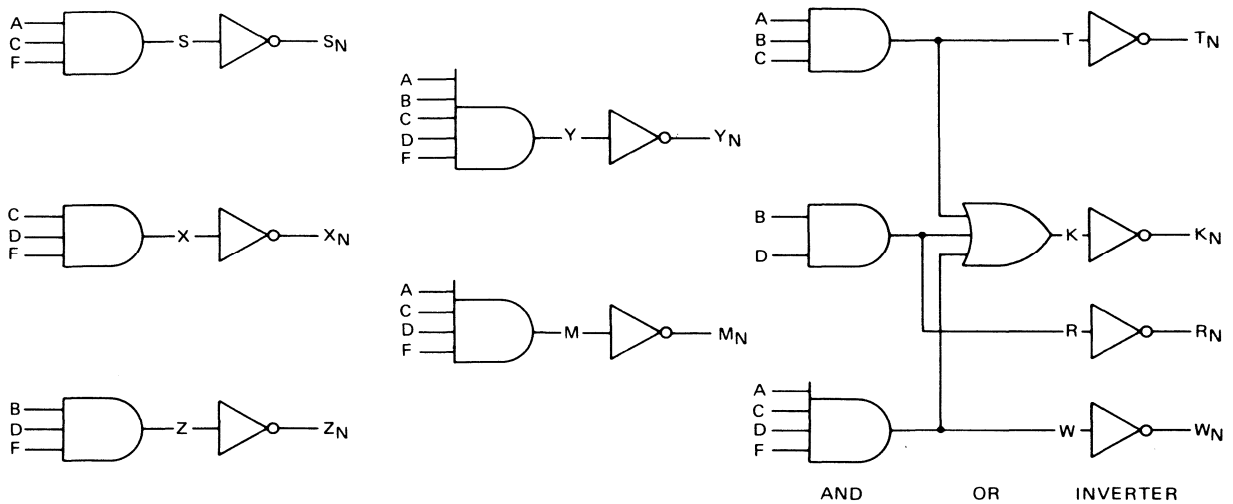
-55°C to +125°C TEMPERATURE RANGE (CON'T)			
PRODUCT	DESCRIPTION MATRIX CONFIG.	REV. VOLT. BREAKDOWN (MIN.)	REV. REC. TIME (MAX.)
HM1-050-2 HM9-050-2	10 x 4	45V	10ns
HM1-051-2 HM9-051-2	10 x 4	40V	25ns
HM1-055-2 HM9-055-2	10 x 4	35V	50ns
HM1-074-2 HM9-074-2	5 x 5	45V	10ns
HM1-075-2 HM9-075-2	5 x 5	40V	25ns
HM1-077-2 HM9-077-2	5 x 5	35V	50ns
HM1-080-2 HM9-080-2	8 x 5	45V	10ns
HM1-081-2 HM9-081-2	8 x 5	40V	25ns
HM1-084-2 HM9-084-2	8 x 5	35V	50ns
HM1-090-2 HM9-090-2	4 x 10	45V	10ns
HM1-091-2 HM9-091-2	4 x 10	40V	25ns
HM1-093-2 HM9-093-2	4 x 10	35V	50ns
0°C to +75°C TEMPERATURE RANGE			
HM1-0104-5	10 x 4	20V	100ns
HM1-0110-5	4 x 10	20V	100ns
HM1-0168-5	6 x 8	20V	100ns
HM1-0186-5	8 x 6	20V	100ns

APPLICATIONS

A brief description is given of a few diode matrix applications. These applications are not claimed to be new or unique. Some applications illustrate and amplify particular features of the matrix approach while others have wide practical value. The variety of matrix sizes, coupled with the fuse link technique, provide an unlimited possibility of custom arrays. This fact makes the matrix approach to logic networks a very powerful design tool. Many more applications for the diode matrix exist than are given here. It is hoped that these particular ones will cover the major fields of interest and will work as a catalyst to stimulate new and better design approaches.

LOGIC FUNCTION MATRIX

The ability to form AND and OR gates in the same matrix provides the feature of two-level diode logic. For instance, an HM-30 6 x 8 matrix generates nine logic functions from five logic variables. The logic function A·C·D·F is generated twice to show the extended fan-out capability inherently built into the matrix approach. The output drive mode used with the matrix can provide either AND/OR or NAND/NOR functions for compatibility with other logic systems.



AND/OR LOGIC
S = A·C·F
Y = A·B·C·D·F
EQUATIONS FOR R, T, W, X, Z & M ARE OF THE SAME FORM
K = T + R + W = A·B·C + B·D + A·C·D·F

NAND/NOR LOGIC
$S_N = \overline{A \cdot C \cdot F}$
$Y_N = \overline{A \cdot B \cdot C \cdot D \cdot F}$
EQUATIONS FOR R_N, T_N, W_N, X_N, Z_N & M_N ARE OF THE SAME FORM
$K_N = \overline{T + R + W} = \overline{A \cdot B \cdot C + B \cdot D + A \cdot C \cdot D \cdot F}$

Figure 13A

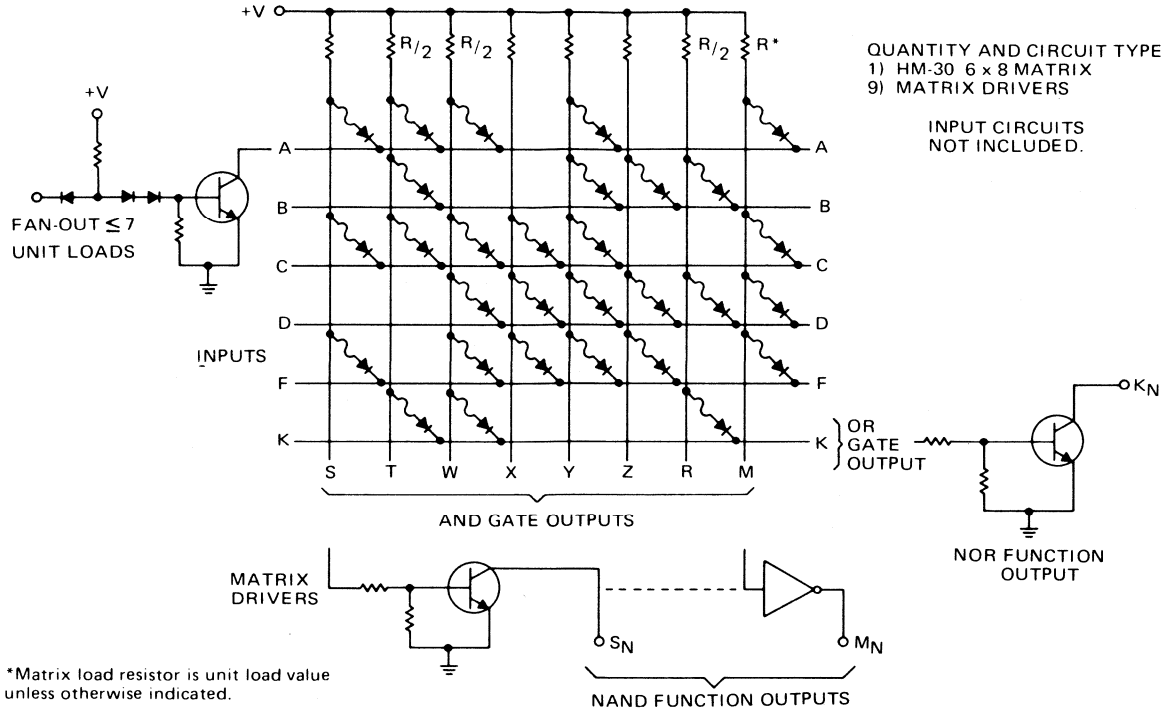


Figure 13B

In Figure 13A the logic diagrams for matrix gates are given for both AND/OR and NAND/NOR logic. The matrix circuit diagram Figure 13B illustrates the custom diode pattern and the drive circuits needed for generation of NAND/NOR functions.

ENCODING MATRIX

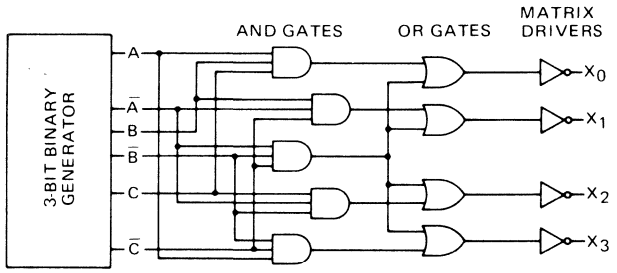


Figure 14A

This matrix is used to encode one binary code into another. In this instance, a three bit binary generator drives an HM-30 6 x 8 diode matrix where the matrix output drivers provide a single zero shift bit. The transfer has been made from a three bit weighted binary to a four bit binary shift code. The output drivers accept two matrix terms to generate the logic NOR. The logic diagram is given in Figure 14A, the truth table in Figure 14B, and the matrix and drive circuits in Figure 14C.

BIT GENERATOR			MATRIX OUTPUT DRIVERS			
A	B	C	X_3	X_2	X_1	X_0
0	0	0	0	0	0	0
1	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
1	1	1	1	1	1	0

Note: Positive Logic True

Figure 14B

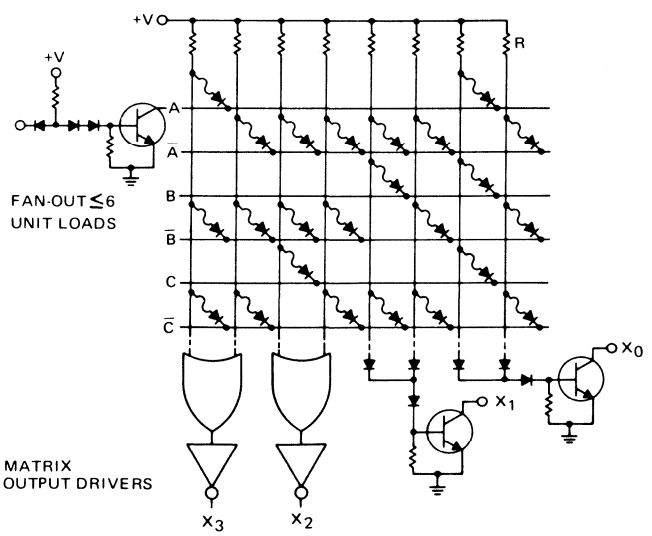


Figure 14C

TELETYPE CODING MATRIX

Large matrices can be formed by assemblies of smaller sizes. In Figure 15, a 5 x 31 matrix is shown, consisting of four HM-10 5 x 8 diode matrices, for the purpose of coding teletype alpha characters into five-bit CCIT2 code. In this application, the matrix is driven through switch contacts from a voltage source. Adequate circuit protection must be used to prevent matrix parameter limits from being exceeded.

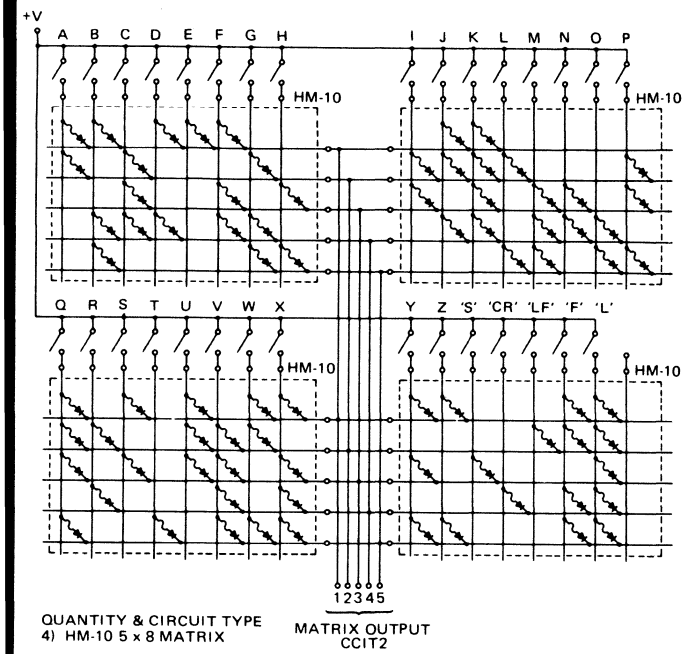


Figure 15

DECIMAL DECODE FOR DISPLAY

A practical example of matrix usage is in a binary coded decimal decode network driving decimal indicators. The monolithic diode matrices can be customized to any weighted binary code to decimal conversion. This design flexibility is provided through the fuse link technique of custom-selecting the desired code pattern. This flexibility is not offered by other integrated decoders, since such BCD decoders are limited to only one weighted binary code.

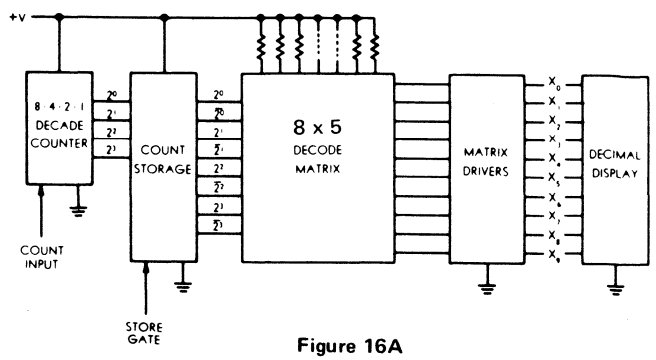


Figure 16A

Figure 16A shows a block diagram and 16B a logic diagram for an 8·4·2·1 binary coded decimal decode matrix. In Figure 16C the matrix circuit diagram and truth table are

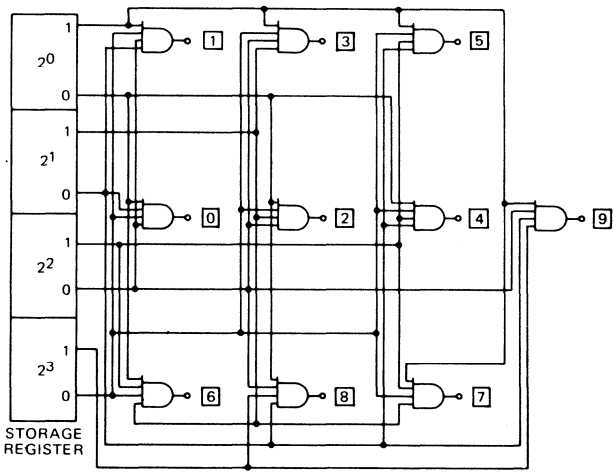
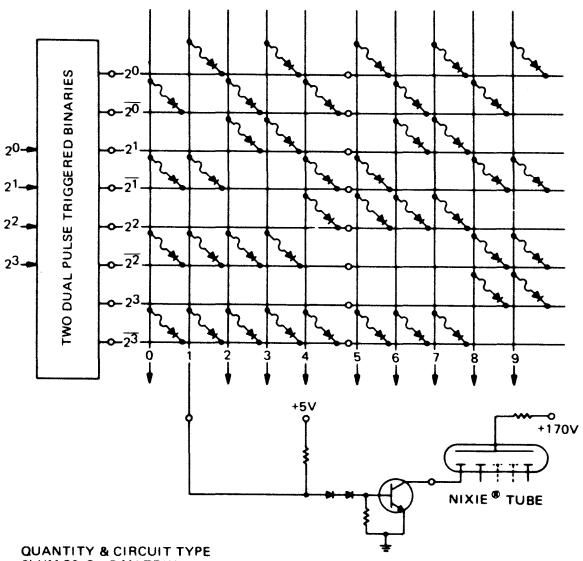


Figure 16B

shown with output drivers for driving gas filled cold cathode indicator tubes. Two HM-80 8 x 5 diode matrices are equivalent to nine logic gate packages needed to perform the same function.



QUANTITY & CIRCUIT TYPE
2) HM-80 8 x 5 MATRIX
1-2/3) HEX INDICATOR DRIVER
Input circuits not included.

2^0	0	1	0	1	0	1	0	1	0	1
2^1	0	0	1	1	0	0	1	1	0	0
2^2	0	0	0	0	1	1	1	1	0	0
2^3	0	0	0	0	0	0	0	0	1	1
DECIMAL OUTPUT	0	1	2	3	4	5	6	7	8	9

Note: 1. Positive logic true
2. Only one output will be on at any time

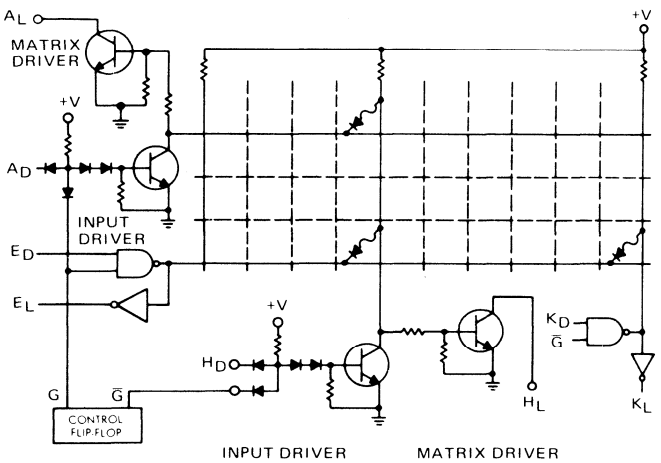
Figure 16C

APP. NOTES

MULTIPLE FUNCTION CODING MATRICES

Information transfer through a matrix is dependent only on the particular custom pattern contained in the matrix. Because of the characteristic of the matrix, the input and output functions can be reversed. As an example, once a matrix has a custom pattern to decode BCD to decimal as in Figure 16C, it can equally well, when properly driven, provide the inverse function of decimal encode to BCD.

In many systems, conversion of codes are done in both directions and a common matrix pattern can be provided independent of the coding direction. It is possible to provide drive circuitry for a single matrix such that by time-sharing the matrix element, it can provide both decoding and encoding functions. A simple 2 x 2 AND function portion of a larger matrix with gate control time-sharing drivers is illustrated in Figure 17. A truth table is given for this multi-function matrix to define the logic states for the control term G inputs. Drivers A_D and E_D control outputs H_L and K_L when the control term input (G) is true. Driver H_D and K_D control outputs A_L and E_L when the control term ($\overline{G}$) is logically true. The truth table for these inputs clearly shows the duality of the matrix.



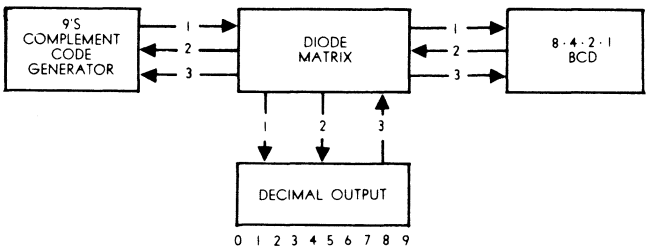
DRIVERS A_D AND E_D							DRIVERS H_D AND K_D							
INPUTS			OUTPUTS				INPUTS			OUTPUTS				
CONTROL TERM	LOGIC TERMS		LOGIC TERMS				CONTROL TERM	LOGIC TERMS		LOGIC TERMS				
G	A_D	E_D	H_L	K_L	A_L	E_L	$\overline{G}$	H_D	K_D	A_L	E_L	H_L	K_L	
1	0	0	0	0	0	0	0	0	0	OUTPUT DETERMINED BY A_D AND E_D				
1	1	0	1	0	1	0	0	0	1					
1	1	1	1	1	1	1	0	1	1					
0	1	1	OUTPUT DETERMINED BY H_D AND K_D				1	1	1	1	1	1	1	
0	0	1					1	1	0	1	0	1	0	
0	0	0					1	0	0	0	0	0	0	

Note: Positive Logic True

Figure 17

NINES COMPLEMENT - BCD

This is an example of a multiple function coding matrix to the decoding of a 9's complement code from a position encoder. Four HM-80 8 x 5 matrices form a unique 16 x 10 decoder-encoder matrix which can provide 8·4·2·1 BCD output for digital recording and, also, simultaneously provide the decimal decode for display. The matrix forms a two-level logic network of AND and OR gates. Since the OR gate function is required, the matrix load resistors vary to satisfy matrix output drive. The four HM-80 custom matrices shown here can provide six code conversions when properly driven.



THREE CODING FUNCTIONS FROM ONE MATRIX [2]

1) 9'S COMPLIMENT TO BCD AND DECIMAL
2) BCD TO 9'S COMPLEMENT AND DECIMAL
3) DECIMAL TO 9'S COMPLEMENT AND BCD

Notes: 1. Arrows Indicate direction of information flow.
2. Proper drive and load circuits are required for each coding function.

Figure 18A

DECIMAL	9'S COMPLEMENT CODE				8·4·2·1 BCD			
	D	C	B	A	X	W	S	R
0	0	1	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	1	1	1	0	0	1	0	1
6	1	0	1	0	0	1	1	0
7	1	0	1	1	0	1	1	1
8	1	0	0	1	1	0	0	0
9	1	1	0	1	1	0	0	1

Note: Positive Logic True

Figure 18B

Figure 18A shows the block diagram with information arrows showing the direction of the six code conversions, and Figure 18B shows the truth table. In Figure 18C the matrix circuit for only the 9's complement to BCD encode and decimal decode is given. The multifunction drive circuits to obtain all six conversions would be similar to that shown in Figure 17. If in a single conversion

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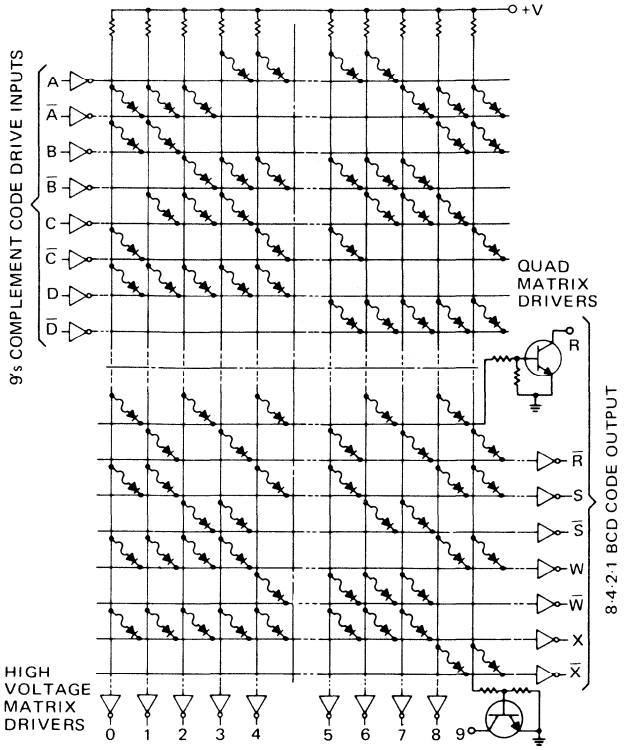
the complements for the BCD are not required, the OR gate complement BCD terms can be eliminated, reducing the matrix input drive requirements.



QUANTITY AND CIRCUIT TYPE
4) HM-80 8 x 5 MATRIX
2½) QUAD H.V. MATRIX DRIVERS
8) MATRIX DRIVERS

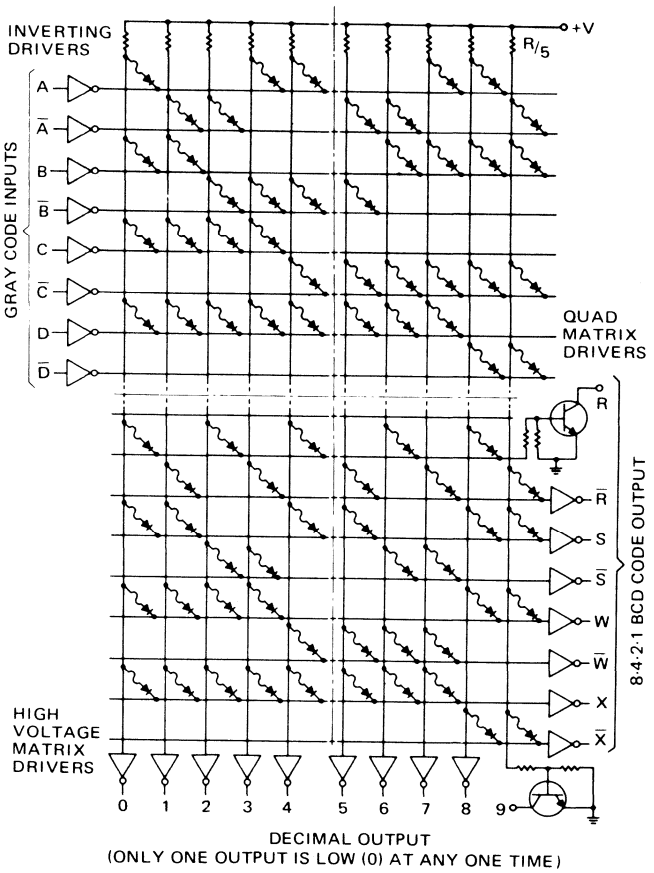
Figure 18C

GRAY CODE - 8•4•2•1 BCD

Another example of a multiple function matrix would be Gray code conversion to 8·4·2·1 and decimal. Figure 19 shows the truth table and the 16 x 10 matrix circuit for only one-direction conversion. The multi-function drive circuits to obtain all six conversions would be similar to that shown in Figure 17.

DECIMAL	GRAY CODE				8·4·2·1 BCD			
	D	C	B	A	X	W	S	R
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1

Figure 19A



QUANTITY AND CIRCUIT TYPE
4) HM-40 8 x 5 MATRIX
2½) QUAD H.V. MATRIX DRIVERS
8) MATRIX DRIVERS

Figure 19B

In Figure 19B, the two lower HM-80 8 x 5 matrices are identical to those used in Figure 18C. This is significant since it shows that with only six custom patterned HM-80 matrices, twelve code conversions can be provided. The same twelve code conversions, using standard NAND/NOR gates, would require many more packages.

FULL ADDER MATRIX

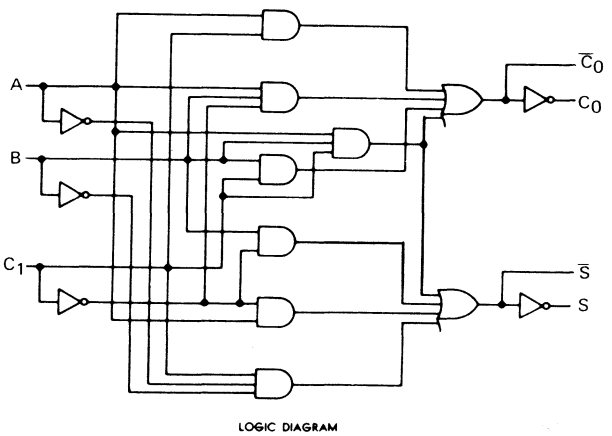
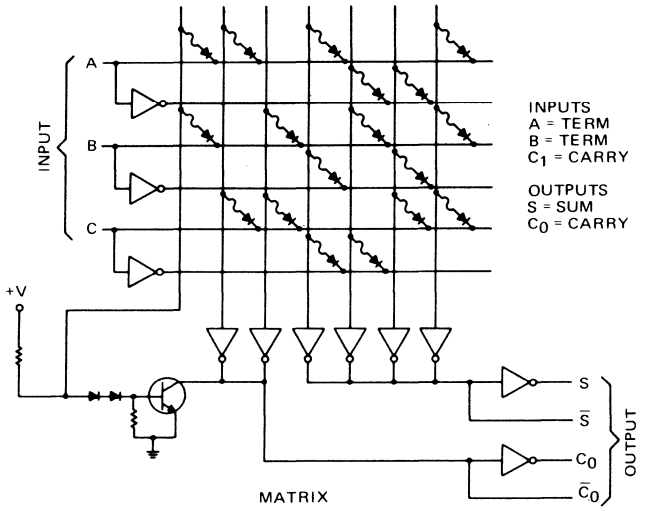


Figure 20A

A binary full adder with complementary Sum and Carry outputs is formed from one HM-30 6 x 8 diode matrix with output drivers.



TRUTH TABLE

A	1	1	0	1	0	0	1	0
B	1	0	1	0	1	0	1	0
C_1	0	1	1	0	0	1	1	0
C_0	1	1	1	0	0	0	1	0
S	0	0	0	1	1	1	1	0

QUANTITY AND CIRCUIT TYPE
1) HM-30 6 x 8 MATRIX
1/3) HEX INVERTER
1 1/6) HEX INTERFACE INVERTEF
INPUT CIRCUITS NOT INCLUDED

Note: Positive Logic True

Figure 20B

Figure 20A shows the logic diagram, 20B the truth table and matrix circuit diagram. The full adder is implemented with the equivalent of three circuit packages. When the number of bits entering the adder increases, the use of other combinations of matrices can be factored to optimize the use of matrix sizes and driver circuits.

SUBTRACTER MATRIX

A subtracter is formed with complementary difference and borrow outputs with only one HM-80 8 x 5 diode matrix when combined with logic drivers. Figure 21 shows the truth table and the matrix circuit diagram. The complementary outputs are provided by this configuration with the equivalent of only two circuit packages.

X	1	0	0	0	1	1	1	0
Y	0	1	0	1	1	1	0	0
B	0	1	1	0	1	0	1	0
B_0	0	1	1	1	1	0	0	0
D	1	0	1	1	1	0	0	0

QUANTITY AND CIRCUIT TYPE
1) HM-80 8 x 5 MATRIX
1/3) HEX INVERTER
2) MATRIX DRIVERS

Note: Positive Logic True

Figure 21A

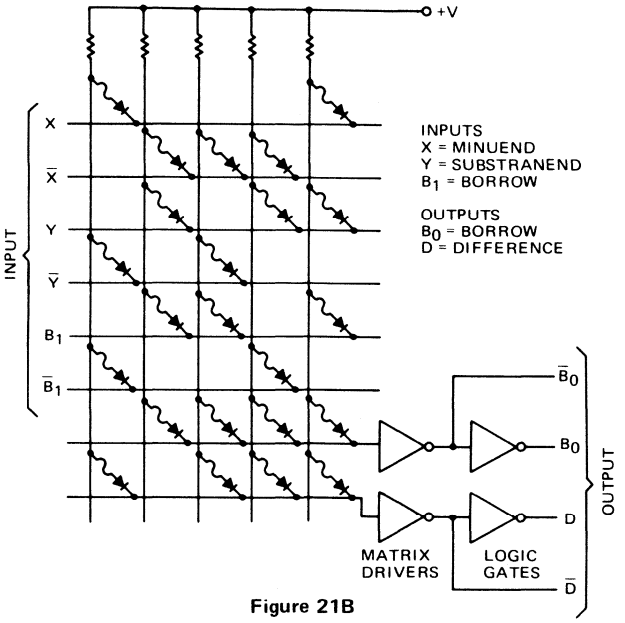


Figure 21B

SHIFT REGISTER MATRICES

A general application of the diode matrix is in the decoding of counters. A particular counter configuration is usually chosen to satisfy systems requirements and/or minimum package count. Examples of encoding and decoding matrices have been shown in Figures 15, 16, 18 and 19. In these cases, however, it is usually necessary to provide buffer storage to allow adequate time to perform the desired output.

Another application is to convert a counter output sequence into an output sequence which simulates an active counter of a different logic organization. The sequential events of the master counter then controls the equivalent decoded sequence. This eliminates the need for and problem of synchronizing two counters in many applications. The reduction in hardware, not only of the decode functions, but of the additional counter increases the design value of the matrix approach.

MODULO 5 SHIFT CODE - BCD

As an example, a Modulo 5 shift register output is decoded to MOD-5 BCD using only one HM-80 8 x 5 diode matrix. Any three bit weighted code can be used as an alternate for the output with the appropriate matrix pattern. As an application, the output code in this case can be used to keep track of the shift counter state.

Figure 22 shows the truth table and the matrix circuit diagram.

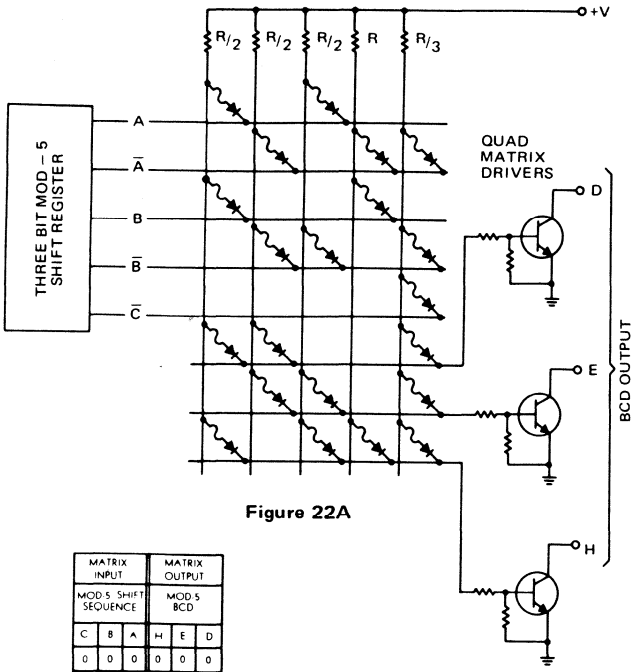


Figure 22A

MATRIX INPUT			MATRIX OUTPUT		
MOD 5 SHIFT SEQUENCE			MOD 5 BCD		
C	B	A	H	E	D
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	1	0	0	1	1
1	0	0	1	0	0

Note: Positive Logic True

QUANTITY AND CIRCUIT TYPE
1) HM-80 8 x 5 MATRIX
3) MATRIX DRIVERS

Figure 22B

BCD-MOD - 5 - SHIFT CODE

Figure 23 shows a BCD input decoded to a MOD-5 shift register and its complement using a similar matrix.

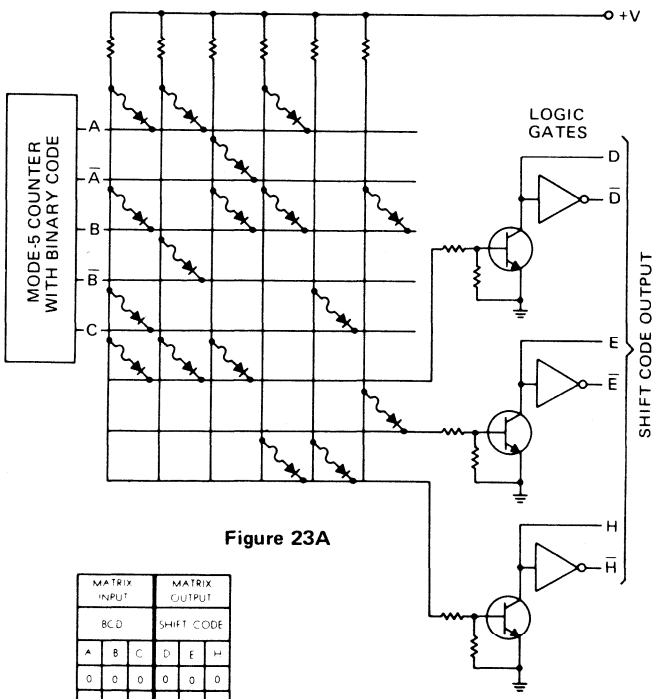


Figure 23A

MATRIX INPUT			MATRIX OUTPUT		
BCD			SHIFT CODE		
A	B	C	D	E	H
0	0	0	0	0	0
1	0	0	1	0	0
0	1	0	1	1	0
1	1	0	0	1	1
0	0	1	0	0	1

Note: Positive Logic True

QUANTITY AND CIRCUIT TYPE
1) HM-40 8 x 6 MATRIX
½) HEX INVERTER
3) MATRIX DRIVERS

Figure 23B

MODULO 10 BCD

Another example is shown in Figure 24 where a 4·2·2·1 BCD counter is decoded to give an equivalent modulo 10 shift register output. Figure 24A is the truth table and 24B the matrix circuit. Only five packages are required for this decode matrix. The five bit output shift sequence is equivalent to a ten-state Johnson counter.

MONOLITHIC DIODE MATRIX MEMORIES

A valuable application of the diode matrix is in read-only memories. The fixed pattern of the diode matrix, obtained by the fuse link technique, provides easy fabrication and updating of memory arrays.

The permanence of the fused link diode matrix provides a memory storage element which is non-volatile and has non-destructive read-out characteristics.

Large memory arrays can be constructed from smaller matrix sizes, making the size and construction of the memory very flexible.

Conventional memories required all information to be mass stored in one memory subsystem in order to economically share the cost of access circuitry. The diode matrix memory can be subdivided and distributed throughout the system. This is possible because the drive requirements for a diode matrix memory can be greatly reduced over conventional memory techniques. In typical applications the memory cell is driven at a unit logic level.

The matrix memory also offers extremely fast access time since the drive and selection circuitry can operate at logic current levels at compatible logic gate speeds.

The reduced power requirement of the access circuitry allows it to be reproduced economically many times. This allows the large memory to be partitioned into smaller functional memories. In addition to the smaller size, the organization is simpler and access times are greatly reduced.

The ability to fabricate small functional memories from standard logic elements has considerable value. Memory design is simplified to the assembly of standard elements with all the design flexibility offered by standard logic gates. The compatible packaging offered by this approach to the memory

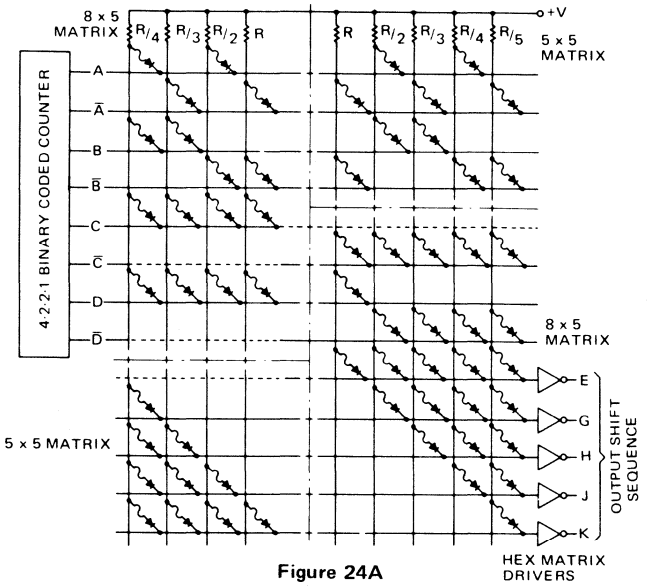


Figure 24A

MATRIX INPUT 4·2·2·1 BCD				MATRIX OUTPUT SHIFT SEQUENCE				
D	C	B	A	K	J	H	G	E
0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0
0	0	1	0	1	1	0	0	0
0	0	1	1	1	1	1	0	0
1	0	0	0	1	1	1	1	0
1	0	1	1	1	1	1	1	1
1	1	0	0	0	1	1	1	1
1	1	0	1	0	0	1	1	1
1	1	1	0	0	0	0	1	1
1	1	1	1	0	0	0	0	1

QUANTITY & CIRCUIT TYPE
2) HM-80 8 x 5 MATRIX
2) HM-74 5 x 5 MATRIX
Input circuits not included

Note: Positive Logic True

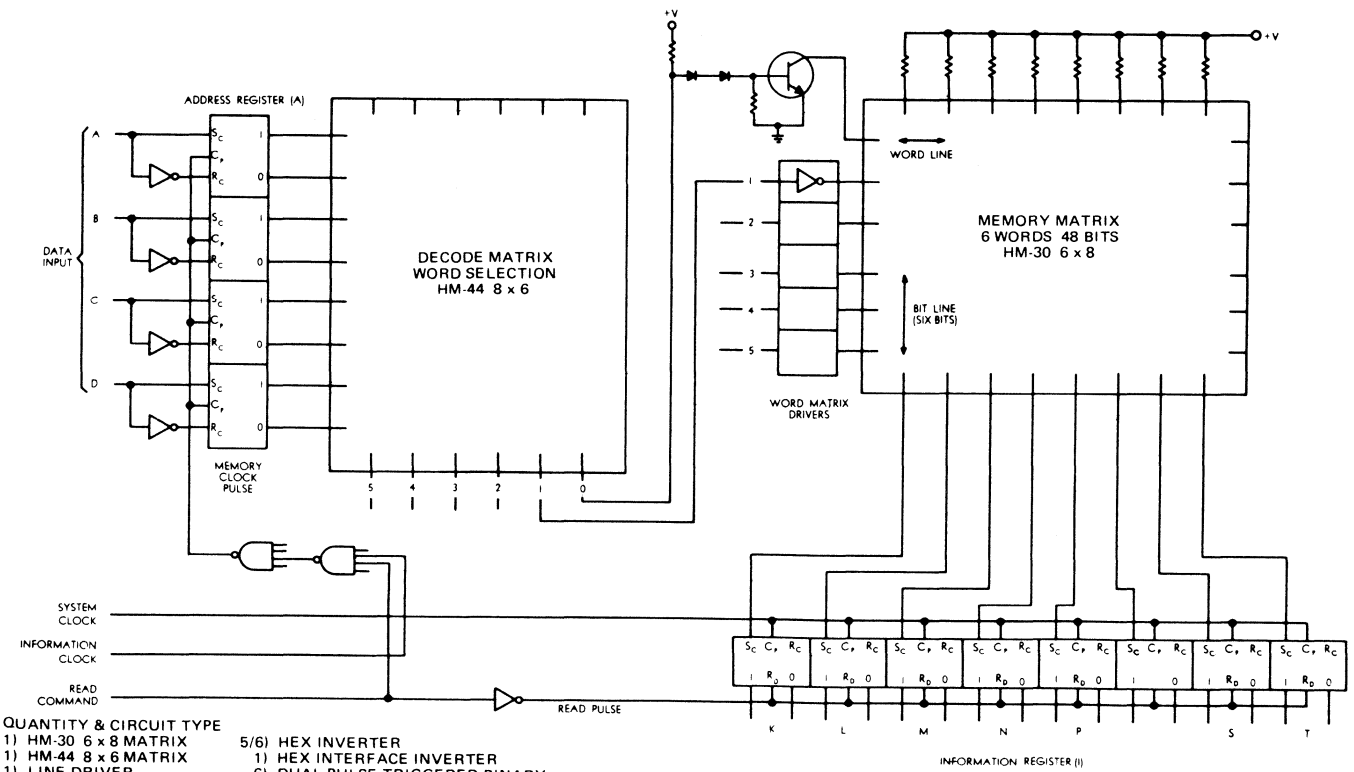
Figure 24B

and logic system would greatly decrease system costs. Several fixed memory examples are given. Two examples of very small memories are used here to center attention on the use of the diode matrix in memory organization. The specific examples given are used only to illustrate the principles of fixed memory applications using integrated diode matrices for building blocks.

READ-ONLY MEMORY

A small six word (8 bits per word) read-only memory is shown in Figure 25A and the timing diagram 25B. The memory is organized as a conventional memory with address register (A), address matrix decode, memory array, and information output register (I). Storage is provided by an HM-30 6 x 8 diode matrix which has a fused diode matrix which has a fused diode pattern representing the fixed stored data. Each word line or matrix row contains a word. Each bit line or matrix column contains six bits. All access circuitry is constructed from standard logic gates.

Operation of the memory is as follows: address information is presented to the address register (A) and is stored at memory clock time (T_M). The address register is decoded to select a word line. The read pulse activates the information (I) register. The eight bits of the selected word provide clock gate control to the information (I) register. The word is transferred to the (I) register at information clock time (T_I). The



QUANTITY & CIRCUIT TYPE
1) HM-30 6 x 8 MATRIX
1) HM-44 8 x 6 MATRIX
1) LINE DRIVER
5/6) HEX INVERTER
1) HEX INTERFACE INVERTER
6) DUAL PULSE TRIGGERED BINARY
1) 8 RESISTOR & 6 RESISTOR NETWORK

Figure 25A

APP. NOTES

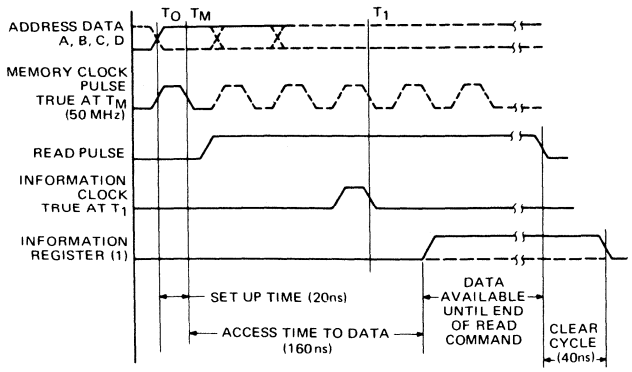


Figure 25B

selected word is stored until the read command removes the read pulse. The information register is then inhibited. This constitutes the complete read cycle. The clear cycle is the reset time of the (I) register. Using standard circuits, the memory can be constructed with a read cycle of 180ns and clear cycle of 40ns.

The memory is more attractive if the number of words is expanded to twelve (total of 96 bits). In this case, a second HM-30 6 x 8 memory matrix is added; the decode matrix is expanded to an 8 x 12, two 8 x 6 matrices, to perform word selection. Two quads 2-input gates are added between the memory matrices and the (I) register to select the proper word (see Figure 25C).

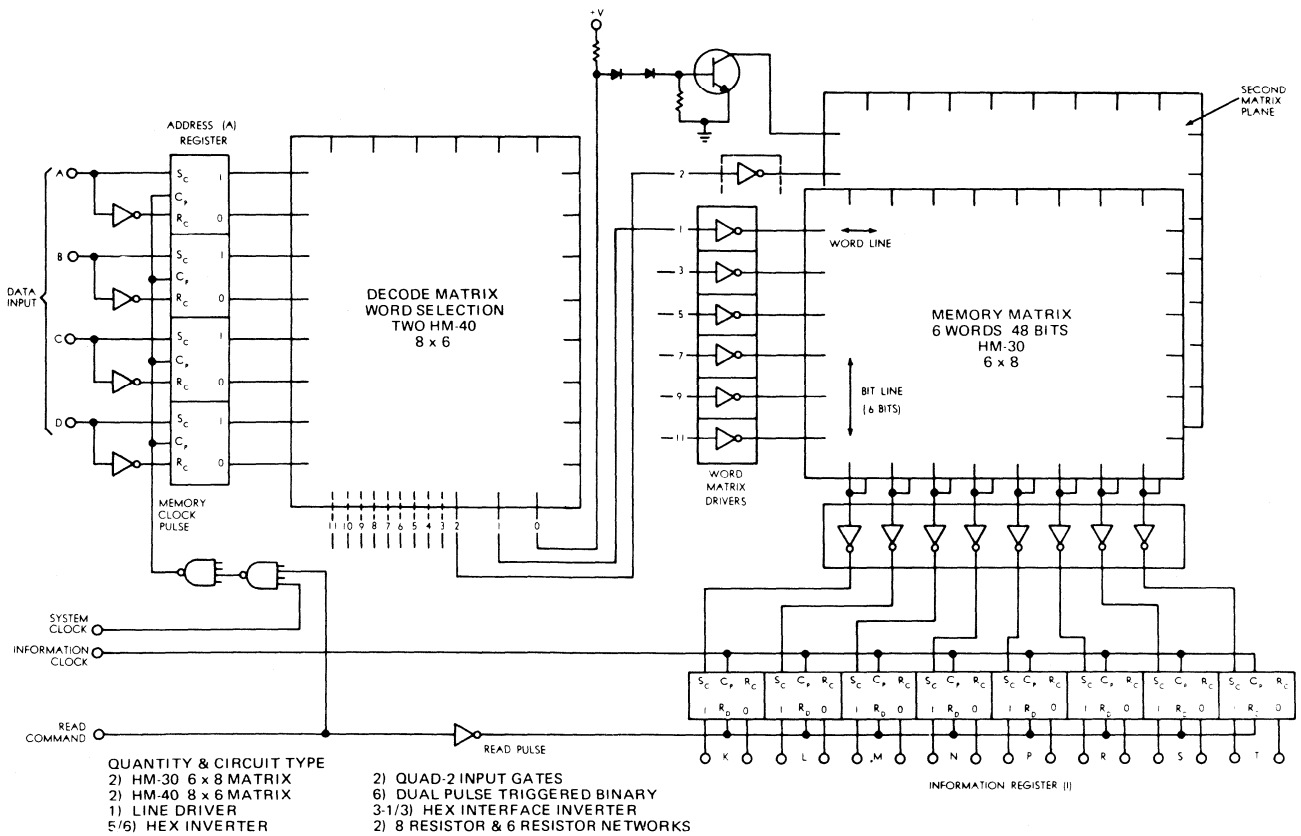
The memory read cycle is increased to 200ns. Even with this organization the cost per bit for circuitry is less than the equivalent memory with storage elements constructed from flip-flops.

This small, read-only memory has several features which make the present organization complicated. It requires two clock pulses and a read command; a high speed clock (50 MHz) to operate at minimum cycle time; and the decode matrix is limited in the two examples to decoding less than the total possible states of the address data.

SIMPLIFIED READ-ONLY MEMORY

Although the fixed diode memory can be constructed as shown in Figure 25, there is a much simpler approach to the same memory. Figure 26A shows the same functional memory constructed from a larger matrix where the decoding, word selection and storage functions are combined into one matrix. The block diagram in Figure 26 shows the simplicity of this memory system.

The timing diagram of Figure 26B shows a read cycle time of 80ns and a clear cycle



QUANTITY & CIRCUIT TYPE
2) HM-30 6 x 8 MATRIX
2) HM-40 8 x 6 MATRIX
1) LINE DRIVER
5/6) HEX INVERTER
2) QUAD-2 INPUT GATES
6) DUAL PULSE TRIGGERED BINARY
3-1/3) HEX INTERFACE INVERTER
2) 8 RESISTOR & 6 RESISTOR NETWORKS

Figure 25C

APP. NOTES

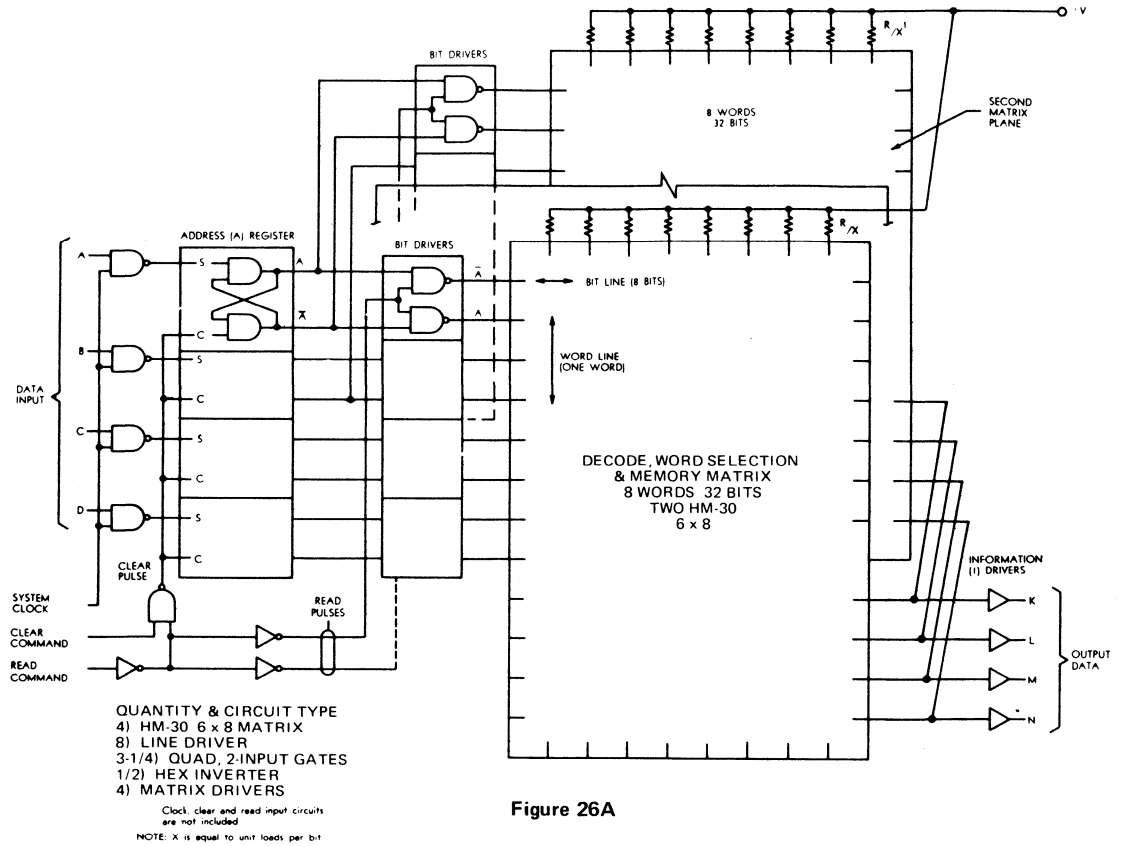


Figure 26A

time of 40ns. Compared to the memory of Figure 25, the read cycle time has been reduced to less than half and the data access time to one third. The memory size shown here is 16 words of four bits each (total 64 bits).

The memory operates in a similar manner to the one in Figure 25. Data is clocked into the address register (A) at memory clock time (T_M). A clear pulse during the first half of the clock pulse is necessary, however, to clear the (A) register. Register (A) drives the bit drivers. The read pulse inhibits the bit drivers until the read command is present. The decode of the address word, selection, and storage of output data are all performed in the memory matrix. The memory matrix drives the information (I) drivers which provide the data at compatible logic levels.

No output register is provided in this memory and therefore there is no need for an information clock. The read pulse provides the means of locking up the memory by controlling the clear pulse to the address register (A). Once the memory is locked up, the output data is available until the end of the read command. The faster access and cycle times are provided by only a 33 MHz clock.

The memory illustrated here is limited to 16 words but can be expanded in bits per word. In this case, the major change would be in the organization of the matrix. For a word length of 8 bits, three memory planes are required, each plane comprised of two HM-040 8 x 6 diode matrices. The two additional planes require four more line drivers and one inverter, plus four more matrix drivers to obtain the eight-bit output. The memory storage has now increased to 128 bits. For expansion beyond this illustration the organization must be considered in light of the specific application.

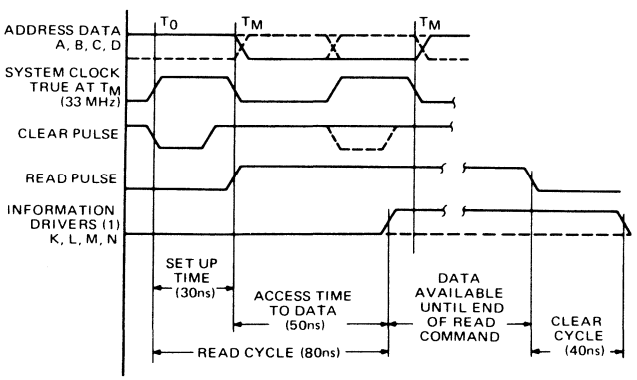


Figure 26B

As shown above, Harris diode matrices can be used in a large variety of interesting and useful applications. With the growing popularity of CMOS and other high threshold logic families, this number will continue to increase. For further information regarding Harris diode matrices, contact your nearest Harris representative or call us direct at the factory.

Dash 8

MIL-STD-883 Off-the-Shelf

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

DASH 8

MIL-STD-883

OFF-THE-SHELF DELIVERY

MIL-STD-883/MIL-M-38510 Reliability Assurance Program

INTRODUCTION

STATEMENT OF SCOPE

This specification establishes the detail requirements for Harris' Circuits screened and tested under the DASH 8 Program.

The Harris DASH 8 Devices pass the screening requirements of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document.

APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent referenced herein:

MIL-M-38510A	"Microcircuit Quality and Reliability Assurance, General Specification for."
MIL-STD-883 (Notice 3)	"Test Methods and Procedures for Microelectronics"

Harris maintains a product assurance program (PAP) using MIL-M-38510, Appendix A, as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

Systems and procedures used are in accordance with NASA Publication 200-3, MIL-Q-9858A and MIL-STD-883.

MIL-STD-883, METHOD 5004, CLASS B,
100% SCREENING PROCEDURE

	SCREEN	METHOD
1	Internal Visual (Precap)	2010 Condition B
2	Stabilization Bake	1008, Condition C, 24 Hours minimum
3	Temperature Cycling	1010, Condition C
4	Constant Acceleration	2001, Condition E Y_1 Plane, 30K G's minimum
5	Seal, Fine Leak	1014, Condition A
6	Seal, Gross Leak	1014, Condition C Omit Step 1, No vacuum Preconditioning Step 2
7	Burn-In	Method 1015, 168 hours @ 125°C (Burn-In Circuit Enclosed).
8	Final Electrical 8.1 D. C. Tests at 25°C, Maximum and minimum operating temperatures 8.2 A. C. Tests at 25°C	Per appropriate Harris DASH 8 Data Sheet
9	External Visual	Method 2009

MIL-STD-883, METHOD 5005, CLASS B

10	Lot Acceptance	Group A, Table 1, Subgroup 1, 2, 3 & 4

NOTE:

LOT DEFINITION: Production Lot and Inspection Lot shall be as defined in MIL-M-38510.

TRACEABILITY: All devices are assigned lot code identification that provides traceability back to the individual wafer fabrication run.

BRANDING: All devices are branded with the HX-XXXX-8 and Harris wafer run date code.

AGED PRODUCT: Product that has been held for more than six months will be rescreened to Group A requirements prior to shipment.

ADDITIONAL REQUIREMENTS: Attributes data will be supplied on Burn-In and Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request; The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all product families in manufacturing. This program provides life test performance results to fulfill customer reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

For customers desiring Lot Qualification, Harris Semiconductor will perform the Group A, Group B and Group C tests to MIL-STD-883, Method 5005.

MIL-STD-883, METHOD 5005.1, GROUP B

TEST	METHOD	CONDITION	QUALITY CONFORMANCE INSPECTION 2/ CLASS B LTPD	QUALIFICATION INSPECTION CLASS B LTPD
SUBGROUP 1				
Physical dimensions	2008	Test condition A	15	10
SUBGROUP 2				
(a) Marking permanency	2008	Test condition B, 3.2.1	4 devices (no failures)	4 devices (no failures)
(b) Visual and mechanical	2008	Test condition B with criteria from design and construction requirements of applicable procurement document.	1 device (no failures)	1 device (no failures)
(c) Bond strength (see 3.7)	2011		15	10
(1) Thermocompression		(1) Test condition B,C or D		
(2) Ultrasonic or wedge		(2) Test condition C or D		
(3) Flip-chip		(3) Test condition F		
(4) Beam lead		(4) Test condition B,C or F		
SUBGROUP 3				
Solderability	2003	Soldering temperature of 250 ± 10°C.	15	10
SUBGROUP 4				
Lead fatigue	2004	Test condition B_2.	15	10
Seal 1/	1014	As applicable.		
(a) Fine				
(b) Gross				

1/ The order of performing the seal test, fine and gross, may be inverted when the fluorocarbon gross method, test condition C, is specified.

2/ Generic data from Harris Reliability Add-On Program available upon request.

MIL-STD-883, METHOD 5005.1, GROUP C

TEST	METHOD	CONDITION	QUALITY CONFORMANCE INSPECTION 4/ CLASS B LTPD	QUALIFICATION INSPECTION CLASS B LTPD
SUBGROUP 1				
Thermal shock	1011	Test condition B as a minimum.	15	10
Temperature cycling	1010	Test condition C.		
Moisture resistance 1/	1004			
Seal 2/ (a) Fine (b) Gross	1014	As applicable.		
End point elec. parameters		As specified in the applicable procurement document.		
SUBGROUP 2				
Mechanical shock	2002	Test condition B	15	10
Vibration, variable frequency	2007	Test condition A		
Constant acceleration	2001	Test condition E		
Seal 2/ (a) Fine (b) Gross	1014	As applicable.		
End point elec. parameters		As specified in the applicable procurement document.		
SUBGROUP 3				
Salt atmosphere	1009	Test condition A	15	10
SUBGROUP 4				
High temperature storage 3/	1008	$150\ ^{+50}_{-25}$ °C storage, 1000 hours.	7	5
End point elec. parameters		As specified in the applicable procurement document.		
SUBGROUP 5				
Operating life test 3/	1005	Test condition to be specified in the applicable procurement document (1000 hours).	5	3
End point elec. parameters		As specified in the applicable procurement document.		

1/ Omit the vibration subcycle of step 7B of Method 1004.
2/ The order of performing the seal test, fine and gross, may be inverted when the fluorocarbon gross method, test condition C is specified.
3/ See 40.4 of appendix B of MIL-M-38510.
4/ Generic data from Harris Reliability Add-On Program available upon request.

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